19-2119; Rev 0; 8/01

MAXIM

Flash Programmable 12-Bit Integrated Data-Acquisition Systems

MAX7651/MAX7652

General Description

The MAX7651/MAX7652 are complete 12-bit data-acquisition systems featuring an algorithmic, switched-capacitor, analog-to-digital converter (ADC), a pulse-width-modulated digital-to-analog converter (DAC), three timer/counters, and an industry-standard 8051 microprocessor core with a variety of I/O peripherals. Power-down capability and full functionality with supply voltages as low as +3V make the MAX7651/MAX7652 suitable for portable and power-sensitive applications.

The MAX7651/MAX7652 perform fully differential voltage measurements with 12-bit resolution, programmable gain, and separate track-and-hold for both positive and negative inputs. The converter accepts versatile input modes consisting of four 2-channel signal pairs or eight 1-channel signals relative to a floating common.

The MAX7651/MAX7652 microprocessor systems feature a CPU, 256 bytes of RAM, two 8kB flash memory, four 8-bit I/O ports, two UARTs, an interrupt controller, and a watchdog timer. Only four clock cycles are required to complete each microprocessor instruction.

The MAX7651/MAX7652 are available in 64-pin TQFP packages.

Applications

Hand-Held Instruments
Portable Data-Acquisition Systems
Temperature Controllers
Smart Transmitters
Data Loggers
Multi-Channel Data-Acquisition with Data Formatting

Features

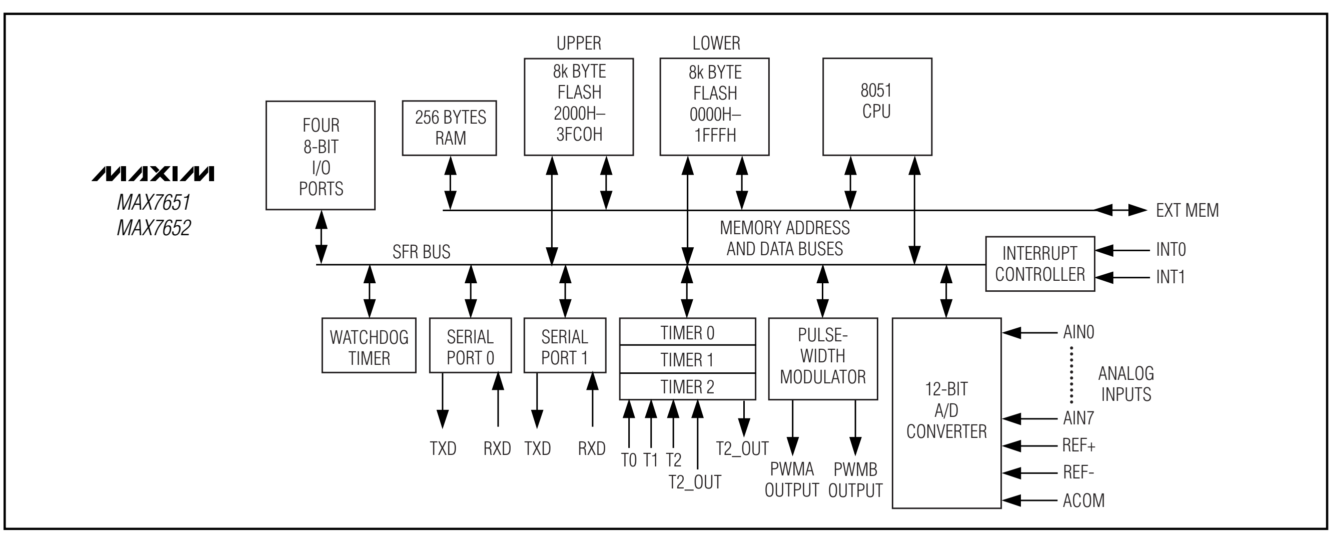
- ♦ **12-Bit 53ksps ADC with Fully Differential Inputs**
- ♦ **Dual 8-Bit PWM DAC Outputs**
- ♦ **Three Timers**
- ♦ **4-Clock Cycle 8051-Compatible Instruction Set with Dual Data Pointers**
- ♦ **Programmable Watchdog Supervisor**
- ♦ **Four Parallel I/O Ports**
- ♦ **Dual Serial I/O Ports (up to 375kb)**
- ♦ **+3V or +5V Single-Supply Operation**
- ♦ **DC to 12MHz Clock Speed**
- ♦ **64-Pin TQFP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX7651CCB	0°C to +70°C	64 TQFP
MAX7651ECB	-40°C to +85°C	64 TQFP
MAX7652CCB	0°C to +70°C	64 TQFP
MAX7652ECB	-40°C to +85°C	64 TQFP

Pin configuration appears at end of data sheet.

Functional Diagram



Flash Programmable 12-Bit Integrated Data-Acquisition Systems

ABSOLUTE MAXIMUM RATINGS

AV_{DD}, PWMV, DV_{DD} to AGND_ ....-0.3V to +6V
AV_{DD}, DV_{DD} to DGND...-0.3V to +6V
AV_{DD} to DV_{DD} ....-0.3V to +0.3V
AGND, PWMG to DGND ....-0.3V to +0.3V
Analog Inputs (AIN_, ACOM, XTAL1, XTAL2)
to AGND...-0.3V to $AV_{DD\_}$ + 0.3V
Analog Outputs (PWMA, PWMB)
to AGND_...-0.3V to $AV_{DD\_}$ + 0.3V
Digital I/O (A_, AD_, ALE/$\overline{PROG}$, $\overline{EA}$/V_{PP}, $\overline{INT0}$,
$\overline{INT1}$, P_._, $\overline{PSEN}$, RST) to DGND ....-0.3V to DV_{DD} + 0.3V
REF+, REF- to AGND_.............................-0.3V to $AV_{DD\_}$ + 0.3V
Short-Circuit Duration (PWM_, P_._, ALE/$\overline{PROG}$, $\overline{PSEN}$)..........1s
Continuous Power Dissipation (T_A = +70°C)
64-Pin TQFP (derate 5.00mW/°C above +70°C).........500mW
Operating Temperature Range
MAX765_CCB ....0°C to +70°C
MAX765_ECB ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX7651 $AV_{DD} = V_{PWMV} = DV_{DD} = V_{REF+}$ = +4.5V to +5.5V, V_{REF-} = 0, f_{XTAL} = 12MHz. MAX7652 $AV_{DD} = V_{PWMV} = DV_{DD}$ = +2.7V to +3.6V, V_{REF+} = +2.5V, V_{REF-} = 0, $A_{COM} = A_{VDD}/2$, f_{XTAL} = 12MHz. $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution	RES			12			bits
Relative Accuracy (Note 1)	INL	Differential	MAX7651			±1.5	LSB
			MAX7652			±1.0	
		Single-ended	MAX7651			±4.0	
			MAX7652			±1.5	
Differential Nonlinearity (Note2)	DNL	Differential			±0.5	±1	LSB
		Single-ended			±0.5	±1	
Offset Error (Note 2)					±2.3	±7	LSB
Offset Temperature Coefficient					±0.25		LSB/°C
Gain Error (Note 2)						3	%
Gain Temperature Coefficient					±3		ppm/°C
Channel-to-Channel Matching (Note 2)		Offset and gain			±0.25		LSB
DYNAMIC SPECIFICATIONS (53ksps, 1kHz SINE-WAVE INPUT, 5Vp-p (MAX7651), 2.5Vp-p (MAX7652))							
Signal-to-Noise + Distortion	SINAD	Differential			71		dB
		Single-ended			67		
Total Harmonic Distortion	THD	All unaliased harmonics	Differential		-78		dB
			Single-ended		-73		
Spurious-Free Dynamic Range	SFDR	Differential			81		dB
		Single-ended			79		
Channel-to-Channel Crosstalk		(Note 3)			-85		dB
Small-Signal Bandwidth		-3dB rolloff			1		MHz
Full-Power Bandwidth					1		MHz

ELECTRICAL CHARACTERISTICS (continued)

(MAX7651 AV_{DD} = V_{PWMV} = DV_{DD} = V_{REF+} = +4.5V to +5.5V, V_{REF-} = 0, f_{XTAL} = 12MHz. MAX7652 AV_{DD} = V_{PWMV} = DV_{DD} = +2.7V to +3.6V, V_{REF+} = +2.5V, V_{REF-} = 0, A_{COM} = A_{VDD}/2, f_{XTAL} = 12MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION RATE						
Conversion Time	t_{CONV}	f_{XTAL} = 12MHz	18.7			µs
Conversion Rate		f_{XTAL} = 12MHz			53.6	ksps
ANALOG INPUTS (AIN0–AIN7, ACOM)						
Input Voltage Range			0		AV_{DD}	V
Common-Mode Range			0		AV_{DD}	V
Input Current					1	µA
Input Capacitance	C_{IN}			10		pF
DIGITAL INPUTS						
Input Voltage Low	V_{IL}		-0.5		0.2 x (DV_{DD} - 1)	V
Input Voltage High	V_{IH}	Input high voltage, except XTAL and RST	0.2 x (DV_{DD} + 0.9)		DV_{DD} + 0.5	V
		Input high voltage, XTAL and RST	0.7 x (DV_{DD} + 0.1		DV_{DD} + 0.5	
Internal Reset Pulldown Resistance	R_{RST}	MAX7651	90		409	kΩ
		MAX7652	170		490	
Logical High-to-Low Transition Current	I_{TL}	Guaranteed by design			750	µA
Logical Zero Input Current, Ports 1, 2, and 3 ALE, $\overline{\text{PSEN}}$		(Note 4)			75	µA
Input Leakage Current, Port 0	I_{IN}	V_{IN} = DV_{DD} or DGND			±10	µA
Input Capacitance				10		pF
DIGITAL OUTPUTS						
Output Low Voltage	V_{OL}	I_{SINK} = 4mA			0.45	V
Output High Voltage	V_{OH}	MAX7651: I_{SOURCE} = 4mA	2.4			V
		MAX7652: I_{SOURCE} = 2mA	2.4			

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ELECTRICAL CHARACTERISTICS (continued)

(MAX7651: $AV_{DD} = V_{PWMV} = DV_{DD} = V_{REF+}$ = +4.5V to +5.5V, V_{REF-} = 0, f_{XTAL} = 12MHz. MAX7652: $AV_{DD} = V_{PWMV} = DV_{DD}$ = +2.7V to +3.6V, V_{REF+} = +2.5V, V_{REF-} = 0, $A_{COM} = A_{VDD}/2$, f_{XTAL} = 12MHz. $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL VOLTAGE REFERENCE CHARACTERISTICS (REF+, REF-)						
Reference Voltage Range		$V_{REF+} - V_{REF-}$	0		AV_{DD}	V
Reference Input Current					35	µA
Reference Input Capacitance				10		pF
POWER REQUIREMENTS						
Analog Supply Current					5	mA
Digital Supply Current		MAX7651, during page erase			55	mA
		MAX7652, during page erase			40	
Idle-Mode Digital Supply Current		MAX7651		13	30	mA
		MAX7652		5	12	
Stop-Mode Supply Current		$I_{AVDD} + I_{DVDD}$ (Note 5)			10	µA
Analog Power-Supply Rejection Ratio	PSRR			-40		dB
PWM OUTPUTS						
Output Low Voltage		I_{SINK} = 2mA			0.4	V
Output High Voltage		I_{SOURCE} = 2mA	2.4			V
FLASH EXTERNAL PROGRAMMING (FIGURE 1, NOTE 6)						
Program Pulse Width	t_{PROGL}		$10t_{CK}$			ns
Program Address and Data Setup	t_{ASUW}	Guaranteed by design	$3t_{CK}$			ns
Program Cycle Time	t_{WRITE}	MAX7651	$7t_{CK}$ + 54000		$16t_{CK}$ + 72000	ns
		MAX7652	$7t_{CK}$ + 54000		$32t_{CK}$ + 72000	
Verify Address and Data Set	t_{ADSUR}		$3t_{CK}$			ns
Verify Access Time	t_{READ}				$9t_{CK}$ + 50	ns
Minimum P2.7 Pulse Width Low	t_{P27L}		$10t_{CK}$			ns
Minimum P2.7 Pulse Width High	t_{P27H}	Guaranteed by design	$3t_{CK}$			ns
Clock Period	t_{CK}		83		250	ns
FLASH EXTERNAL MASS ERASE (FIGURE 2, NOTE 6)						
Erase Mode Setup	t_{P23SU}		$3t_{CK}$			ns
Program Pulse Width	$t_{ERASLOW}$		$10t_{CK}$			ns
Erase Cycle Time	$t_{MASSERASE}$		8.29		11	ms

TIMING CHARACTERISTICS

(MAX7651: AV_{DD} = V_{PWMV} = DV_{DD} = V_{REF+} = +4.5 to +5.5V, V_{REF-} = 0, f_{XTAL} = 12MHz. MAX7652: AV_{DD} = V_{PWMV} = DV_{DD} = +2.7V to +3.6V, V_{REF+} = +2.5V, V_{REF-} = 0, ACOM = AV_{DD}/2, f_{XTAL} = 12MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Figure 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RST Pulse Width (High)			100 + (64 x t_{CK})			µs
EXTERNAL CLOCK						
Clock Frequency	f_{CK}				12	MHz
Clock Period	t_{CLCL}		83			ns
Clock High Time	t_{CHCX}		25			ns
Clock Low Time	t_{CLCX}		25			ns
Clock Rise Time	t_{CLCH}	Guaranteed by design			10	ns
Clock Fall Time	t_{CHCL}	Guaranteed by design			10	ns
INSTRUCTION TIMING CHARACTERISTICS						
ALE Pulse Width	t_{LHLL}		1.5t_{CLCL} - 20			ns
Address Valid to ALE Low	t_{AVLL}		0.5t_{CLCL} - 15			ns
Address Hold after ALE Low	t_{LLAX}		0.5t_{CLCL} - 20			ns
ALE Low to Valid Instruction In	t_{LLIV}				2.5t_{CLCL} - 35	ns
ALE Low to $\overline{PSEN}$ Low	t_{LLPL}		0.5t_{CLCL} - 10			ns
$\overline{PSEN}$ Pulse Width	t_{PLPH}		2t_{CLCL} - 15			ns
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}				2t_{CLCL} - 35	ns
Input Instruction Hold after $\overline{PSEN}$	t_{PXIX}		0			ns
Input Instruction Float after $\overline{PSEN}$	t_{PXIZ}				t_{CLCL} - 15	ns
Address to Valid Instruction In	t_{AVIV}				3t_{CLCL} - 50	ns
$\overline{PSEN}$ Low to Address Float	t_{PLAZ}				10	ns

TIMING CHARACTERISTICS (continued)

(MAX7651: AV_{DD} = V_{PWMV} = DV_{DD} = V_{REF+} = +4.5 to +5.5V, V_{REF-} = 0, f_{XTAL} = 12MHz. MAX7652: AV_{DD} = V_{PWMV} = DV_{DD} = +2.7V to +3.6V, V_{REF+} = +2.5V, V_{REF-} = 0, ACOM = AV_{DD}/2, f_{XTAL} = 12MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Figure 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MOVX TIMING CHARACTERISTICS (Note 6)						
$\overline{RD}$ Pulse Width	t_{RLRH}	t_{MCS} = 0, Guaranteed by design	$2t_{CLCL}$ - 20			ns
		t_{MCS} > 0, Guaranteed by design	t_{MCS} - 20			
$\overline{WR}$ Pulse Width	t_{WLWH}	t_{MCS} = 0	$2t_{CLCL}$ - 20			ns
		t_{MCS} > 0	t_{MCS} - 20			
$\overline{RD}$ Low to Valid Data In	t_{RLDV}	t_{MCS} = 0			$2t_{CLCL}$ - 55	ns
		t_{MCS} > 0			t_{MCS} - 55	
Data Hold After $\overline{RD}$	t_{RHDX}		0			ns
Data Float After $\overline{RD}$	t_{RHDZ}	t_{MCS} = 0			t_{CLCL} - 10	ns
		t_{MCS} > 0			$2t_{CLCL}$ - 10	
ALE Low to Valid Data In	t_{LLDV}	t_{MCS} = 0			$2.5t_{CLCL}$ - 58	ns
		t_{MCS} > 0			$1.5t_{CLCL}$ - 58 + t_{MCS}	
Port 0 Address to Valid Data In	t_{AVDV1}	t_{MCS} = 0			$3t_{CLCL}$ - 60	ns
		t_{MCS} > 0			$2t_{CLCL}$ - 61 + t_{MCS}	
Port 2 Address to Valid Data In	t_{AVDV2}	t_{MCS} = 0			$3t_{CLCL}$ - 60	ns
		t_{MCS} > 0			$2t_{CLCL}$ - 64 + t_{MCS}	
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	t_{MCS} = 0	$0.5t_{CLCL}$ - 5		$0.5t_{CLCL}$ + 10	ns
		t_{MCS} > 0	$1.5t_{CLCL}$ - 5		$1.5t_{CLCL}$ + 10	
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{MCS} = 0	t_{CLCL} - 10			ns
		t_{MCS} > 0	$2t_{CLCL}$ - 10			
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	t_{MCS} = 0	t_{CLCL} - 10			ns
		t_{MCS} > 0	$2t_{CLCL}$ - 10			

TIMING CHARACTERISTICS (continued)

(MAX7651: AV_{DD} = V_{PWMV} = DV_{DD} = V_{REF+} = +4.5 to +5.5V, V_{REF-} = 0, f_{XTAL} = 12MHz. MAX7652: AV_{DD} = V_{PWMV} = DV_{DD} = +2.7V to +3.6V, V_{REF+} = +2.5V, V_{REF-} = 0, ACOM = AV_{DD}/2, f_{XTAL} = 12MHz. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Figure 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	t_{MCS} = 0	-9			ns
		t_{MCS} > 0	t_{CLCL} - 12			
Data Valid Before $\overline{WR}$ High	t_{QVWH}	t_{MCS} = 0	$2t_{CLCL}$ - 20			ns
		t_{MCS} > 0	t_{MCS} - 30			
Data Hold After $\overline{WR}$ High	t_{WHQX}	t_{MCS} = 0	t_{CLCL} - 18			ns
		t_{MCS} > 0	$2t_{CLCL}$ - 18			
$\overline{RD}$ Low to Address Float	t_{RLAZ}				0	ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	t_{MCS} = 0	0		10	ns
		t_{MCS} > 0	t_{CLCL} - 5		t_{CLCL} + 11	
SERIAL PORT TIMING CHARACTERISTICS						
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0 (12 clocks/cycle)		$12t_{CLCL}$		ns
		SM2 = 1 (4 clocks/cycle)		$4t_{CLCL}$		
Output Data Setup to Clock Rising Edge	t_{QVXH}	SM2 = 0 (12 clocks/cycle)		$10t_{CLCL}$		ns
		SM2 = 1 (4 clocks/cycle)		$3t_{CLCL}$		
Output Data Hold after Clock Rising Edge	t_{XHQX}	SM2 = 0 (12 clocks/cycle)		$2t_{CLCL}$		ns
		SM2 = 1 (4 clocks/cycle)		t_{CLCL}		
Input Data Hold after Clock Rising Edge	t_{XHDX}	SM2 = 0 (12 clocks/cycle)		t_{CLCL}		ns
		SM2 = 1 (4 clocks/cycle)		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0 (12 clocks/cycle)		$11t_{CLCL}$		ns
		SM2 = 1 (4 clocks/cycle)		$3t_{CLCL}$		

Note 1: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the offset and gain errors have been nullified.

Note 2: AV_{DD} = +5.0V, (V_{REF}+) - (V_{REF}-) = +5.0V or AV_{DD} = +3.0V, (V_{REF}+) - (V_{REF}-) = +2.5V.

Note 3: Ground at “ON” channel; 10kHz sine-wave applied to all “off” channels.

Note 4: ALE and PSEN are in reset cycle.

Note 5: All digital inputs are at DGND or DV_{DD}. f_{XTAL} = 0.

Note 6: Table 1. Data Memory Stretch Values.

Note 7: The minimum frequency when writing to the internal flash is 4MHz.

Table 1. Data Memory Stretch Values

MD2	MD1	MD0	MEMORY CYCLES	READ/WRITE STROBE WIDTH (CLOCKS)	STROBE WIDTH TIME AT 12MHz	t_{MCS}
0	0	0	2	2	167ns	$0t_{CLCL}$
0	0	1	3 (default)	4	334ns	$4t_{CLCL}$
0	1	0	4	8	668ns	$8t_{CLCL}$
0	1	1	5	12	997ns	$12t_{CLCL}$
1	0	0	6	16	1330ns	$16t_{CLCL}$
1	0	1	7	20	1666ns	$20t_{CLCL}$
1	1	0	8	24	2000ns	$24t_{CLCL}$
1	1	1	9	28	2333ns	$28t_{CLCL}$

Table 2. External Flash Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.6	P3.7	P2.5
Write Lower FLASH	H	L	↑↓	H	L	H	H	H	L
Read Lower FLASH	H	L	H	H	L	↑↓	H	H	L
Write Lock Bit 1	H	L	↑↓	H	H	H	H	H	H
Write Lock Bit 2	H	L	↑↓	H	H	H	L	L	H
Write Lock Bit 3	H	L	↑↓	H	H	L	H	L	H
Mass Erase	H	L	↑↓	H	H	L	L	L	H
Read Sig Bytes	H	L	H	H	L	L	L	L	L
Write Upper FLASH	H	L	↑↓	H	L	H	H	H	H
Read Upper FLASH	H	L	H	H	L	↑↓	H	H	H

Note 1: To program the lock bits, ALE must be low for duration of “Write Lockbit” cycle.
Note 2: $\overline{INT0}$ and $\overline{INT1}$ are open-drain and must either be driven or require a pullup (typically 10kΩ) to DV_{DD}.

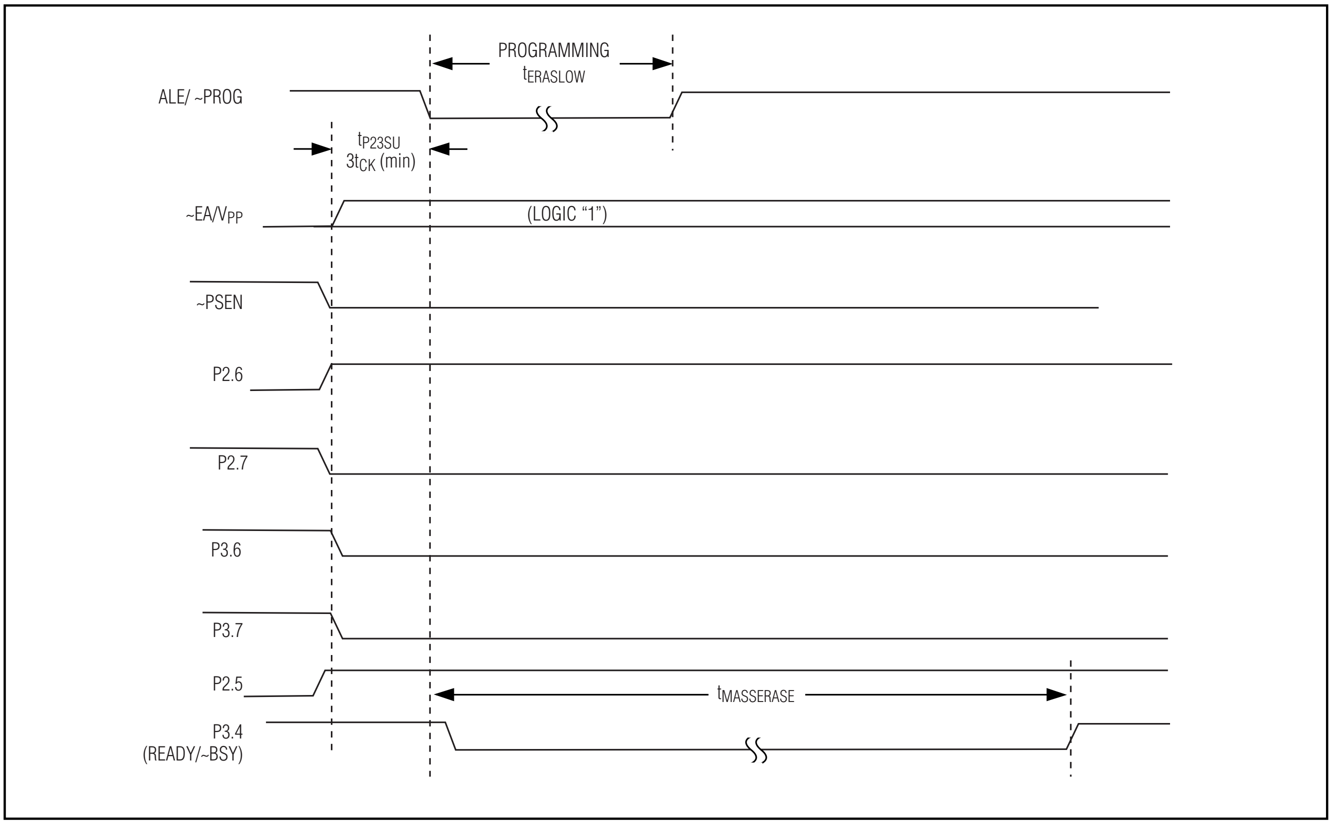

Figure 1. FLASH External Mass Erase Waveforms

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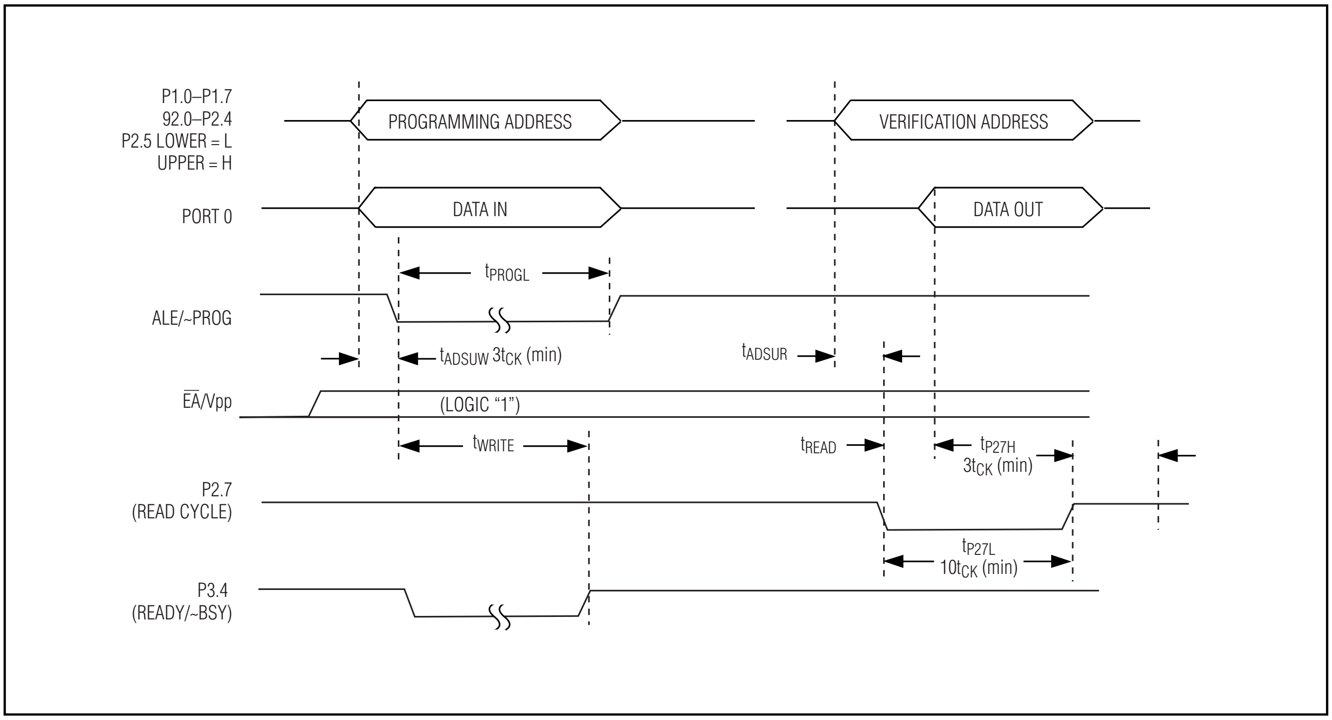


Figure 2. FLASH External Programming and Verification Waveforms

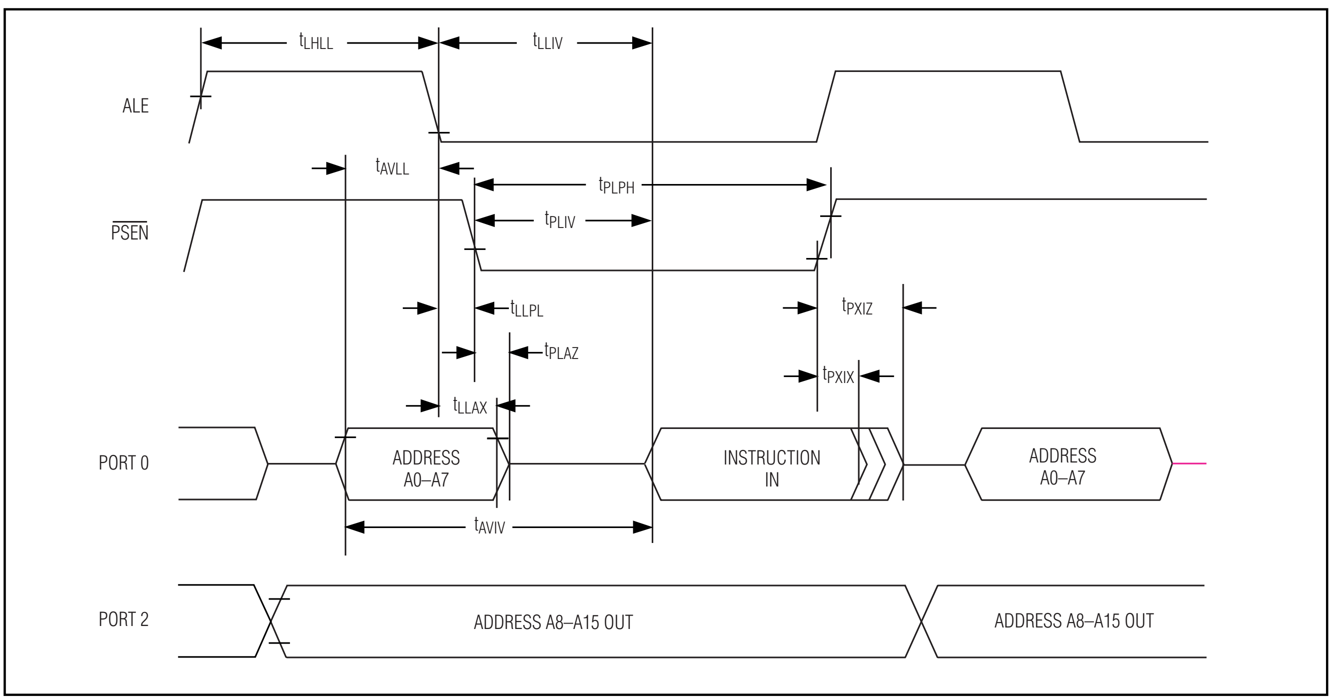


Figure 3a. External Program Memory Read Cycle

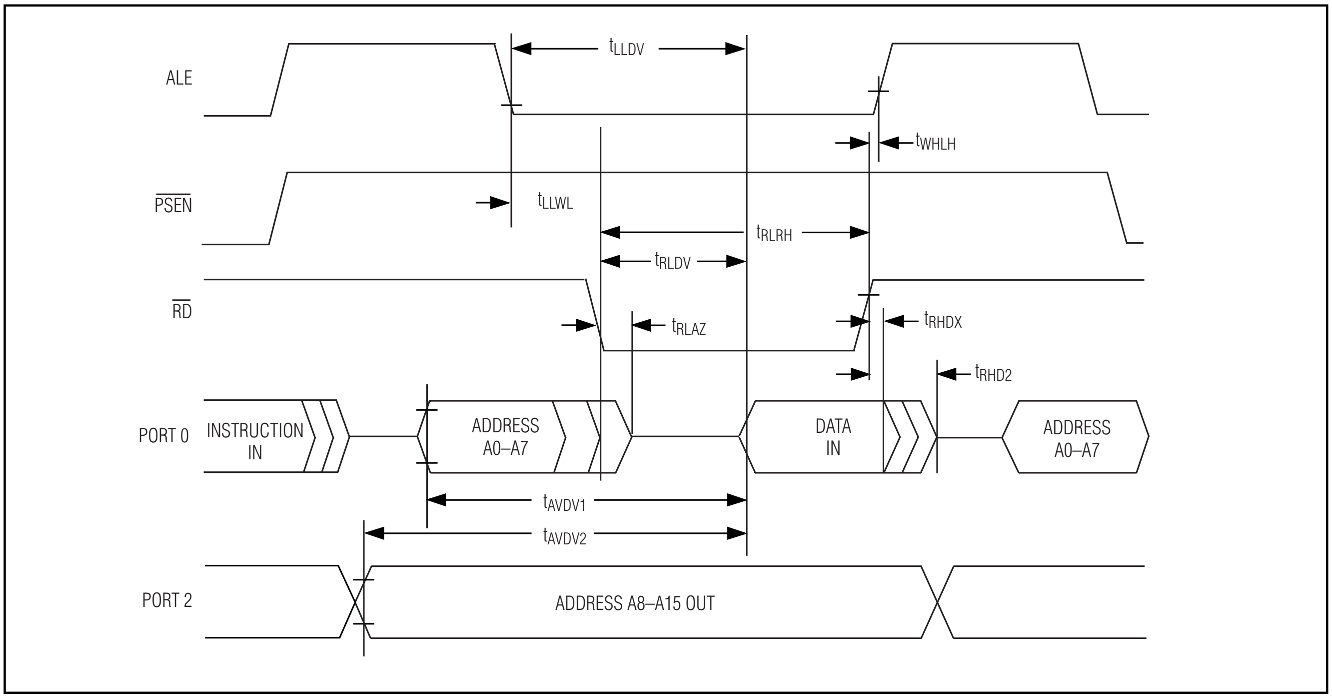


Figure 3b. External Data Memory Read Cycle

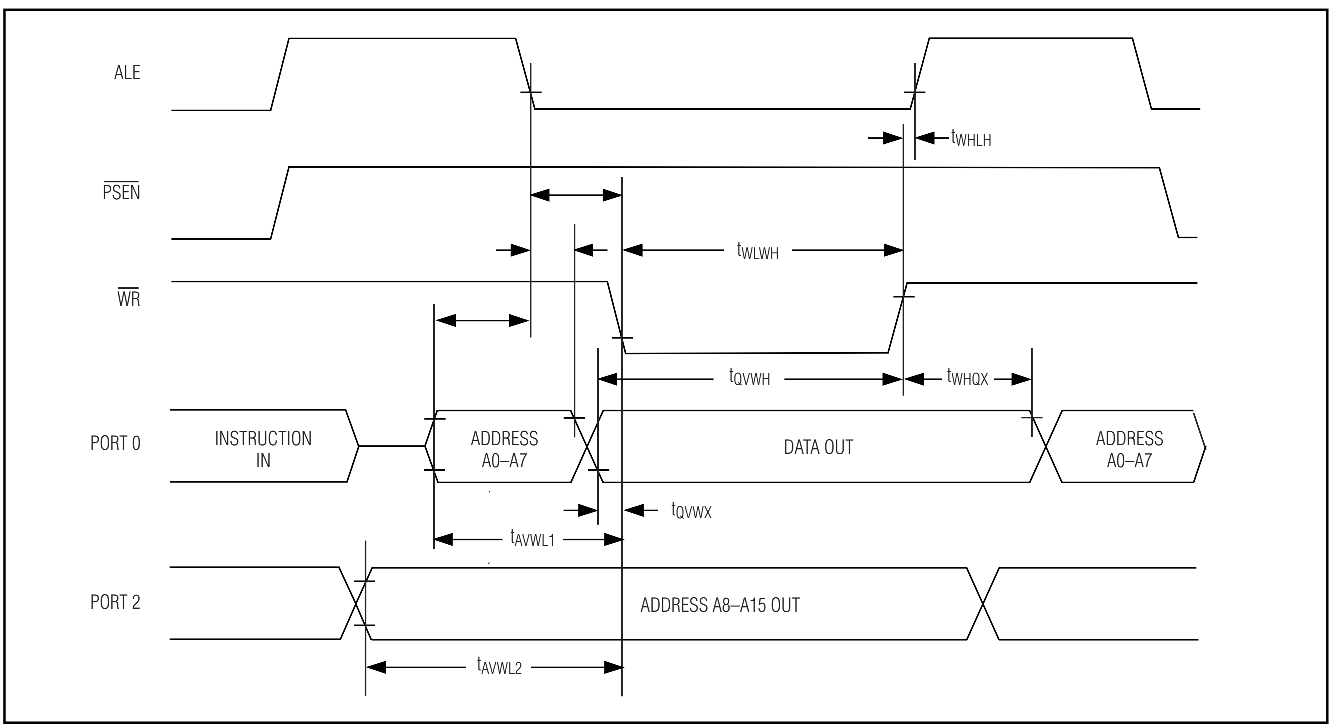


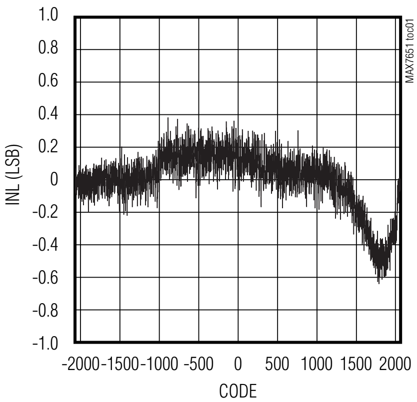
Figure 3c. External Program Memory Write Cycle

Flash Programmable 12-Bit Integrated Data-Acquisition Systems

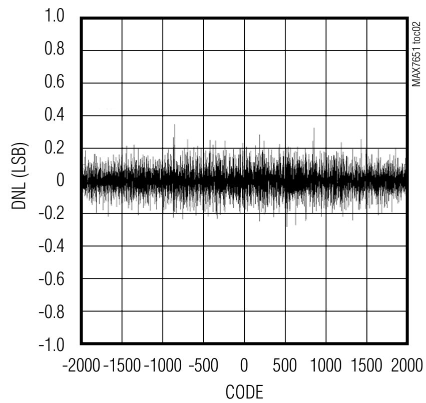
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)
MAX7651: $AV_{DD} = V_{PWMV} = DV_{DD} = V_{REF+}$ = 5.0V, V_{REF-} = 0, $V_{COM} = AV_{DD}/2$, f_{XTAL} = 12MHz.
MAX7652: $AV_{DD} = V_{PWMV} = DV_{DD} = V_{REF+}$ = 3.0V, V_{REF-} = 0, $V_{COM} = AV_{DD}/2$, f_{XTAL} = 12MHz.

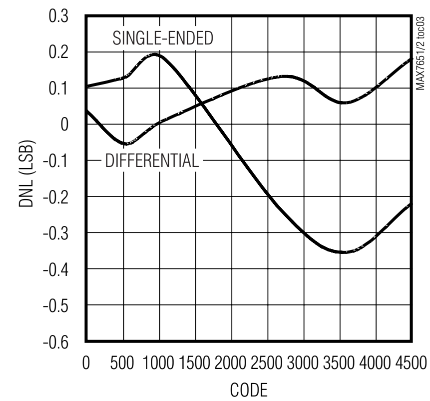
SINGLE-ENDED INL vs. OUTPUT CODE



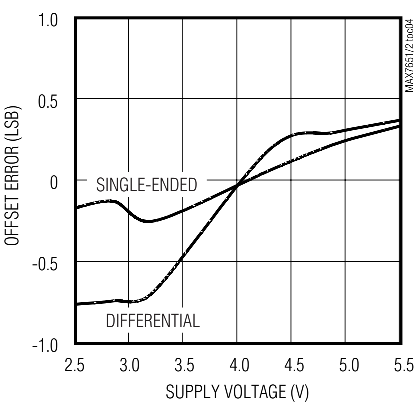
DNL vs. OUTPUT CODE



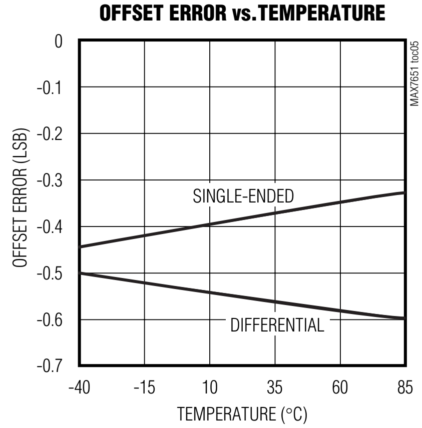
NEGATIVE GAIN ERROR vs. SUPPLY VOLTAGE



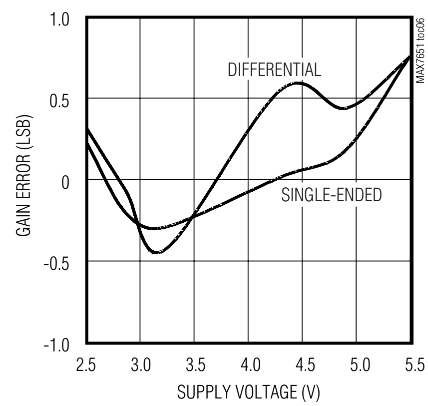
OFFSET ERROR vs. SUPPLT VOLTAGE



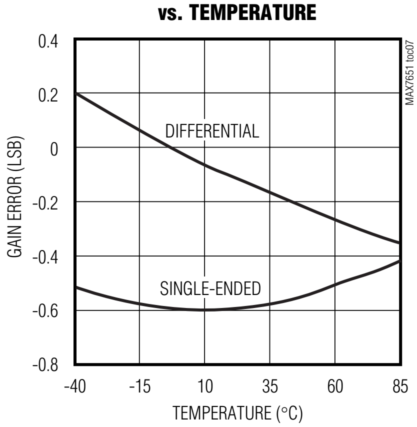
OFFSET ERROR vs.TEMPERATURE



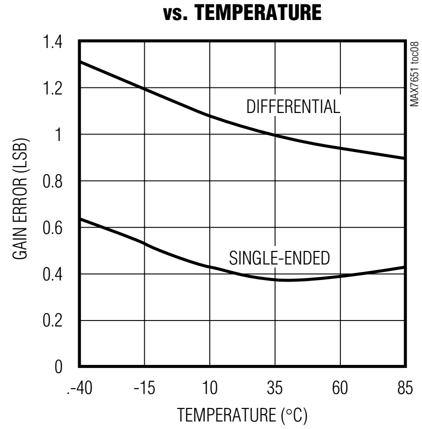
POSITIVE GAIN ERROR vs. SUPPLY VOLTAGE



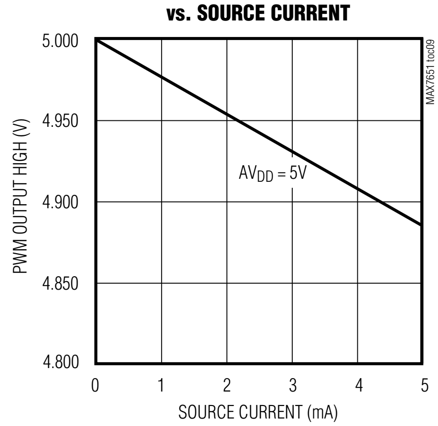
POSITIVE GAIN ERROR vs. TEMPERATURE



NEGATIVE GAIN ERROR vs. TEMPERATURE



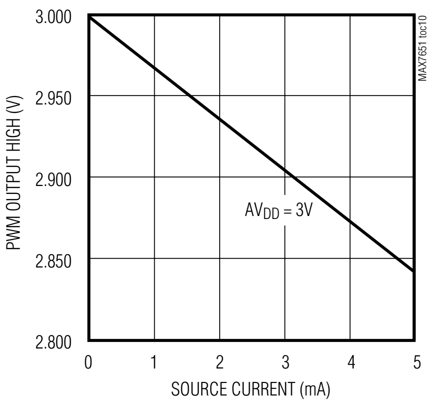
PWM OUTPUT HIGH vs. SOURCE CURRENT



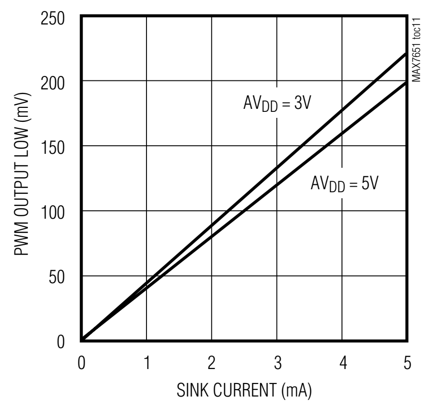
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)
MAX7651: $AV_{DD} = V_{PWMV} = DV_{DD} = V_{REF+}$ = 5.0V, V_{REF-} = 0, $V_{COM} = AV_{DD}/2$, f_{XTAL} = 12MHz.
MAX7652: $AV_{DD} = V_{PWMV} = DV_{DD} = V_{REF+}$ = 3.0V, V_{REF-} = 0, $V_{COM} = AV_{DD}/2$, f_{XTAL} = 12MHz.

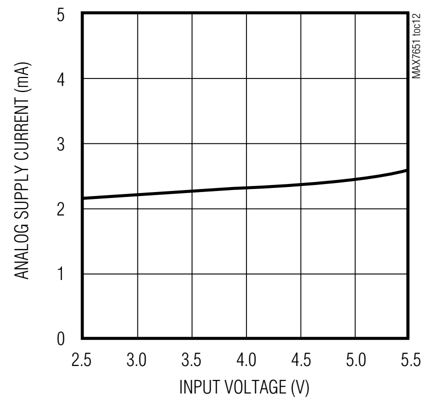
PWM OUTPUT HIGH vs. SOURCE CURRENT



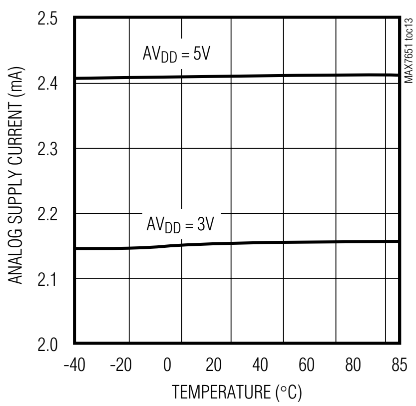
PWM OUTPUT LOW vs. SINK CURRENT



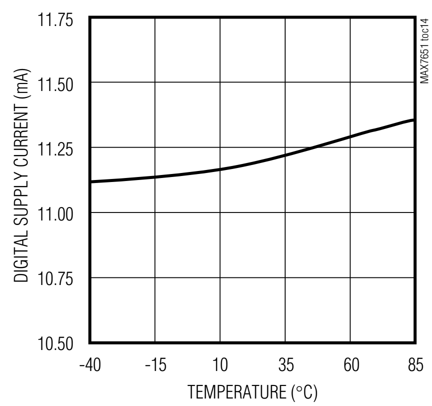
ANALOG SUPPLY CURRENT vs. INPUT VOLTAGE



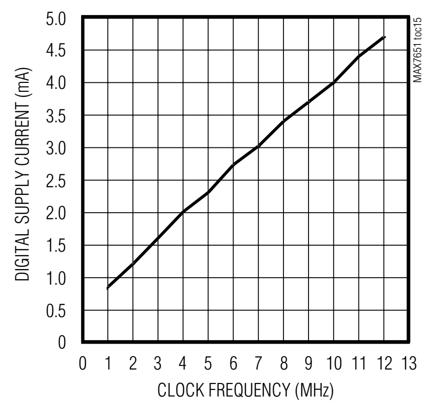
ANALOG SUPPLY CURRENT vs. TEMPERATURE



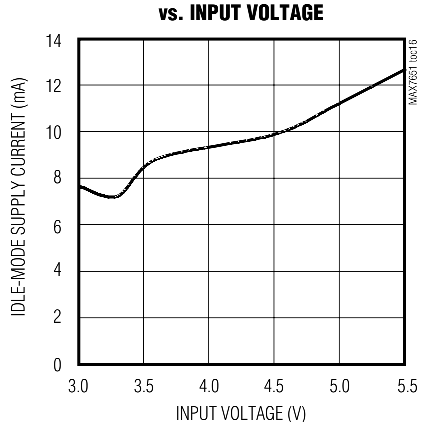
DIGITAL SUPPLY CURRENT vs.TEMPERATURE



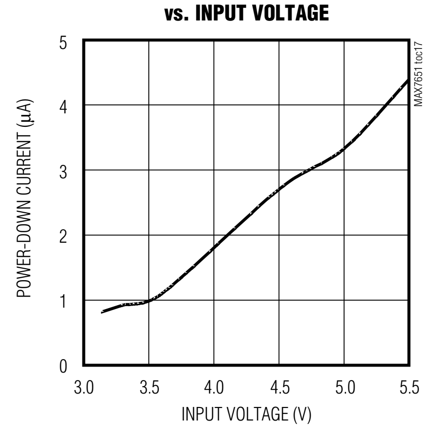
DIGITAL SUPPLY CURRENT vs. CLOCK FREQUENCY



IDLE-MODE SUPPLY CURRENT vs. INPUT VOLTAGE



POWER-DOWN CURRENT vs. INPUT VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	AIN0	Analog Input 0. Negative differential input relative to AIN1 or positive differential input relative to ACOM. (See Table 6)
2	AIN1	Analog Input 1. Positive differential input relative to AIN0 or positive differential input relative to ACOM. (See Table 6)
3	AIN2	Analog Input 2. Negative differential input relative to AIN3 or positive differential input relative to ACOM. (See Table 6)
4	AIN3	Analog Input 3. Positive differential input relative to AIN2 or positive differential input relative to ACOM. (See Table 6)
5	AIN4	Analog Input 4. Negative differential input relative to AIN5 or positive differential input relative to ACOM. (See Table 6)
6	AIN5	Analog Input 5. Positive differential input relative to AIN4 or positive differential input relative to ACOM. (See Table 6)
7	AIN6	Analog Input 6. Negative differential input relative to AIN7 or positive differential input relative to ACOM. (See Table 6)
8	AIN7	Analog Input 7. Positive differential input relative to AIN6 or positive differential input relative to ACOM. (See Table 6)
9	AV_{DD}	Positive Analog Supply Voltage. Analog power source for the A/D converter and other analog functions excluding the PWM D/A converter. Bypass with a 0.1µF in parallel with a 10µF low ESR capacitor to AGND.
10	AGND	Analog Ground. Connect PWMG to AGND.
11	REF+	High-Side Reference Input. High-side reference voltage for A/D conversions. Must be between AV_{DD} and AGND. Bypass to AGND with a 0.1µF in parallel with a 10µF low ESR capacitor to AGND.
12	REF-	Low-Side Reference Input. Low-side reference voltage for A/D conversions. Must be between AV_{DD} and AGND. If not connected to AGND bypass to AGND with a 0.1µF in parallel with a 10µF low ESR capacitor to AGND.
13	PWMV	Positive Analog Supply Voltage 2. Analog power source for the the PWM D/A converter outputs. Bypass with a 0.1µF in parallel with a 10µF low ESR capacitor to PWMG.
14	PWMG	Ground for PWM. Connect to AGND.
15	PWMA	PWM Output A. Output of PWM D/A Converter A. See *PWM Digital-to-Analog Conversions*.
16	PWMB	PWM Output B. Output of PWM D/A Converter B. See *PWM Digital-to-Analog Conversions*.
17	$\overline{\text{INT0}}$	External Interrupt 0 Input (active-low)
18	$\overline{\text{INT1}}$	External Interrupt 1 Input (active-low)
19	P3.7/$\overline{\text{RD}}$	P3.7: Bit 7 for General Purpose I/O Port 3 (most significant bit)
		$\overline{\text{RD}}$: Read Output. Read strobe for accessing external data memory (active-low)
20	P3.6/$\overline{\text{WR}}$	P3.6: Bit 6 for General Purpose I/O Port 3
		$\overline{\text{WR}}$: Write Output. Write strobe for writing to external data memory (active-low)
21	P3.5/T1	P3.5: Bit 5 for General Purpose I/O Port 3
		T1: Timer 1 External Input
22	P3.4/T0/ READY	P3.4: Bit 4 for General Purpose I/O Port 3
		T0: Timer 0 External Input
		READY: Ready State Output (external flash programming mode only)
23	P3.3	P3.3: Bit 3 for General Purpose I/O Port 3
24	P3.2	P3.2: Bit 2 for General Purpose I/O Port 3

Pin Description (continued)

PIN	NAME	FUNCTION
25	P3.1/ TXD0	P3.1: Bit 1 for General Purpose I/O Port 3
		TXD0: Transmit Serial Output for Serial Port
26	P3.0/ RXD0	P3.0: Bit 0 for General Purpose I/O Port 3 (least significant bit)
		RXD0: Receive Serial Input for Serial Port
27	DGND	Digital Ground. Connect DGND to AGND at the power source. Connect pins 27, 39, and 61 together.
28	DV_{DD}	Positive Digital Supply Voltage. Bypass with a 0.1µF in parallel with a 10µF low ESR capacitor to DGND. Connect pins 28, 40, and 62 together.
29	P2.0/A8	P2.0: Bit 0 for General Purpose I/O Port 2 (least significant bit)
		A8: Bit 8 for Internal Flash Memory Address
30	P2.1/A9	P2.1: Bit 1 for General Purpose I/O Port 2
		A9: Bit 9 for Internal Flash Memory Address
31	P2.2/A10	P2.2: Bit 2 for General Purpose I/O Port 2
		A10: Bit 10 for Internal Flash Memory Address
32	P2.3/A11	P2.3: Bit 3 for General Purpose I/O Port 2
		A11: Bit 11 for Internal Flash Memory Address
33	P2.4/A12	P2.4: Bit 4 for General Purpose I/O Port 2
		A12: Bit 12 for Internal Flash Memory Address
34	P2.5	P2.5: Bit 5 for General Purpose I/O Port 2
		Upper and Lower Internal Flash Memory Select (see Table 2)
35	P2.6	P2.6: Bit 6 for General Purpose I/O Port 2
		Flash Programming Mode Select (see Table 2)
36	P2.7	P2.7: Bit 7 for General Purpose I/O Port 2 (most significant bit)
		Flash Programming Mode Select (see Table 2)
37	$\overline{PSEN}$	Program Store Enable (active-low). Qualifies program read from external devices. To ensure flash data integrity during RST insertions, R_{LOAD} must be greater than or equal to 200kΩ.
38	ALE/ $\overline{PROG}$	ALE: Address Latch Enable. To ensure flash data integrity during RST insertions, R_{LOAD} must be greater than or equal to 200kΩ.
		$\overline{PROG}$: Flash Memory Program Pulse
39	DGND	Digital Ground. Connect pins 27, 39, and 61 together.
40	DV_{DD}	Positive Digital Supply Voltage. Bypass with a 0.1µF in parallel with a 10µF low ESR capacitor to DGND. Connect pins 28, 40 and 62 together.
41	P0.0/AD0	P0.0: Bit 0 for General Purpose I/O Port 0 (least significant bit)
		AD0: Bit 0 for Internal Flash Memory Data or External Memory I/O Data (least significant bit)
42	P0.1/AD1	P0.1: Bit 1 for General Purpose I/O Port 0
		AD1: Bit 1 for Internal Flash Memory Data or External Memory I/O Data
43	P0.2/AD2	P0.2: Bit 2 for General Purpose I/O Port 0
		AD2: Bit 2 for Internal Flash Memory Data or External Memory I/O Data
44	P0.3/AD3	P0.3: Bit 3 for General Purpose I/O Port 0
		AD3: Bit 3 for Internal Flash Memory Data or External Memory I/O Data
45	P0.4/AD4	P0.4: Bit 4 for General Purpose I/O Port 0
		AD4: Bit 4 for Internal Flash Memory Data or External Memory I/O Data

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Pin Description (continued)

PIN	NAME	FUNCTION
46	P0.5/ AD5	P0.5: Bit 5 for General Purpose I/O Port 0
		AD5: Bit 5 for Internal Flash Memory Data or external memory I/O
47	P0.6/ AD6	P0.6: Bit 6 for General Purpose I/O Port 0
		AD6: Bit 6 for Internal Flash Memory Data or external memory I/O
48	P0.7/ AD7	P0.7: Bit 7 for General Purpose I/O Port 0 (most significant bit)
		AD7: Bit 7 for Internal Flash Memory Data or external memory I/O
49	P1.0/T2/ T2OUT/ AD0	P1.0: Bit 0 for General Purpose I/O Port 1 (least significant bit)
		T2: Timer 2 External Input
		T2OUT: Timer 2 External Output
		AD0: Bit 0 for Internal Flash Memory Address
50	P1.1/ T2EX/ AD1	P1.1: Bit 1 for General Purpose I/O Port 1
		T2EX: Timer 2 External Capture/Reload Trigger
		AD1: Bit 1 for Internal Flash Memory Address
51	P1.2/ RXD1/ AD2	P1.2: Bit 2 for General Purpose I/O Port 1
		RXD1: Receive Serial Input for UART 1
		AD2: Bit 2 for Internal Flash memory Address
52	P1.3/ TXD1/ AD3	P1.3: Bit 3 for General Purpose I/O Port 1
		TXD1: Transmit Serial Input for UART 1
		AD3: Bit 3 for Internal Flash Memory Address
53	P1.4/ AD4	P1.4: Bit 4 for General Purpose I/O Port 1
		AD4: Bit 4 for Internal Flash Memory Address
54	P1.5/ AD5	P1.5: Bit 5 for General Purpose I/O Port 1
		AD5: Bit 5 for Internal Flash Memory Address
55	P1.6/ AD6	P1.6: Bit 6 for General Purpose I/O Port 1
		AD6: Bit 6 for Internal Flash Memory Address
56	P1.7/ AD7	P1.7: Bit 7 for General Purpose I/O Port 1
		AD7: Bit 7 for Internal Flash Memory Address
57	$\overline{EA}$/V_{PP}	$\overline{EA}$: Connect to DGND to use external ROM. Connect $\overline{EA}$ to DV_{DD} for internal flash memory.
		V_{PP}: Flash Programming Voltage (external flash programming mode only)
58	RST	Active High Reset. Connected to an internal 130kΩ pulldown resistor. Connect a 2.2µF (typ) capacitor from DV_{DD} to RST.
59	XTAL2	Clock Output. Connect a crystal across XTAL1 and XTAL2. The on-chip clock signal is not available at XTAL2. Leave XTAL2 unconnected when XTAL1 is driven with an external clock.
60	XTAL1	Clock Input. Connect a crystal across XTAL1 and XTAL2. Alternatively, drive XTAL1 with a CMOS-compatible clock and leave XTAL2 unconnected.
61	DGND	Digital Ground. Connect pins 27, 39, and 61 together.
62	DV_{DD}	Positive Digital Supply Voltage. Bypass with a 0.1µF in parallel with a 10µF low ESR capacitor to DGND. Connect pins 28, 40 and 62 together.
63	TEST	Test Point. Must be connected to DGND.
64	ACOM	Analog Common Input. Negative differential input relative to AIN_ for single-ended measurements (see Table 6). Connect to $AV_{DD}/2$ for maximum input range.

Detailed Description

MAX7651/MAX7652 Architecture

The MAX7651/MAX7652 are complete 12-bit data-acquisition systems featuring an algorithmic, switched-capacitor, analog-to-digital converter (ADC), dual pulse-width-modulated digital-to-analog converter (DAC), and an industry-standard 8051 microprocessor core with a variety of I/O and timing peripherals.

Using an external oscillator with an operating frequency between 1MHz and 12MHz, the MAX7651/MAX7652 execute the majority of its commands in only four clock periods to yield an average speed improvement of 2.5 times over typical 8051 microprocessors requiring 12 clock periods instructions. See the MAX7651/MAX7652 *Programmer's Reference Manual* for further details.

On-chip peripherals include four 8-bit parallel ports, two serial ports, three general-purpose timers, and a watchdog timer. The MAX7651/MAX7652 also feature 16kB in two banks of 8kB flash memory and 256 bytes of high-speed random access memory.

Memory Organization

The MAX7651/MAX7652 support up to 64kB of external program (read-only) memory and data (random-access) memory in conformance with the 8051 industry standard.

Figure 4 shows the program memory organization. When $\overline{EA}$ is high, the CPU has access to two internal 8kB blocks of flash memory beginning at addresses 0000H (lower block) and 2000H (upper block). Addresses 0000H–0002H and 0003H–006AH of the lower block are reserved for the CPU reset vector and a set of interrupt vectors, respectively (see Table 3). Addresses 3FC0H–3FFFH of the upper block are also reserved and cannot be accessed by the CPU. Addresses 4000H–FFFFH are for external ROM. When $\overline{EA}$ is low, the external ROM must be used for all program addresses (0000H–FFFFH).

Figure 5 shows the data memory (RAM) organization. The first 256 bytes are partitioned between two internal 128-byte blocks. The lower block (addresses 0000H–007FH) is used for registers or scratchpad memory and can be accessed either directly or indirectly (see the MAX7651/MAX7652 *Programmer's Reference Manual*). The upper block (addresses 0080H–00FFH) reflects a set of special function registers (SFRs) when accessed directly, and separate scratchpad memory when accessed indirectly. Addresses 0100H–FFFFH are reserved for external RAM.

Table 4 shows the SFR mapping to memory and Table 5 shows the SFR contents on power-up or reset. Unshaded register designations are consistent with the industry standard 8051. Shaded register designations

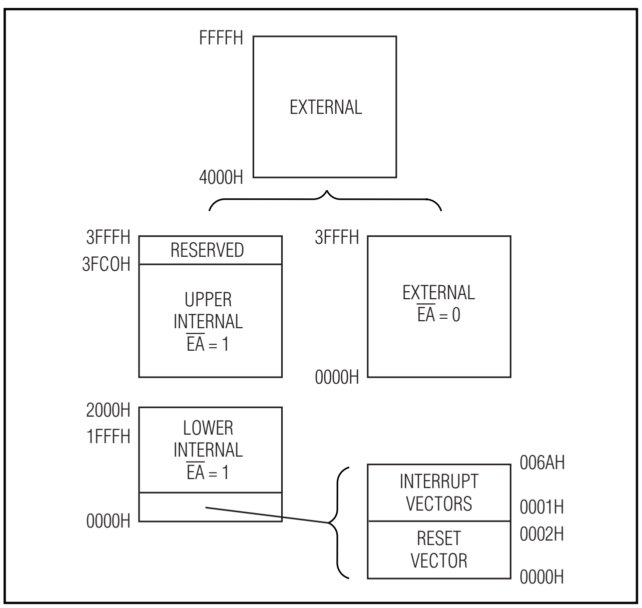

Figure 4. Program Memory Organization

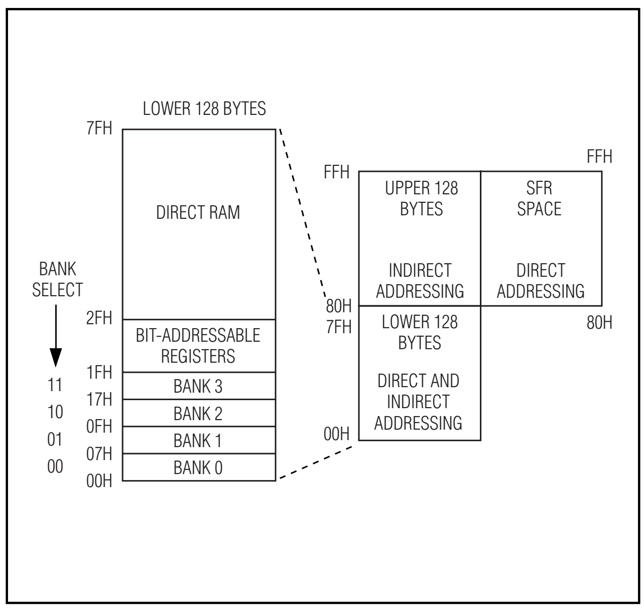

Figure 5. Data Memory (RAM) Organization

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Table 3. Reset and Interrupt Vector Locations

ADDRESS RANGE	FUNCTION	NATURAL PRIORITY*
0000H–0002H	Reset Vector	0
INTERRUPT VECTORS		
0003H–000AH	$\overline{\text{INT0}}$ (external interrupt 0)	1
000BH–0012H	Timer 0	2
0013H–001AH	$\overline{\text{INT1}}$ (external interrupt 1)	3
001BH–0022H	Timer 1	4
0023H–002AH	Serial Port 0 transmit/receive	5
002BH–0032H	Timer 2	6
0033H–003AH	Reserved	—
003BH–0042H	Serial Port 1 transmit/receive	7
0043H–004AH	Flash memory write/page erase	8
004BH–0052H	ADC (end of conversion)	9
0053H–005AH	Reserved	10
005BH–0062H	Reserved	11
0063H–006AH	Watchdog timer	12

**Lower priority number takes precedence.*

Table 4. SFR Memory Organization

HEX ADDRESS	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
F8	EIP						PWMC	
F0	B							
E8	EIE		EEAL	EEAH	EEDAT	EESTCMD		
E0	ACC							
D8	EICON		PWPS	PWDA	PWDB	WDT		
D0	PSW							
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2		
C0	SCON1	SBUF1	ADDAT0	ADDAT1	Reserved	ADCON		
B8	IP		Reserved	Reserved				
B0	P3		VERSION	Reserved	Reserved			
A8	IE							
A0	P2							
98	SCON0	SBUF0						
90	P1	EXIF						
88	TCON	TMOD	TL0	TH0	TL1	TH1	CKCON	Reserved
80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

Note 1: SFRs in column 0/8 are bit addressable. Other SFRs are not bit addressable.
Note 2: The VERSION SFR contains the silicon ID and will change for future MAX7651/MAX7652 revisions.

Table 5. SFR Contents on Power-Up or Reset

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80	1	1	1	1	1	1	1	1
SP	81	0	0	0	0	0	1	1	1
DPL0	82	0	0	0	0	0	0	0	0
DPH0	83	0	0	0	0	0	0	0	0
DPL1	84	0	0	0	0	0	0	0	0
DPH1	85	0	0	0	0	0	0	0	0
DPS	86	0	0	0	0	0	0	0	0
PCON	87	0	0	1	1	0	0	0	0
TCON	88	0	0	0	0	0	0	0	0
TMOD	89	0	0	0	0	0	0	0	0
TL0	8A	0	0	0	0	0	0	0	0
TH0	8B	0	0	0	0	0	0	0	0
TL1	8C	0	0	0	0	0	0	0	0
TH1	8D	0	0	0	0	0	0	0	0
CKCON	8E								
P1	90	0	0	0	0	0	0	0	0
EXIF	91	0	0	0	0	1	0	0	0
SCON0	98	0	0	0	0	0	0	0	0
SBUF0	99	0	0	0	0	0	0	0	0
P2	A0	1	1	1	1	1	1	1	1
IE	A8	0	0	0	0	0	0	0	0
P3	B0	1	1	1	1	1	1	1	1
IP	B8	1	0	0	0	0	0	0	0
SCON1	C0	0	0	0	0	0	0	0	0
SBUF1	C1	0	0	0	0	0	0	0	0
ADDAT0	C2	0	0	0	0	0	0	0	0
ADDAT1	C3	0	0	0	0	0	0	0	0
ADCON	C5	0	0	0	0	0	0	0	0
T2CON	C8	0	0	0	0	0	0	0	0
RCAP2L	CA	0	0	0	0	0	0	0	0
RCAP2H	CB	0	0	0	0	0	0	0	0
TL2	CC	0	0	0	0	0	0	0	0
TH2	CD	0	0	0	0	0	0	0	0
PSW	D0	0	0	0	0	0	0	0	0
EICON	D8	0	1	0	0	0	0	0	0
PWPS	DA	0	0	0	0	0	0	0	0
PWDTA	DB	0	0	0	0	0	0	0	0
PWDTB	DC	0	0	0	0	0	0	0	0
WDT	DD	0	0	0	0	0	0	0	0

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Table 5. SFR Contents on Power-Up or Reset (continued)

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ACC	E0	0	0	0	0	0	0	0	0
EIE	E8	1	1	1	0	0	0	0	0
EEAL	EA	0	0	0	0	0	0	0	0
EEAH	EB	0	0	0	0	0	0	0	0
EEDAT	EC	0	0	0	0	0	0	0	0
EESTCMD	ED	0	0	0	0	0	0	0	0
B	F0	0	0	0	0	0	0	0	0
EIP	F8	1	1	1	0	0	0	0	0
PWMC	FE	0	0	0	0	0	0	0	0

are unique to the MAX7651/MAX7652. Subsequent sections of this data sheet explain the SFR functions.

RESERVED SFR addresses are used for MAX7651/MAX7652 testing and should not be accessed by user software. Undesignated SFR addresses are not implemented and will return indefinite data when read.

Special Function Registers for Microprocessor Operations and Control

Accumulator SFR

The Accumulator SFR is used for arithmetic operations including addition, subtraction, multiplication, division, and Boolean bit manipulation. Accumulator specific instructions designate the accumulator as “A”.

B SFR

The B SFR is used for multiply and divide operations. It is otherwise available as a scratchpad register.

Program Status Word SFR

The PSW or Program Status Word SFR contains bits that indicate the state of the microprocessor CPU. Table 6 shows the individual bit functions.

Stack Pointer SFR

The SP or Stack Pointer SFR contains the “top-of-the-stack” address in internal RAM. This address increments before data is stored during PUSH and CALL executions. The default value is 07H after reset, so that the stack begins at 08H.

Dual Data Pointer SFRs

The MAX7651/MAX7652 feature dual data pointers to enhance execution times when moving large blocks of data. All DPTR-related instructions use 16 bits contained at SFR pairs DPH0 and DPL0 or DPH1 and DPL1 to address external data RAM or peripherals. Bit 0 (SEL) within the DPS SFR determines the data pointer. No other bits have significance in this register. When SEL= 0, DPTR instructions use DPH0 and DPL0, when SEL=1, DPTR instructions use DPH1 and DPL1. Program code developed for 8051 platforms that use a single data pointer (DPH0 and DPL0) requires no modification if SEL = 0 (the default value).

Power Control SFR

The PCON Power Control SFR provides software control over the power modes. In both IDLE and STOP modes, CPU processing is suspended and internal registers maintain their current data. The STOP mode additionally disables the internal clock and analog circuitry. Any enabled CPU interrupt can be used to terminate the IDLE mode. A reset is necessary to terminate the STOP mode and is sufficient to terminate the IDLE mode. Table 7 shows the PCON SFR format.

Instruction Set

The MAX7651/MAX7652 instruction set is compatible with the 8051 industry standard. See the MAX7651/ MAX7652 *Programmer's Reference Manual* for a complete listing.

Analog-to-Digital Converter

ADC Operation

Figure 6 shows a simplified model of the converter input structure and the associated switch timing. Once initiated, a voltage conversion requires 224 periods of the external master clock. Capacitor C_{HOLD} charges to the difference between inputs AIN+ and AIN- during eight clock periods of acquisition time that begin on the rising edge of clock cycle 13. This charge sample is subsequently transferred to the ADC (through the action of SW5) during eight clock periods that begin on the rising edge of clock cycle 21. The ADC asserts a conversion complete flag on the rising-edge of clock cycle 225 (see *ADC Special Function Registers*).

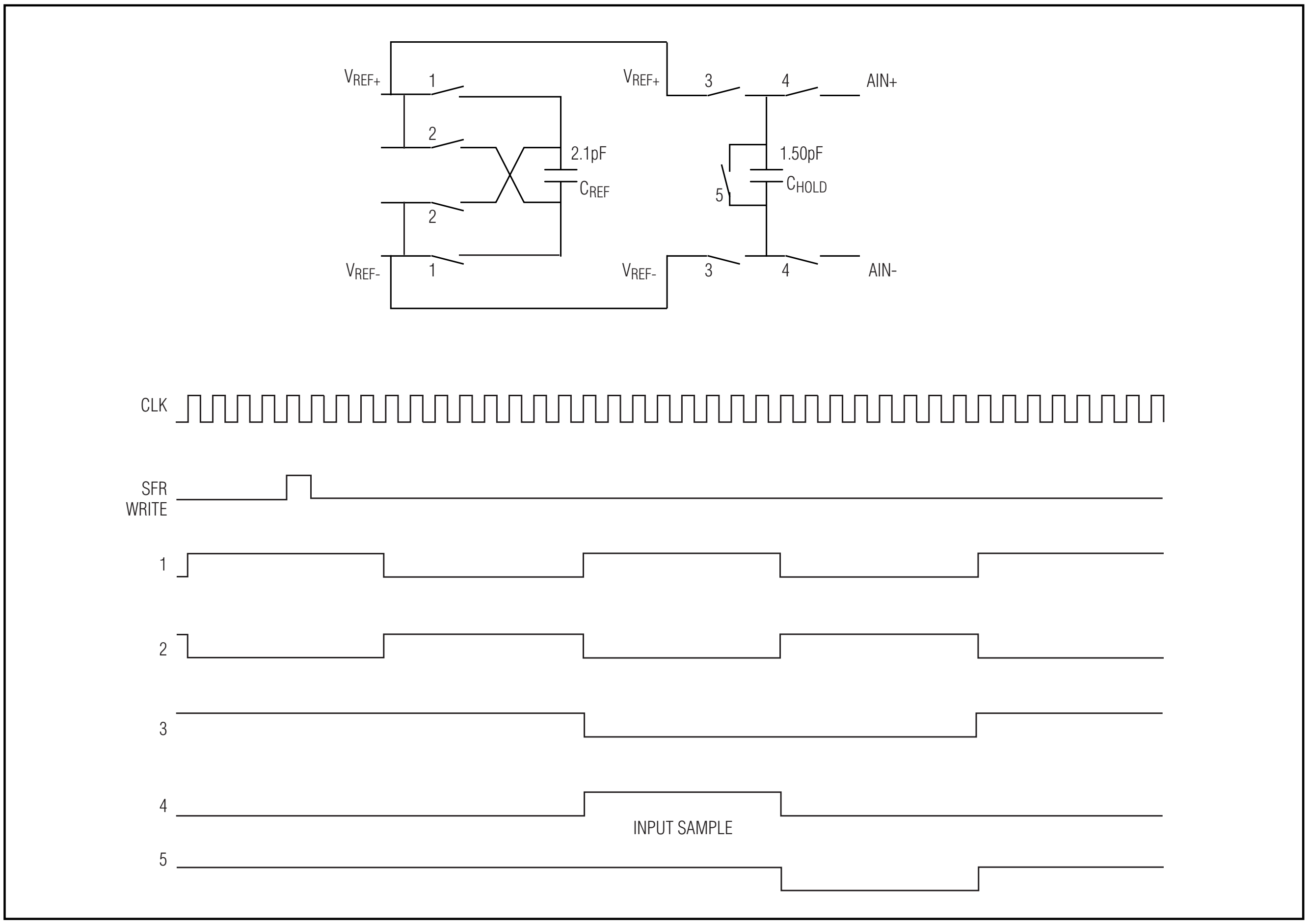

Figure 6. ADC Input Structure and Switch Timing

Since the acquisition time is limited to eight clock periods, the acquired voltage at C_{HOLD} can have significant error if the analog input source impedance (R_S) is large. Limit the worst-case error to 1/2 LSB by ensuring,

$$R_S < 0.9\ t_{CLK} / C_{HOLD}$$

where t_{CLK} is the clock period. Smaller R_S values may be necessary if an antialiasing filter is used.

The ADC continuously samples the positive and negative difference between the two external reference voltages REF+ and REF- by reconfiguring capacitor C_{REF} over alternate eight clock-period intervals. Switch pairs 1 and 2 are forced off and on, respectively, on the rising edge of clock cycle five to ensure synchronization with conversions. Capacitor C_{HOLD} also charges to the difference between REF+ and REF- on the rising edge of clock cycle 29 and remains charged until the next conversion. Nevertheless, continuous C_{REF} charging requirements dominate loading at the REF+ and REF- inputs.

Analog Inputs

The MAX7651/MAX7652 operate in either single-ended or differential mode. In single-ended mode, one of eight input channels (AIN0–AIN7) is assigned to AIN+, and ACOM is assigned to AIN- (see Figure 6). In differential mode, the eight input channels are assigned to AIN+ and AIN- with four distinct pairings. Table 6 shows the input assignments for different values of bits M3, M2, M1, and M0 in the A/D Control SFR (see *ADC Special Function Registers*).

Analog Input Protection

Internal protection diodes clamp the analog inputs to AV_{DD} and AGND, so channels can swing within AGND -

0.3V and AV_{DD} + 0.3V without damage. For accurate conversions the inputs should not extend beyond the supply rails.

Transfer Function

Figure 7 shows the bipolar two's complement ADC transfer function. The single-ended conversion range extends from $-V_{REF}/2$ to $+V_{REF}/2$, where $V_{REF} = V_{REF+} - V_{REF-}$. The differential conversion range extends from $-V_{REF}$ to $+V_{REF}$. Each LSB in the single-ended and differential mode reflects voltage increments of $V_{REF}/4096$ and $2V_{REF}/4096$, respectively.

ADC Special Function Registers

The ADCON or A/D Control SFR establishes ADC operating conditions and input configurations. Table 7 shows the individual bit functions. A "write" to ADCON initiates the A/D conversion process.

Table 6. Program Status Word (PSW) Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
CY	AC	F0	RS1	RS0	OV	F1	P

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>7</td><td>CY</td><td colspan="3">Carry Flag. Set to "1", following an additional operation that results in a carry or a subtraction operation that results in a borrow. Otherwise cleared to 0.</td></tr>
<tr><td>6</td><td>AC</td><td colspan="3">Auxiliary Carry Flag. Similar to CY, but used for BCD operations.</td></tr>
<tr><td>5</td><td>F0</td><td colspan="3">User Flag 0. General-purpose flag for software control.</td></tr>
<tr><td rowspan="6">4,3</td><td rowspan="6">RS1,
RS0</td><td colspan="3">Register Select Bits. These select one of four banks of eight registers that occupy the first 32 addresses in the lower internal RAM.</td></tr>
<tr><th>RS1</th><th>RS0</th><th>SELECTED REGISTER BANK</th></tr>
<tr><td>0</td><td>0</td><td>Register bank 0, addresses 00H–07H</td></tr>
<tr><td>0</td><td>1</td><td>Register bank 1, addresses 08H–0FH</td></tr>
<tr><td>1</td><td>0</td><td>Register bank 2, addresses 10H–17H</td></tr>
<tr><td>1</td><td>1</td><td>Register bank 3, addresses 18H–1FH</td></tr>
<tr><td>2</td><td>OV</td><td colspan="3">Overflow Flag. Set to "1", for any arithmetic operation that yields an overflow. Otherwise cleared to zero.</td></tr>
<tr><td>1</td><td>F1</td><td colspan="3">User Flag 1. General-purpose flag for software control.</td></tr>
<tr><td>0</td><td>P</td><td colspan="3">Parity flag. Set to "1", when the module 2 sum of the accumulator bits is one (odd number of 1's), otherwise clear to zero (even number of 1's).</td></tr>
</table>

Table 7. Power Control (PCON) Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
SMOD0	—	—	—	GF1	GF0	STOP	IDLE

BIT	NAME	DESCRIPTION
7	SMOD0	Serial Port 0 Baud-Rate Doubler Enable. SMOD0 = 1, doubles the baud rate.
6,5,4	—	Reserved
3	GF1	General Flag 1. General-purpose flag for software control.
2	GF0	General Flag 0. General-purpose flag for software control.
1	STOP	STOP Mode Select. STOP = 1 stops the crystal oscillator and powers down the analog circuitry.
0	IDLE	IDLE Mode Select. IDLE = 1 results in suspension of CPU processing.

External Reference

The MAX7651/MAX7652 require external reference voltages at V_{REF+} and V_{REF-}. A single reference voltage can be used at V_{REF+}, when V_{REF-} is connected to AGND. The positive reference voltages must be no greater than the analog supply voltage AV_{DD} and capable of supplying 30µA. Bypass each reference voltage to AGND with a 0.1µF capacitor in parallel with a 10µF low ESR capacitor.

PWM Digital-to-Analog Converters (DACs)

The MAX7651/MAX7652 provide two pulse-width modulated (PWM) DACs for applications that do not require high conversion accuracy. Figure 8 shows the pulse-width-modulator block diagram. The clock signal is divided by 2 (x + 1), where x is the content of the Pulse-Width Prescaler (PWPS) SFR register. This reduced frequency signal is used to drive a modulo-255 counter. When the counter value exceeds the value stored in SFRs PWDA (Output A) or PWDB

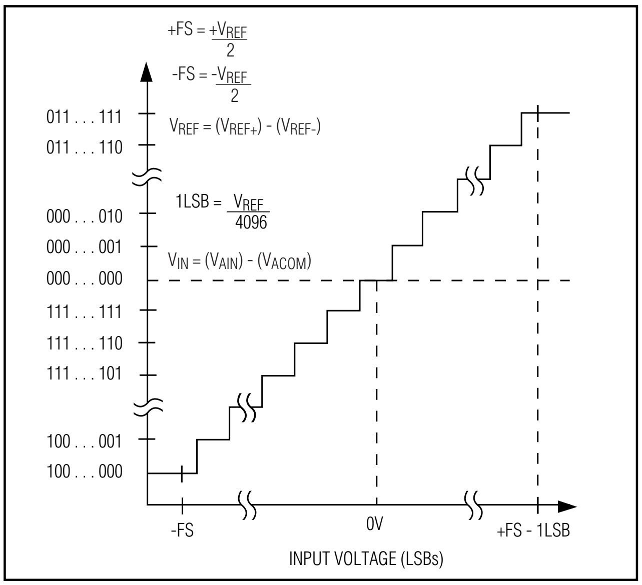

Figure 7a. Single-Ended Mode Transfer Function

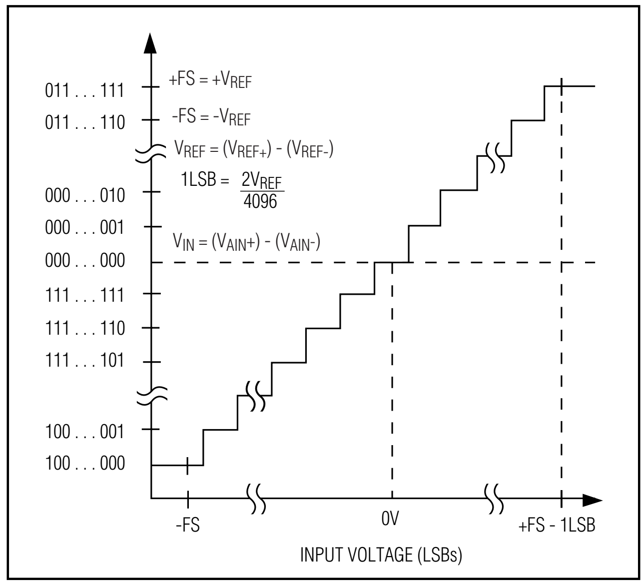

Figure 7b. Differential Mode Transfer Function

Table 8. Analog Input Selection

MD3	MD2	MD1	MD0	MODE	AIN+	AIN-
0	0	0	0	Single-ended	AIN0	ACOM
0	0	0	1	Single-ended	AIN1	ACOM
0	0	1	0	Single-ended	AIN2	ACOM
0	0	1	1	Single-ended	AIN3	ACOM
0	1	0	0	Single-ended	AIN4	ACOM
0	1	0	1	Single-ended	AIN5	ACOM
0	1	1	0	Single-ended	AIN6	ACOM
0	1	1	1	Single-ended	AIN7	ACOM
1	0	0	0	Differential	AIN1	AIN0
1	0	0	1	Differential	AIN3	AIN2
1	0	1	0	Differential	AIN5	AIN4
1	0	1	1	Differential	AIN7	AIN6
1	1	0	0	—	REF+	REF-

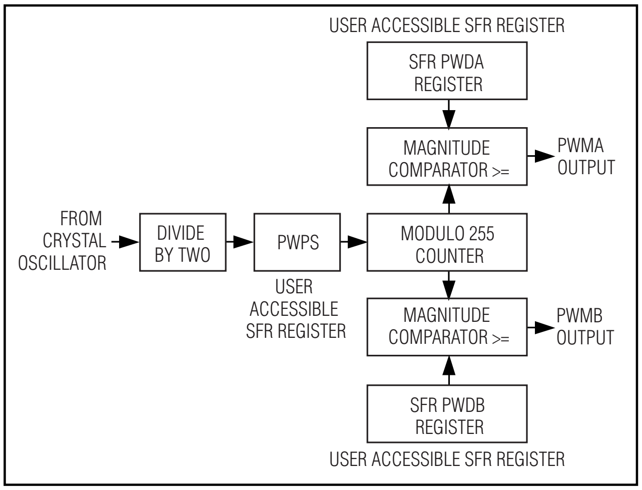

Figure 8. PWM Block Diagram

(Output B), the corresponding output transitions from low to high (Figure 9).

Writing 00H to PWDA or PWDB, yields a waveform with 100% duty cycle (High), and writing FFH to PWDA or PWDB yields a waveform with 0% duty cycle (Low). Writing an intermediate register value y, yields a waveform with duty cycle (1 - y / 255) × 100%. Tables 10, 11, and 12 show the formats of the PWPS, PWDA, and PWDB SFR's.

External low-pass filters are needed to obtain DC voltages between 0 and DV_{DD} from the PWM outputs. Simple RC filters are preferred. Choose R >2kΩ to avoid excessive loading, and choose C <0.1µF to avoid large transient currents that reflect the PWM switching action. Each filtered PWM output can source or sink up to 2mA. Do not exceed this specification. If larger output capability is required, provide an appropriate buffer such as a unity-gain op amp. PWM circuitry and PWM Outputs A and B are enabled with the Pulse-Width Modulator Control (PWMC) SFR. Table 13 shows the PWMC SFR format.

Watchdog Timer

The MAX7651/MAX7652 features a watchdog timer that resolves irregular software control. The watchdog timer resets the microprocessor if software fails to reset the timer within one of four pre-selected time intervals. The timer generates an optional interrupt after 2^{16}, 2^{19}, 2^{22}, or 2^{25} clock periods of the external oscillator. It generates the reset signal after an additional 512 clock periods. Table 14 indicates specific interrupt and reset times that apply for a 12MHz clock frequency.

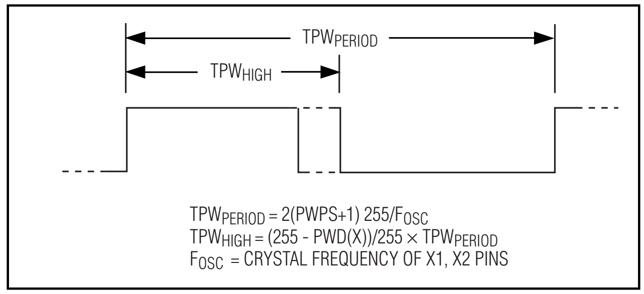

Figure 9. PWM Output Waveform

Five watchdog-related control bits and two status flags are located in different special function registers. Table 15 shows the particular functions and SFR locations.

8051-Compatible Peripherals

Parallel I/O Ports

Like other 8051-based systems, the MAX7651/MAX7652 features four 8-bit parallel ports that support general input and output, address and data lines, and various special functions. Each bidirectional port has a latch register (SFRs P0, P1, P2, and P3), an input buffer, and an output driver.

Port P0 is open-drain. Writing a logic level 1 to a P0 pin establishes a high-impedance input. When used as a general-purpose output, a P0 pin requires an external pull-up resistor to validate a logic level 1. When used as an address/data output, a P0 pin features an internal active high driver. Port 0 is a bidirectional Flash data I/O port during Flash programming and verification.

Port 1: Port 1 is a bidirectional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups and can serve as inputs. Port 1 receives low-order address bytes during Flash programming and verification.

Port 2: Port 2 is a bidirectional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups and can serve as inputs. Port 2 also serves as the high-order address and data bus (for 16-bit operations) during accesses to external memory, using strong internal pullups when emitting 1's.

Port 3: Port 3 is a bidirectional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups and can serve as inputs.

The P1 and P3 ports support the special functions listed in Table 16. Write a "1" to the corresponding bit in the port register to enable the alternative function.

Table 9. A/D Control (ADCON) Format—SFR Address C5H

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
CC	CCVT	CCIE	OVRN	M3	M2	M1	M0

BIT	NAME	DESCRIPTION
7	CC	Conversion Complete Flag (Read Only). The MAX7651/MAX7652 set this flag to 1 following a conversion to indicate valid data in the ADDAT1 and ADDAT0 data SFRs (see below). The CC bit is cleared to 0 when ADDAT1 is read by the CPU.
6	CCVT	Continuous Conversion Enable (Read/Write). When CCVT = 1, the ADC performs continuous conversions at the rate of 224 clock cycles/conversion. Conversions continue until the MAX7651/MAX7652 is reset or until CCVT is cleared, in which case conversions stops after the current conversion ends.
5	CCIE	Conversion Complete Interrupt Enable (Read/Write). When CCIE = 1, interrupt 3 is generated at the end of each conversion.
4	OVRN	Overrun Flag (Read Only). The MAX7651/MAX7652 set this flag to 1 whenever a conversion completes while CC is set. The previous conversion result is overwritten. The OVRN bit is cleared to 0 when ADDAT1 is read by the CPU.
3–0	M3–M0	Analog Input Multiplexer Select Bits. Used to establish input configurations for single-ended or differential conversions (see Table 6).

***Note:** SFRs ADDAT1 and ADDAT0 contain the results of individual A/D conversions with the formats shown in Tables 8 and 9. A read to ADDAT1 clears the CC and OVRN flags in ADCON.*

Table 10. A/D Data-1 (ADDAT1) Format—SFR Address C3H

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
SIGN BIT	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4

Table 11. A/D Data-0 (ADDAT0) Format—SFR Address C2H

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
BIT 3	BIT 2	BIT 1	BIT 0	0	0	0	0

Table 12. Pulse-Width Prescaler (PWPS) Format—SFR address DAH

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PWPS7	PWPS6	PWPS5	PWPS4	PWPS3	PWPS2	PWPS1	PWPS0

Table 13. Pulse-Width Data A (PWDA) Format—SFR address DBH

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PWDA7	PWDA6	PWDA5	PWDA4	PWDA3	PWDA2	PWDA1	PWDA0

Table 14. Pulse-Width Data B (PWDB) Format—SFR address DCH

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PWDB7	PWDB6	PWDB5	PWDB4	PWDB3	PWDB2	PWDB1	PWDB0

Table 15. Pulse-Width-Modulator Control (PWMC) Format—SFR Address FEH

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PWON	—	—	—	—	—	PWENA	PWENB

BIT	NAME	DESCRIPTION
7	PWON	Pulse-Width-Modulator Enable. Set PWON to 1 to enable the divide-by-two, PWPS prescaler, and modulo-255 counter circuit functions.
6–2	—	Not used
1	PWENA	PWM Output A Enable. Set to 1 to enable PWM output A.
0	PWENB	PWM Output B Enable. Set to 1 to enable PWM output B.

Table 16. Watchdog Interrupt and Reset Times (f_{CK} = 12MHz)

WD1	WD0	INTERRUPT TIMOUT	TIME (ms)	RESET TIMOUT	TIME (ms)
0	0	2^{16} clocks	5.461	2^{16} + 512 clocks	5.474
0	1	2^{19} clocks	43.691	2^{19} + 512 clocks	43.734
1	0	2^{22} clocks	349.525	2^{22} + 512 clocks	349.567
1	1	2^{25} clocks	2796.000	2^{25} + 512 clocks	2796.042

Serial Interface Ports

The MAX7651/MAX7652 each have two serial interfaces that operate according to the 8051 industry standard. Serial Port 0 uses SFRs SCON0 and SBUF0 for control and buffer functions. Serial Port 1 uses SFRs SCON1 and SBUF1 with identical bit functionality. See the MAX7651/MAX7652 *Programmer's Reference Manual* for details concerning serial-port data operations and timing information.

Timers/Counters

The MAX7651/MAX7652 have three timer/counters that function in several different modes for applications such as UART baud-rate control. All three timer/counters operate according to the 8051 industry standard. Specifically, the control (TCON), mode (TMOD), timer-0 parameter (TL0, TH0), Timer1 parameter (TL1, TH1), and Timer-2 parameter (TL2, TH2, RCAP2L, RCAP2H) SFRs have conventional formats. See the MAX7651/MAX7652 *Programmer's Reference Manual* for information concerning timer/counter applications.

Crystal Oscillator

The MAX7651/MAX7652 each have a single-stage inverter (Input at XTAL1, Output at XTAL2) that supports a crystal controlled oscillator. The crystal oscillator frequency should be between 1 and 12 MHz.

Note: External flash memory programming requires a minimum crystal oscillator frequency of 4MHz.

Crystal Specification:

Rs(typ)	25–40Ω
Rs(max)	150Ω
Load Capacitance	10–15pF
Oscillation Mode	Fundamental
Frequency	12,000MHz (max)
Tolerance	±0.01%
Holder Capacitance	3pF
Motional Inductance (typ)	50mH
Motional capacitance (typ)	0.0035pF

An external oscillator can also be used to clock the MAX7651/MAX7652 at frequencies between 1 and 12MHz, provided that the duty cycle is between 40% and 60%. When using an external clock source connect the clock to XTAL1, with XTAL2 unconnected.

Applications Information

Performing a Conversion

An example of a conversion with the MAX7651/MAX7652 is as follows:

- Write to the ADCON SFR, setting bit CCIE to 1, and bits M3–M0 to appropriate values for the desired differential or single-ended analog input configuration (Tables 6 and 7).
- Wait 224 clock cycles to receive Interrupt 3 as an indication that the A/D conversion is complete.
- Read the conversion data in SFRs ADDAT0 and ADDAT1 as described in Tables 8 and 9.

Using FLASH Memory

The upper and lower 8kB blocks of internal Flash memory are each organized as 128 64-byte pages. Read, write, and page-erase operations cannot be applied to either block while executing program commands from the other block.

Note: Standard MOVC operations are supported.

FLASH Memory Special Function Registers

Tables 17 and 18 show the formats for the EEAH and EEAL SFRs. The EEAH register specifies the applicable Flash memory block (high or low) and the page address within that block. The EEAL register specifies the byte address within the specified page.

Table 19 shows the format for the Flash memory data (EEDAT) SFR that is used for 8-bit read and write transfers from and to a specified address.

Table 20 shows the format for the Flash memory status and command (EESTCMD) SFR. Bits RDYHI and RDYLO are cleared to zero when a read, write, or page-erase operation is applied to the high or low flash memory block. These bits are set to one once the flash

Table 17. Watchdog Timer Control and Status Bits

NAME	SFR	BIT	DESCRIPTION
WDIF	EICON	3	Watchdog Interrupt Flag. WDIF is set to 1 after completion of the interrupt timeout period (see Table 14). WDIF must be cleared by software before exiting interrupt service routine. Otherwise interrupt reoccurs upon exiting. WDIF is automatically cleared by either an external RST assertion or a WDT-generated reset.
WTRF	WDT	2	Watchdog Reset Flag. The WTRF bit is a status/control bit indicating that the Watchdog counter has counted an additional 512 clocks past the WDT interrupt and has generated a processor RESET. The 8051's "reset" routine should check the WTRF flag to determine the source of the reset. Additionally, if the WTRF flag has been set the Watchdog Timer counts will be reset when a zero is written to the WTRF flag. This allows the processor to regain synchronization with the WDT after a WDT reset has occurred. WTRF is also cleared when a zero is written to it.
EWT	EICON	1	Enable Watchdog Timer. Set to 1 to enable the watchdog timer. An assertion at the external RST pin automatically clears EWT. If EWT is cleared after being set. The watchdog timer count will suspend until EWT is set to 1 again.
RWT	EICON	0	Reset Watchdog Timer. Writing a "1" to the RWT bit will reset the watchdog counter ONLY if the end of the count has been reached (WDIF = 1) and the 512 clock window has not expired (WTRF = 0). ***Writing to RWT before the timeout period will not reset the watchdog timer***.
WD1	CKCON	7	Watchdog Control Bit 1. Controls the watchdog interrupt timeout (see Table 14).
WD0	CKCON	6	Watchdog Control Bit 0. Controls the watchdog interrupt timeout (see Table 14).
EWDI	EIE	4	Enable Watchdog Interrupt. An interrupt will be generated after the interrupt timeout period when EWDI = 1. Either a WDT-generated reset or an assertion at the external RST pin automatically clears EWDI.

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Table 18. Alternate Port Functions

PORT PIN	ALTERNATIVE FUNCTION	DESCRIPTION
P1.3	TXD1	Transmit Serial Output for Serial Port
P1.2	RXD1	Receive Serial Input for Serial Sort
P1.1	T2EX	Timer 2 External Capture/Reload Trigger
P1.0	T2/T2_OUT	Timer 2 External Input/Output
P3.7	$\overline{RD}$	Read Output
P3.6	$\overline{WR}$	Write Output
P3.5	T1	Timer 1 External Input
P3.4	T0/READY	Timer 0 External Input/Ready State Output (External Flash Programming mode only)
P3.1	TXD0	Transmit Serial Output for UART 0
P3.0	RXD0	Receive Serial Input for UART 0

Table 19. Flash Address High (EEAH) Format—SFR Address EBH

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
BLOCK	EEAH6	EEAH5	EEAH4	EEAH3	EEAH2	EEAH1	EEAH0

BIT	NAME	DESCRIPTION
7	BLOCK	Flash Memory Block. Set BLOCK = 1 to access the high Flash memory block. Set BLOCK = 0 to access the low Flash memory block.
6 - 0	EEAH_	Page Address. Determines the Flash memory page. EEAH6 is the MSB.

Table 20. Flash Address Low (EEAL) Format—SFR Address EAH

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
—	—	EEAL5	EEAL4	EEAL3	EEAL2	EEAL1	EEAL0

BIT	NAME	DESCRIPTION
7,6	—	Not used.
5 - 0	EEAL_	Byte within Page Address Bit. Determines the byte address within a Flash memory page. EEAL5 is the MSB.

memory operation is complete. **Never attempt to execute a flash memory command when either RDYHI or RDYLO are 0 (command action in progress).**

Flash Memory Read

To read Flash memory, load the address into SFRs EEAH and EEAL. Then write AAH to EESTCMD. The results of the read operation will be available in SFR EEDAT in the next CPU instruction cycle.

Flash Memory Write

Erase operations set all bits to “1”. After a byte has been programmed it must be erased before it is re-written. To write to Flash memory, load the address into SFRs EEAH and EEAL, and load the data into EEDAT. Then write 55H to EESTCMD. The execution time for flash memory write is 63µs (typ) and is independent of the CPU clock.

Note: Do not write to the same location more than twice before the next page/mass erase operation.

Flash Memory Page Erase

The page erase operation sets all bits within the page to “1”s. To erase a page from Flash memory, load the page address into SFR EEAH, register EEAL is not used. Then write 5AH to EESTCMD. The execution time for page erase is 9.4ms (typ) and is independent of the CPU clock.

Note: Do not attempt to apply read, write, or page-erase operations to the flash memory block in which the CPU is currently executing program instructions.

External Flash Memory Programming

The MAX7651/MAX7652 are normally shipped with the internal Flash memory blocks fully erased (all bits set to 1) and ready for external programming. External write, read (verify), and mass-erase operations are available. Flash memory addresses for either the upper or lower 8-kbyte blocks are specified at Ports 1 and 2.

Before applying any external Flash memory operations, power-up the MAX7651/MAX7652 with RST asserted. ALE, $\overline{PSEN}$, and ports P1 –P3 are pulled high with weak resistive pullups. Port P0 requires 10kΩ external pull-ups. Wait at least 10ms for the oscillator and internal circuitry to stabilize. The program, verify and mass-erase flash memory programming steps are outlined below.

Note: Failure to follow proper power-up conditions or the specified flash memory programming steps can result in loss of flash data integrity.

External Flash Memory Program (Table 2)

Erase operations. Set all bits to “1”. After a byte has been programmed it must be erased before it is re-written.

1) Power-up the device with RST asserted and allow ALE and $\overline{PSEN}$ to float to the “1” state (they will be internally pulled-up during RST assertion).
2) Wait 10ms for the internal bandgap and oscillator to stabilize.
3) Apply the memory location on the address lines at ports 1 and 2.
4) Apply data to the data lines at port 0.
5) Raise $\overline{EA}$ / V_{PP} to DV_{DD} and pull $\overline{PSEN}$ low.
6) Set P2.6, P2.7, P3.6, and P3.7 to the levels shown in Table 2.
7) Set P2.5 low or high for the lower or higher 8kB Flash memory block.
8) Force ALE / $\overline{PROG}$ low. P3.4 (READY) will go low to indicate a write in progress.
9) When P3.4 returns high (write complete after approximately 63μs), set ALE / $\overline{PROG}$ high.
10) Power-down sequence.
    - A) Remove drive from and allow $\overline{PSEN}$ and ALE/$\overline{PROG}$ to float high.
    - B) Pull $\overline{EA}$ low.
    - C) High-Z all digital pins.
    - D) Remove power from all power pins.

Note: Do not write to the same location more than twice before the next page/mass erase operation.

External Flash Memory Verify (Table 2)

External Verify:

If lock bits LB1 and LB2 have not been programmed, the programmed flash array(s) can be read back through the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

External verify (readback) power-up sequence:

1) Power-up the MAX7651/MAX7652 with RST asserted, allow ALE and $\overline{PSEN}$ to float to the “1” state (they will be internally pulled-up during RST assertion). Wait 10ms for the internal bandgap and oscillator to stabilize.
2) Pull $\overline{PSEN}$ LOW, $\overline{EA}$ HIGH, ALE HIGH, and set P2.6, P2.7, P3.6, P3.7, P2.5, as per *Flash Programming* Modes (Table 2) for reading either LOWER or UPPER flash memory block.

Note: P2.7 is cycled low/high to perform a FLASH read operation. Minimum low time for P2.7 is ten clock cycles.

External verify power-down sequence:

1) Power-down sequence
    - A) Remove drive from and allow $\overline{PSEN}$ and ALE/$\overline{PROG}$ to float high.
    - B) Pull $\overline{EA}$ low.
    - C) Hi-z all digital pins.
    - D) Remove power from all power pins.

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External Flash Memory Mass Erase

A mass erase operation sets all bits, including the lock bits to "1" (Table 22).

External Erase:

Both FLASH arrays can be simultaneously mass-erased electrically by using the proper combination of control signals as shown in Table 2. The erase operation must be executed before either memory can be programmed. Lock bits are also erased (Set to 1).

External chip erase power-up sequence:

1) Power-up chip with RST asserted, and allow ALE and $\overline{PSEN}$ to float to the "1" state (they will be internally pulled-up during RST assertion). Wait 10ms for the internal bandgap and oscillator to stabilize.
2) Pull $\overline{PSEN}$ LOW, $\overline{EA}$ HIGH, set P2.6, P2.7, P3.6, P3.7, and P2.5, as per Mass Erase mode in the Flash Programming Modes (table 2).
3) P3.4 will be LOW during mass erase cycle and return HI at the end of mass erase cycle.

External chip erase power-down sequence:

1) Power-down sequence

   A) Remove drive from and allow $\overline{PSEN}$ and ALE/$\overline{PROG}$ to float high.

   B) Pull $\overline{EA}$ low.

   C) Hi - z all digital pins.

   D) Remove power from all power pins.

Figure 2 shows the timing waveforms that apply for the Flash memory mass erase operation.

Flash Memory Lock Bits

The MAX7651/MAX7652 each contains three lock bits which can be left unprogrammed (logic "1") or can be programmed (logic "0") to obtain the additional features listed in the table below:

When lock bit "1" is programmed (set to logic "0"), the logic level at the $\overline{EA}$ pin is sampled and latched during RST deassertion. Subsequent changes in logic levels on $\overline{EA}$ have no effect. If the device is powered-up without a reset (RST), the latch initializes to a random value and holds that value until RST is pulsed high, then low. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Signature Bytes

The MAX7651/MAX7652 contain three signature bytes with the information shown in Table 23. Read each byte by following the *Flash Memory Read* procedure, but set P2.6, P2.7, P3.6, and P3.7 at low. Signature bytes are not affected by mass erase or page erase operations.

Table 21. Flash Memory Data (EEDAT) Format—SFR Address ECH

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0

Table 22. Flash Status and Control (EESTCMD) Format—SFR Address EDH

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
RDYHI/ EECMD7	RDYLO/ EECMD6	EECMD5	EECMD4	EECMD3	EECMD2	EECMD1	EECMD0

BIT	NAME	DESCRIPTION
7	RDYHI	High Block Ready Status. The MAX7651/MAX7652 set RDYHI to 0 during read, write, and page-erase operations that are applied to the 8-kbyte "high" block of flash memory. The bit is otherwise set to 1.
6	RDYLO	Low Block Ready Status. The MAX7651/MAX7652 set RDYLO to 0 during read, write, and page-erase operations that are applied to the 8-kbyte "low" block of flash memory. The bit is otherwise set to 1.
7 - 0	EECMD	Flash Memory Command Bits. Used to specify read, write, or page-erase memory commands. EECMD7 is the MSB.

Interrupt System

The MAX7651/MAX7652 has ten program-assist interrupts that are either external or internal to the 8051 system. Table 24 shows the SFR bit locations for interrupt enable and priority control. Shaded Table regions reflect the 8051 industry standard. Set SFR bit IE.7 high to enable all interrupts. See the MAX7651/MAX7652 *Programmer's Reference Manual*.

Timers

The MAX7651/MAX7652 feature several modes of timing control through the CKCON special function register. Table 25 shows the CKCON SFR format. The individual control bits can be used to set the number of clock cycles needed (four or twelve) to increment each timer/counter or the number of clock cycles needed to execute the MOVX instruction. See the MAX7651/MAX7652 *Programmer's Reference Manual* for further details.

Analog and Digital Supplies

The MAX7651/MAX7652 have multiple power-supply inputs: one analog AV_{DD} and three digital DV_{DD}. The pulse width modulators have their own power supply inputs, PWMV and PWMG. Decouple all supply inputs with a 0.1µF capacitor in parallel with a 10µF low ESR capacitor, with both capacitors as close to the supply pins as possible and with the shortest possible connection to the ground plane.

Table 23

PARAMETER	MIN	MAX	COMMENTS
T_{PROGL}	$10T_{CK}$		T_{PROGL} must equal T_{WRITE} during lockbit writes
T_{ASUW}	$3T_{CK}$		
T_{WRITE}	$7T_{CK}$ + 54µs	$7T_{CK}$ + 72µs	
T_{ADSUR}	$3T_{CK}$		
T_{READ}		$8T_{CK}$ + 50ns	Read access time
T_{P27L}	$10T_{CK}$		
T_{P27H}	$3T_{CK}$		
T_{CK}	83ns	250ns	

Note: *P2.6, P2.7, P3.6, and P3.7 must also meet T_{ASUW} (min) timing specification.*

Table 24. Lock Bit Protection Modes

PROGRAM LOCK BITS				PROTECTION TYPE
	LB1	LB2	LB3	
1	1	1	1	No program lock features (Default after a mass erase)
2	0	1	1	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset (RST), and further external data programming of both FLASH arrays is disabled.
3	0	0	1	Verify (read) is disabled. (see Mode 2)
4	0	0	0	External execution is disabled ($\overline{EA}$ override, see Mode 3).

Table 25. MAX7651/MAX7652 Signature Bits

ADDRESS	DATA	MEANING
30H	7FH	JEDEC Continuation Byte
31H	CBH	Manufactured by Maxim
32H	20H	MAX7651/MAX7652

Table 26. MAX7651/MAX7652 Interrupts (Note 1)

INTERRUPT	ASSOCIATED FEATURE	ENABLE SFR BIT (NOTE 2)	PRIORITY SFR BIT (NOTE 3)	PRIORITY
$\overline{INT0}$	External Interrupt 0	IE.0	IP.0	1
$\overline{INT1}$	External Interrupt 1	IE.2	IP.1	3
FLASH	Flash Operation Complete	EIE.0	EIP.0	8
ADC	A / D Operation Complete	EIE.1	EIP.1	9
WDTI	Watchdog Timer	EICON.1	EIP.4	10
TF0 or EXF0	Timer 0	IE.1	IP.1	2
TF1 or EXF2	Timer 1	IE.3	IP.3	4
TI_0 or RI_0	Serial Port 0	IE.4	IP.4	5
TF2 or EXF2	Timer 2	IE.5	IP.5	6
TI_1 or RI_1	Serial Port 1	IE.6	IP.6	7

Note 1: Shaded areas reflect the 8051 industry standard.

Note 2: Set Enable SFR bit high to enable interrupt.

Note 3: Set Priority SFR bit high to eatablish high priority.

Table 27. CKCON SFR Address 8EH

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
WD1	WD0	TIMER2	TIMER1	TIMER0	MD2	MD1	MD0

BIT	NAME	DESCRIPTION
7	WD1	Set WD1 and WD0 to adjust the interrupt interval for the watchdog timer. (See *Watchdog Timer.*)
6	WD10	
5	TIMER2	Timer 2 Control. Set TIMER2 = 1 for TIMER2-associated counter increments at four clock intervals. Set TIMER2 = 0 for increments at 12 clock intervals.
4	TIMER1	Timer 1 Control. Set TIMER1 = 1 for Timer1-associated counter increments at four clock intervals. Set TIMER1 = 0 for increments at 12 clock intervals.
3	TIMER0	Timer 0 Control. Set TIMER0 = 1 for Timer0-associated counter increments at four clock intervals. Set TIMER0 = 0 for increments at 12 clock intervals.
2	MD2	Set MD2, MD1, and MD0 to adjust the Read/Write strobe width (in clocks). The number of clock cycles is two plus the MD2, MD1, MD0 decimal value. MD0 is the LSB.
1	MD1	
0	MD0	

Power Requirements

MAX7651 operates from +5V while the MAX7652 operates from +3V analog and digital supply voltages. The analog supply current is typically 2mA. The typical digital supply currents (continuous A/D conversions at 12MHz clock frequency) are 5mA and 13mA at +3V and +5V, respectively. Current consumption will vary depending on RAM read/write and flash read/write page erase duty cycle.

Idle Mode

In idle mode, CPU processing is suspended and internal data registers maintain their current data. However, unlike typical 8051 systems, the clock is not disabled internally. Set PCON.0 (IDLE) high to enter the Idle mode after the instruction is complete. Figure 10 shows the related timing characteristics.

Enable any interrupt to clear PCON.0 and exit the Idle mode (See Figure 11 for the related timing). Assert RST alternately.

Stop Mode

In stop mode, the internal clock and analog circuitry are powered-down. Set PCON.1 (STOP) HIGH to enter the Stop mode after the instruction is complete. Figure 12 shows the related timing characteristics. The only way to exit Stop mode is to assert RST.

Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX7651/MAX7652 are measured using the best straight-line fit method.

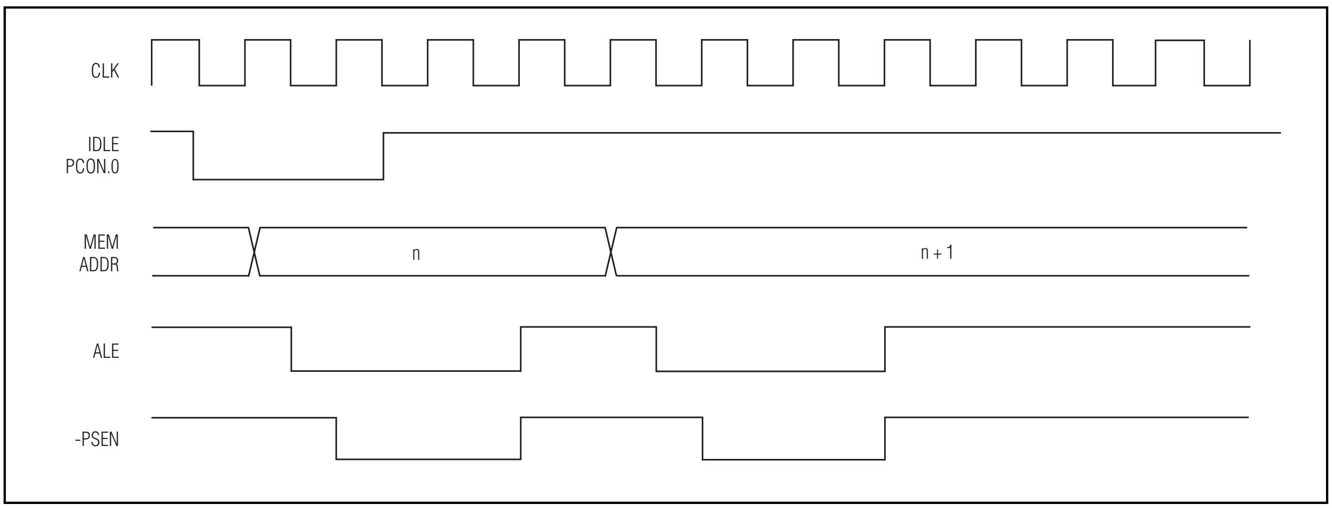


Figure 10. Idle Mode Entry Timing

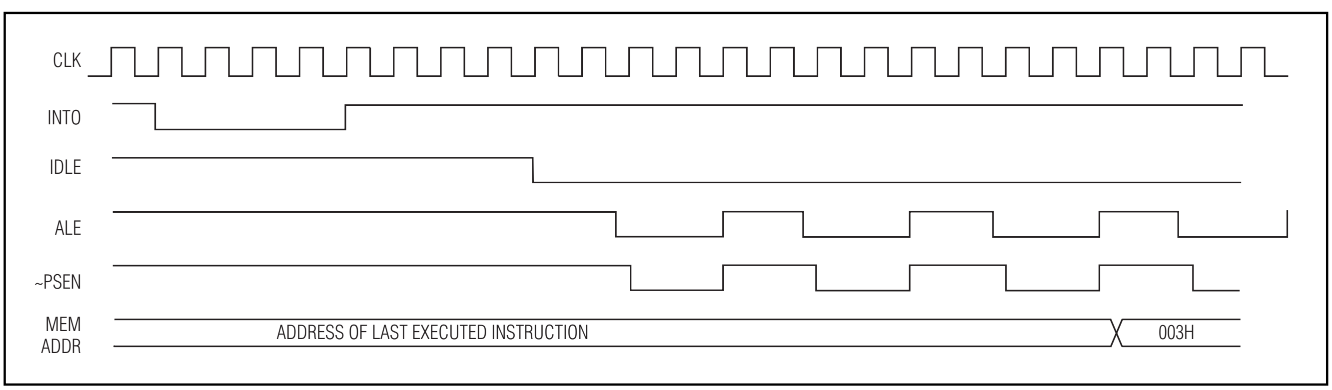


Figure 11. Idle Mode Exit Timing

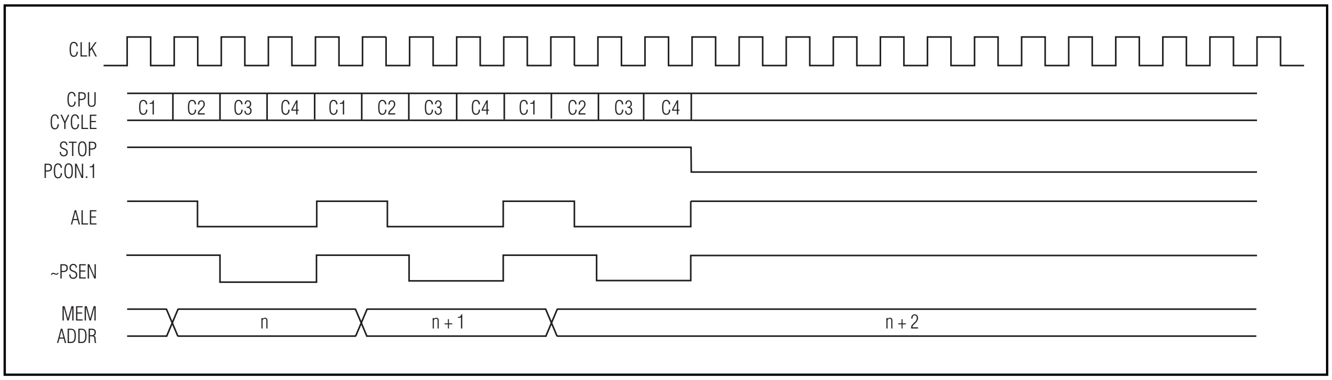


Figure 12. Stop Mode Timing

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

The offset error is the difference between the ideal and the actual offset points. For an ADC, the offset point is the midstep value when the digital output is zero.

Gain Error

The gain or full-scale error is the difference between the ideal and actual gain points on the transfer function, after the offset error has been canceled out. For an ADC the gain point is the midstep value when the digital output is full-scale.

Signal-To-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, SNR is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADCs resolution (N Bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise including thermal noise, reference noise, clock jitter. Therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-To-Noise Plus Distortion (SINAD)

Signal-To-Noise Plus Distortion is the ratio of the fundamental input frequency's RMS amplitude to RMS equivalent of all other ADC output signals.

$$SINAD\ (dB) = 20 \times \log (Signal_{RMS} / Noise_{RMS})$$

Effective Number Of Bits (ENOB)

ENOB indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADCs error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left[\frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)}}{V_1} \right]$$

where V1 is the fundamental amplitude, and V2 through V5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

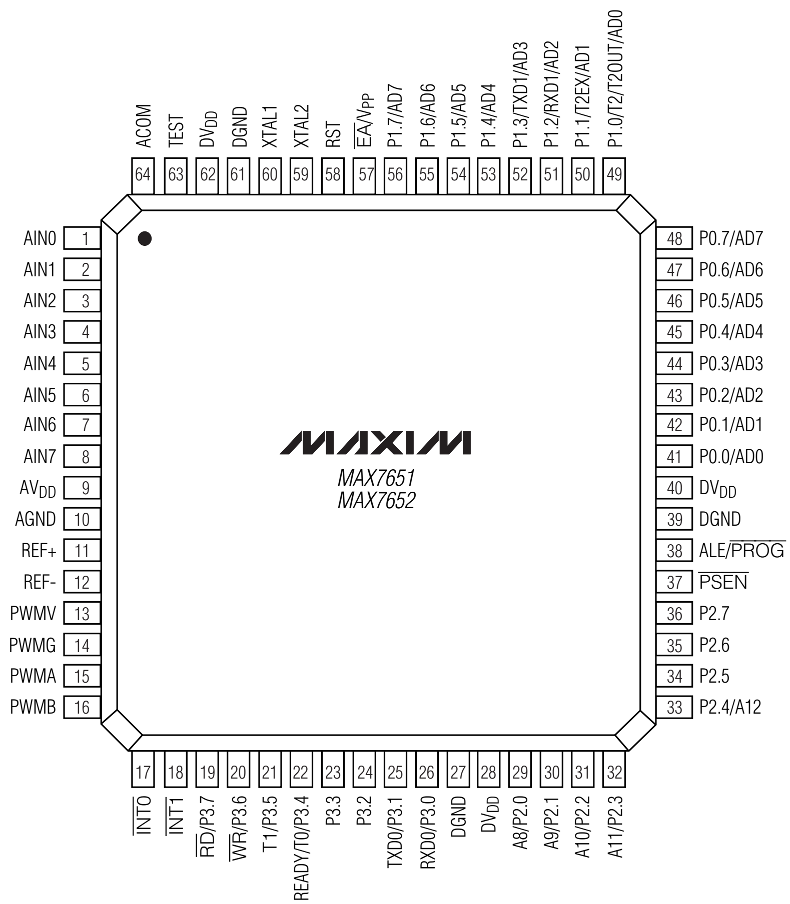
SFDR is the ratio of RMS amplitude of the fundamental maximum signal component to the RMS value of the next largest distortion component.

Chip Information

TRANSISTOR COUNT: 358,000

PROCESS: CMOS

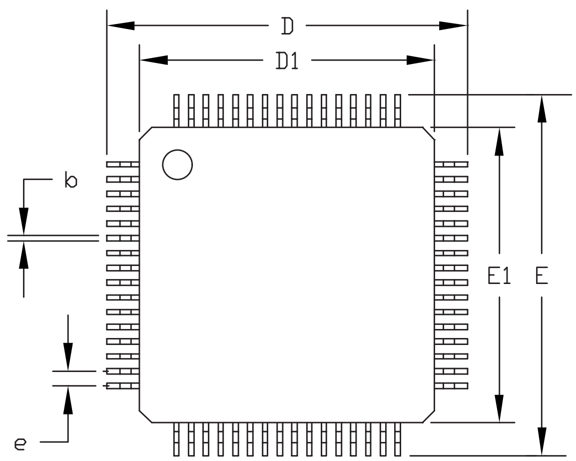
Pin Configuration

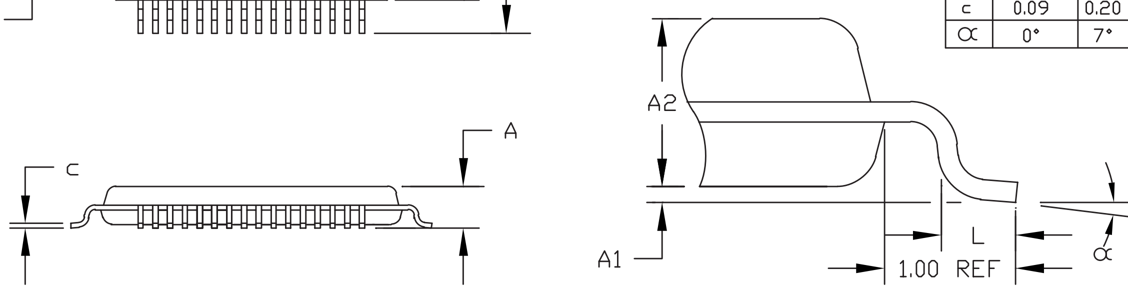


64-TQFP

Flash Programmable 12-Bit Integrated Data-Acquisition Systems

Package Information





JEDEC VARIATION		
	BJ	
	64 LEAD	
	MIN.	MAX.
A	---	1.60
A_1	0.05	0.15
A_2	1.35	1.45
D	12.00 BSC.	
D_1	10.00 BSC.	
E	12.00 BSC.	
E_1	10.00 BSC.	
e	0.5 BSC.	
L	0.45	0.75
b	0.17	0.27
c	0.09	0.20
α	0°	7°

64L, 10x10x1.4 TQFP.EPS

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BJ.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 64L, 10x10x1.4 MM TQFP

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