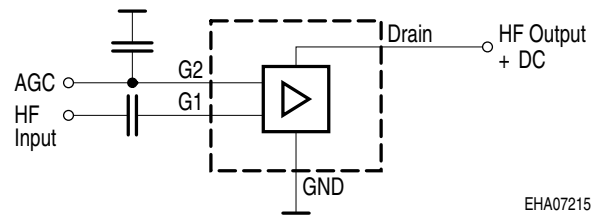
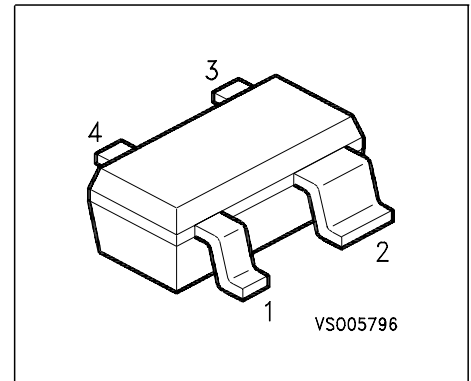


Dual - MOS FET Monolithic Integrated Circuit

- For low noise, high gain controlled input stages up to 1GHz
- Operating voltage 9V
- Integrated stabilized bias network



ESD: Electrostatic discharge sensitive device, observe handling precaution!

Class 2 (2000V - 4000V) pin to pin **Human Body Model**

Type	Marking	Pin Configuration						Package
BF1009SR	NZs	1=D	2=S	3=G1	4=G2	-	-	SOT143R

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	8	V
Continuous drain current	I_D	25	mA
Gate 1/ gate 2-source current	$\pm I_{G1/2SM}$	10	
Gate 1 (external biasing)	$+V_{G1SE}$	3	V
Total power dissipation $T_S \leq 76^\circ\text{C}$	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	$^\circ\text{C}$
Channel temperature	T_{ch}	150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Channel - soldering point ¹⁾	R_{thchs}	≤ 370	K/W

¹⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Note:

It is not recommended to apply external DC-voltage on Gate 1 in active mode.

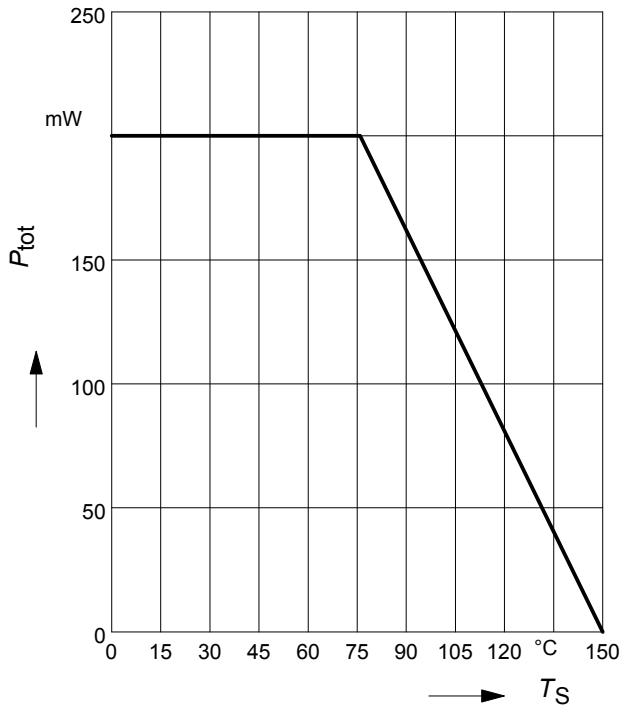
Electrical Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage $I_D = 300\text{ }\mu\text{A}$, $V_{G1S} = 0\text{ V}$, $V_{G2S} = 0\text{ V}$	$V_{(BR)DS}$	12	-	-	V
Gate1-source breakdown voltage $+I_{G1S} = 10\text{ mA}$, $V_{G2S} = 0\text{ V}$, $V_{DS} = 0\text{ V}$	$+V_{(BR)G1SS}$	8	-	12	
Gate2 source breakdown voltage $\pm I_{G2S} = 10\text{ mA}$, $V_{G1S} = 0\text{ V}$, $V_{DS} = 0\text{ V}$	$\pm V_{(BR)G2SS}$	10	-	13	
Gate1-source leakage current $V_{G1S} = 6\text{ V}$, $V_{G2S} = 0\text{ V}$	$+I_{G1SS}$	-	-	60	μA
Gate 2 source leakage current $\pm V_{G2S} = 8\text{ V}$, $V_{G1S} = 0\text{ V}$, $V_{DS} = 0\text{ V}$	$\pm I_{G2SS}$	-	-	50	nA
Drain current $V_{DS} = 9\text{ V}$, $V_{G1S} = 0$, $V_{G2S} = 6\text{ V}$	I_{DSS}	-	-	500	μA
Operating current (selfbiased) $V_{DS} = 9\text{ V}$, $V_{G2S} = 6\text{ V}$	I_{DSO}	10	14	19	mA
Gate2-source pinch-off voltage $V_{DS} = 9\text{ V}$, $I_D = 100\text{ }\mu\text{A}$	$V_{G2S(p)}$	-	0.9	-	V

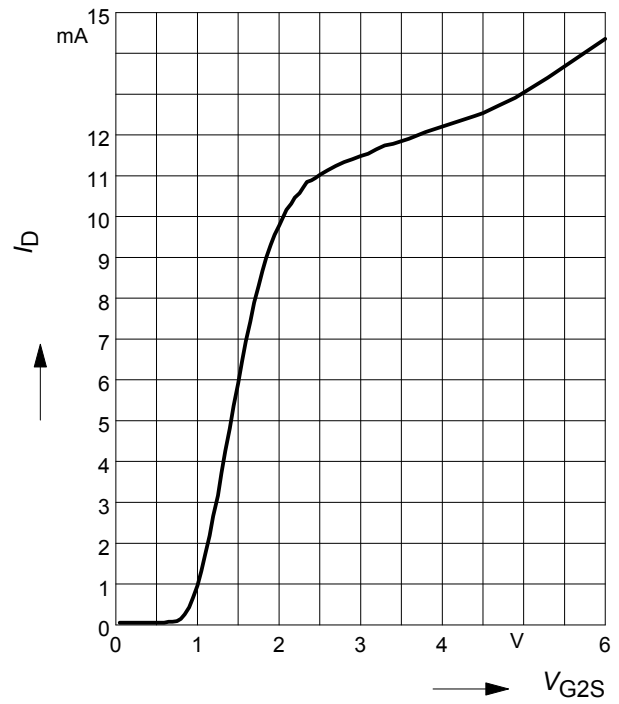
Electrical Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics					
Forward transconductance $V_{DS} = 9\text{ V}$, $V_{G2S} = 6\text{ V}$	g_{fs}	26	30	-	mS
Gate1 input capacitance $V_{DS} = 9\text{ V}$, $V_{G2S} = 6\text{ V}$, $f = 1\text{ MHz}$	C_{g1ss}	-	2.1	2.7	pF
Output capacitance $V_{DS} = 9\text{ V}$, $V_{G2S} = 6\text{ V}$, $f = 100\text{ MHz}$	C_{dss}	-	0.9	-	
Power gain (self biased) $V_{DS} = 9\text{ V}$, $V_{G2S} = 6\text{ V}$, $f = 800\text{ MHz}$	G_p	18	22	-	dB
Noise figure (self biased) $V_{DS} = 9\text{ V}$, $V_{G2S} = 6\text{ V}$, $f = 800\text{ MHz}$	F	-	1.4	-	dB
Gain control range $V_{DS} = 9\text{ V}$, $V_{G2S} = 6...0\text{ V}$, $f = 800\text{ MHz}$	ΔG_p	40	50	-	

Total power dissipation $P_{\text{tot}} = f(T_S)$

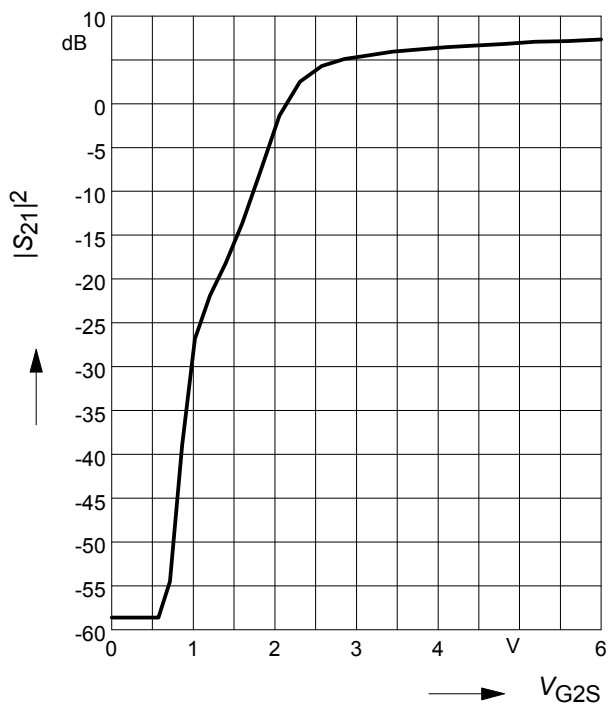


Drain current $I_D = f(V_{G2S})$



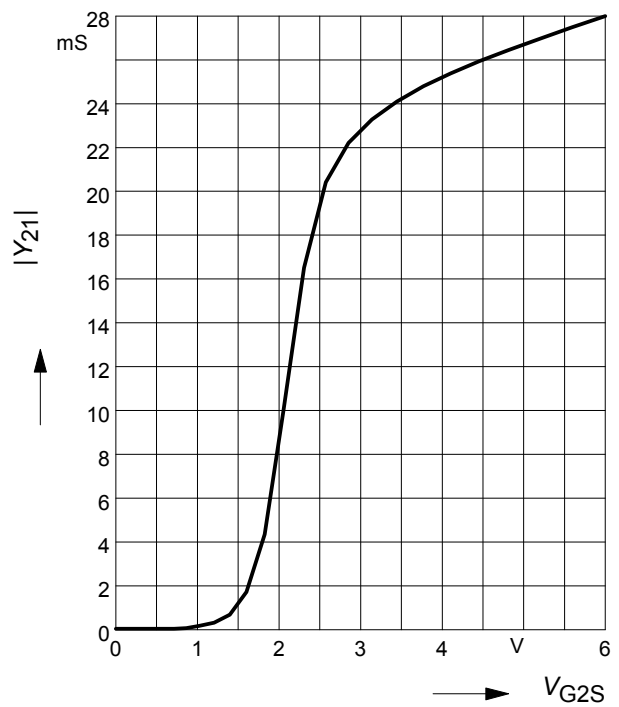
Insertion power gain

$$|S_{21}|^2 = f(V_{G2S})$$



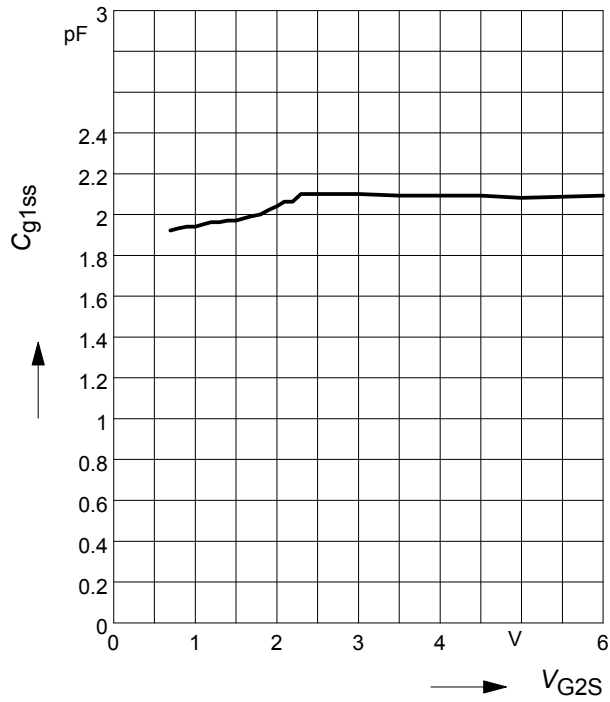
Forward transfer admittance

$$|Y_{21}| = f(V_{G2S})$$



Gate 1 input capacitance $C_{g1ss} = f(V_{G2S})$

$f = 200\text{MHz}$



Output capacitance $C_{dss} = f(V_{G2S})$

$f = 200\text{MHz}$

