NAU88L25

Ultra-Low Power Audio CODEC for Headphone/Headsets Application With 124dB Class G Headphone Drive and Advanced Headset Features

Description

The NAU88L25 is an ultra-low power high performance audio codec designed for headphone or headset application in smartphone, tablet PC, Chromebooks, laptop, game controller, Bluetooth headphones and other portable devices. It includes one I2S/PCM interface, one high quality stereo DACs, one mono ADC, a Class G stereo headphone amplifier, and industry leading advanced headset features.

Advanced on-chip signal processing engine including dynamic range compressor (DRC), programmable bi-quad filters, sidetone and ditial mixers, can maximize audio qualiy enhencements and eliminate the undersirable frequency components. A frequency locked loop(FLL) is also integrated in the design to support various clocks wih less external components.

The NAU88L25 has powerful headset detection mechanism, which detects jack insertion / ejection, microphone presence, speaker impedance, and up-to 8 user defined buttons with long/short key press debouce circuit. It also supports headphone crosstalk detection/suppression, and automatic microphone & ground detection / switching to work automatically with different audio jack formats without using external chips or components.

The NAU88L25 operates with analog supply voltages from 1.6V to 1.8V, while the digital core can operate from 1.1V to 1.98V to conserve power. The NAU88L25 is specified for operation from -40°C to +85°C, and is available in QFN 32 or CSP package with 0.4mm pitch.

Features

- DAC with auto attenuate : 124dB SNR; without auto mute: 113dB SNR, (A-weighted) @ 0dB gain, 1.8V and -89dB THD @ 20mW and RL= 32Ω, DAC playback to headphone output mode
- ADC : 101dB SNR (A-weighted) @ 0dB MIC gain, 1.8V, Fs = 48kHz and -91dB THD , 1.8V, MIC gain 0dB, OSR 128x
- 1 Digital I2S/PCM I/O port
- Dynamic Range Compressor (DRC)
- Programmable Biquad filter
- 1 Headset Mic, 1 Differential Analog Mic input, Line-input, or two single-ended Mic input
- Class G Headphone Amplifier(28mW @ 32Ω, 1% THD+N)
- Sampling rate from 8K to 192 KHz
- Headset Detection & Auto Headset switch for MIC and Ground
- Jack Insertion and Ejection Detection
- Distinct Keys Detection
- Package : 32 Pin QFN package, and Optional 42 Balls WLCSP with 0.4mm Pitch

Applications

- Gaming Controller
- Ultra-Portable Laptop
- Mobile Device
- Wireless Headset
- Smart Remote Controller

Block Diagram

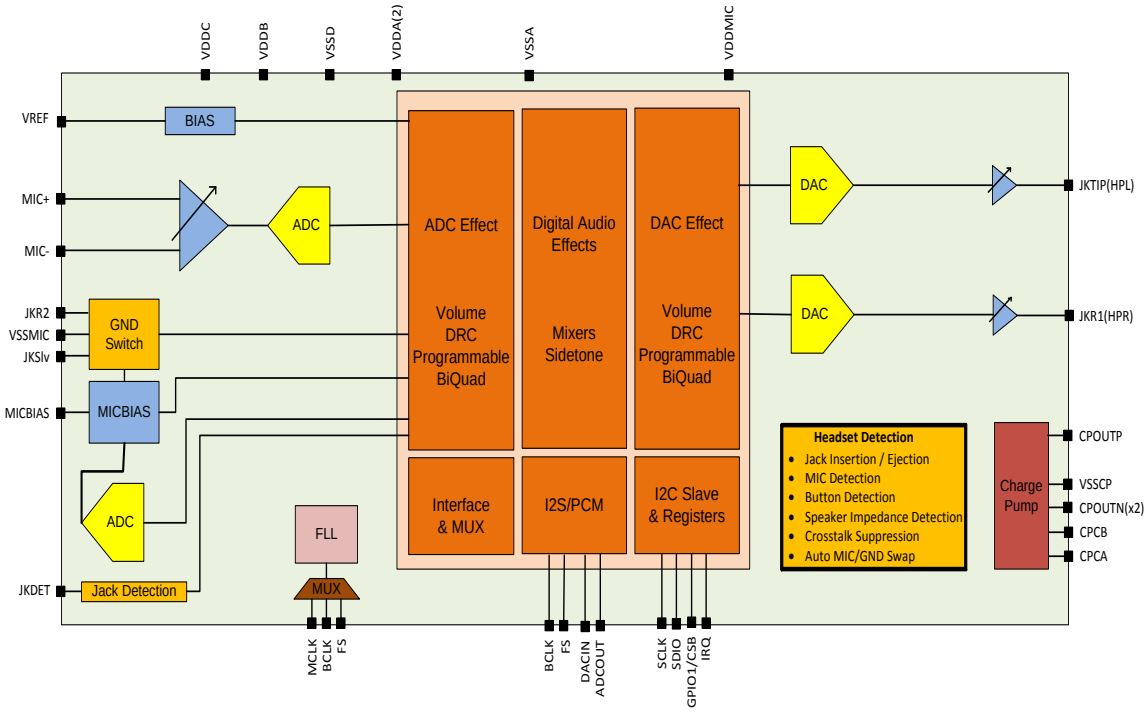
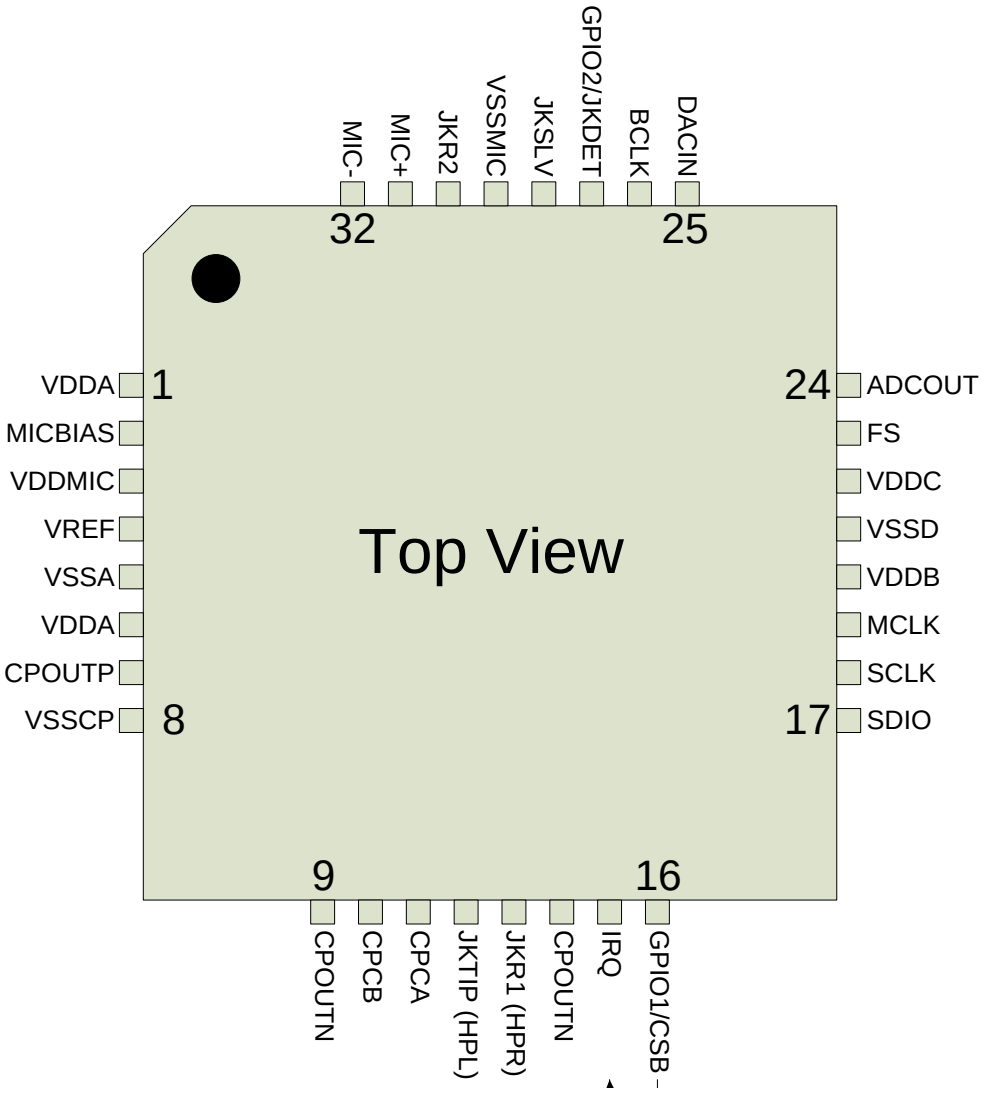


Figure 1: NAU88L25 Block Diagram

Pin Diagram


MIC-
MIC+
JKR2
VSSMIC
JKSLV
GPIO2/JKDET
BCLK
DACIN
32
25
VDDA 1
MICBIAS
VDDMIC
VREF
VSSA
VDDA
CPOUTP
VSSCP 8
24 ADCOUT
FS
VDDC
VSSD
VDDB
MCLK
SCLK
17 SDIO
Top View
9
16
CPOUTN
CPCB
CPCA
JKTIP (HPL)
JKR1 (HPR)
CPOUTN
IRQ
GPIO1/CSB

Pin Descriptions

Pin #	Name	Type	Functionality
1	VDDA	Supply	Analog Supply
2	MICBIAS	Analog Output	Microphone Bias Output
3	VDDMIC	Supply	Microphone supply
4	VREF	Analog I/O	Internal DAC & ADC voltage reference decoupling I/O
5	VSSA	Ground	Analog Supply Ground
6	VDDA	Supply	Analog Supply
7	CPOUTP	Analog I/O	Charge Pump positive voltage
8	VSSCP	Ground	Charge Pump Supply ground
9	CPOUTN	Analog I/O	Charge Pump negative voltage
10	CPCB	Analog I/O	Charge Pump switching capacitor node B
11	CPCA	Analog I/O	Charge Pump switching capacitor node A
12	JKTIP (HPL)	Analog Output	Headphone left channel output
13	JKR1 (HPR)	Analog Output	Headphone right channel output
14	CPOUTN	Analog I/O	Charge Pump negative voltage
15	IRQ	Digital Output	Programmable Interrupt Output
16	GPIO1	Digital I/O	General Purpose IO/I2C Address/SPI_CSB
17	SDIO	Digital I/O	Serial Data for I2C or SPI
18	SCLK	Digital Input	Serial Data Clock for I2C or SPI
19	MCLK	Digital Input	CODEC Master clock input
20	VDDB	Supply	Digital IO Supply
21	VSSD	Ground	Digital IO ground
22	VDDC	Supply	Digital core supply
23	FS	Digital I/O	Frame Sync input or output for I2S or PCM data
24	ADCOUT	Digital Output	Serial Audio data Output for I2S or PCM data
25	DACIN	Digital Input	Serial Audio data input for I2S or PCM data
26	BCLK	Digital I/O	Serial data bit clock input or output for I2S or PCM data
27	JKDET	Analog Input	Jack detect input
28	JKSLV	Analog I/O	Headset Jack pin 4
29	VSSMIC	Ground	Analog Supply Ground
30	JKR2	Analog I/O	Headset Jack pin 3
31	MIC+	Analog Input	PGA MIC1+ Analog Input
32	MIC1-	Analog Input	PGA MIC1- Analog Input

Electrical Characteristics

Conditions: $V_{DD}A = V_{DD}B = V_{DD}C = 1.8V$; $V_{DD}MIC = 4.2V$.
R_L(Headphone) = 32 Ω, f = 1kHz, MCLK=12.88MHz, unless otherwise specified. Limits apply for T_A = 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
ISD	Shutdown Current	$V_{DD}A$ in Shutdown Mode	0.2	1	µA
		$V_{DD}A$	0.2	1	
		$V_{DD}B$	0.2	1	
		$V_{DD}C$	2	10	
		$V_{DD}MIC$	0.2	1	
I_{DD}	Standby Mode	MCLK off, Jack Insertion, IRQ enabled	5		µA
		Headphone Amplifier			
P_O	Output Power	Stereo R_L = 32Ω, DAC Input, CPV_{DD}= 1.8V, f=1kHz, 22kHz BW, THD+N = 1%(CSP package), w. headset switch	30		mW
		Stereo R_L = 32Ω, DAC Input, CPV_{VDD} = 1.8V, f=1kHz, 22kHz BW, THD+N = 1% (QFN package), w. headset switch	28		mW
		Stereo R_L = 16Ω, DAC Input, CPV_{VDD} = 1.8V, f=1kHz, 22kHz BW, THD+N = 1% (CSP Package), w. headset switch	35		mW
		Stereo R_L = 16Ω, DAC Input, CPV_{VDD} = 1.8V, f=1kHz, 22kHz BW, THD+N = 1% (QFN Package), w. headset switch	35		mW
THD+N	Total Harmonic Distortion + Noise	R_L = 32Ω, f=1kHz, P_O = 20mW, with headset switch	-89		dB
SNR	Signal to Noise Ratio	VOUT = 1VRMS, DAC Input, DAC_Gain = 0dB, HP_Gain = 0dB, Digital Zero Input, f=1kHz, A-Weighted), w. headset switch	113		dB
		VOUT = 1 V_{RMS}, DAC Input, DAC_Gain = 0dB, HP_Gain = 0dB, Digital Zero Input, f=1kHz, A-Weighted, auto mute enabled, w. headset switch	124		dB
PSRR	Power Supply Rejection Ratio	f_{RIPPLE} = 217Hz, V_{RIPPLE} = 200mV_{P_P} Input Referred, HP_GAIN = 0dB DAC Input, DAC_Gain = 0dB Ripple Applied to $V_{DD}A$	81		dB
X_{TALK}	Channel Crosstalk	Left Channel to Right Channel, - 1dBFS, Gain = 0dB, f = 1kHz, MIC/GND Switching Off without HCS	88		dB
		Left Channel to Right Channel, -1dBFS, Gain = 0dB, f = 1kHz, MIC/GND Switching On with HCS	91		dB
	Interchannel Level Mismatch	Headphone Right and Left Channel Difference with 0dBFS Input Sweap from 20Hz to 20KHz	+/- 0.1		dB
	Frequency Response	F = 20Hz ~ 20KHz	+/-0.005		dB

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
e_{OS}	Output Noise	DAC_Gain = 0dB, HP_Gain = 0dB, f_S=48kHz, OSR_{DAC} = 128, A-Weighted	2.2		uV_{RMS}
	Out of Band Noise Level	BW=400Hz-500kHz	-86		dB
V_{OS}	Output Offset Voltage	HP_Gain = 0dB, DAC_Gain= 0dB, DAC Input	0.1	±0.5	mV
	Power Consunption	No Load, No Signal, f_S = 44.1kHz, 16Bit, OSR 32, Stereo DAC On, Amp On, R_{L} = 32Ω, VDDC = 1.2V	5.7		mW
	Pop and Click Noise	Into or Out of DAC to Headphone Shutdown, Headphone Impedance & Crosstalk Detection Disabled	0.1		mVrms
ADC					
THD+N	ADC Total Harmonic Distortion + Noise	MIC Input, MIC_GAIN = 0dB, VIN = 0.8Vrms, f=1KHz, fs = 48KHz, Mono Differential Input	-91		dB
		MIC Input, MIC_GAIN = 30dB, Volume = 0dB, Vin=28.5Vrms, f=1k, Digital Gain = 0dB, Mono Differential Input	-80		dB
SNR	Signal to Noise Ratio	Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0dB,fs = 48KHz, Mono Differential Input	101		dB
		Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 6dB,fs = 8KHz, Mono Differential Input	98		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP} applied to V_{DD}A, f_{RIPPLE} = 217Hz, Input Referred, MIC_GAIN = 0dB, Differential Input	78		dB
CMRR	Common Mode Rejection Ratio	Differential Input 100Vrms, PGA gain = 20dB, frequency sweep from 20Hz to 20KHz	64		dB
FS_{ADC}	ADC Full Scale Input Level	V_{DD}A= 1.8V	1		V_{RMS}
	Minimum Input Impedance		12		KOhm
	Frequency Response	f = 20Hz ~ 20KHz	+/-0.02		dB
	Power Consumption	No Load, No Signal, ADC on, PGA on, f_S = 44.1kHz	5.4		mW

Absolute Maximum Ratings

Parameter	Min	Max	Units
Digital Supply Range	-0.3	2.2	V
Digital I/O Supply Range	-0.3	6.0	V
Analog Supply Range	-0.3	2.2	V
Headphone Supply Range	-0.3	2.2	V
Microphone Bias Supply Voltage	-0.3	6.0	V
Voltage Input Digital Range	DGND - 0.3	VDD + 0.3	V
Voltage Input Analog Range	AGND - 0.3	VDD + 0.3	V
Junction Temperature, T_J	-40	+150	℃
Storage Temperature	-65	+150	℃

CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty

Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital Supply Range	VDDC	1.1	1.2	1.98	V
Digital I/O Supply Range	VDDB	1.6	1.8	3.6	V
Analog Supply Range	VDDA	1.6	1.8	2.0	V
Headphone Supply Range	VDDA	1.6	1.8	2.0	V
Microphone Bias Supply Voltage	VDDMIC	2.5	4.2	5.0	V
Temperature Range	T_A	-40		+85	℃

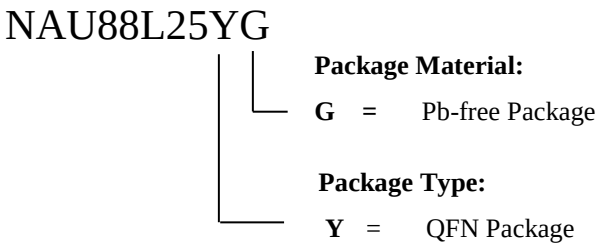
Digital I/O

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW level	V_{IL}	VDDB = 1.8V			0.33 * VDDB	V
		VDDB = 3.3V			0.37*VDDB	
Input HIGH level	V_{IH}	VDDB = 1.8V		0.67*VDDB		V
		VDDB = 3.3V		0.63*VDDB		
Output HIGH level	V_{OH}	I_{Load} = 1mA	VDDB=1.8V	0.9 * VDDB		V
			VDDB = 3.3V	0.95*VDDB		
Output LOW level	V_{OL}	I_{Load} = 1mA	VDDB = 1.8V		0.1 * VDDB	V
			VDDB=3.3V		0.05*VDDB	

Ordering Information

Part Number	Dimension	Package	Package Material
NAU88L25YG	5 x 5 mm	QFN-32L	Green

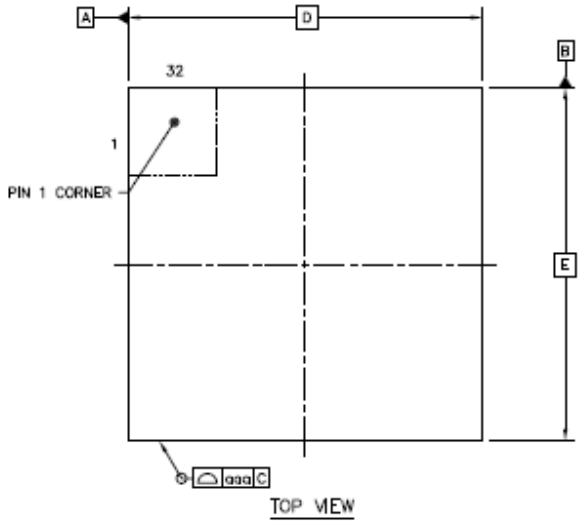
Nuvoton Part Number Description

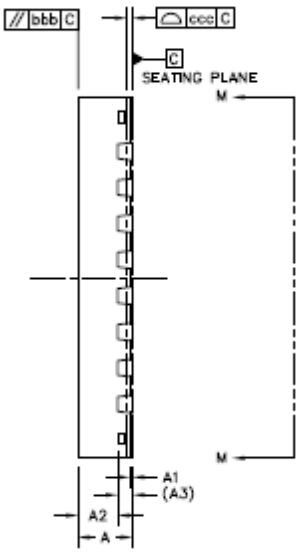


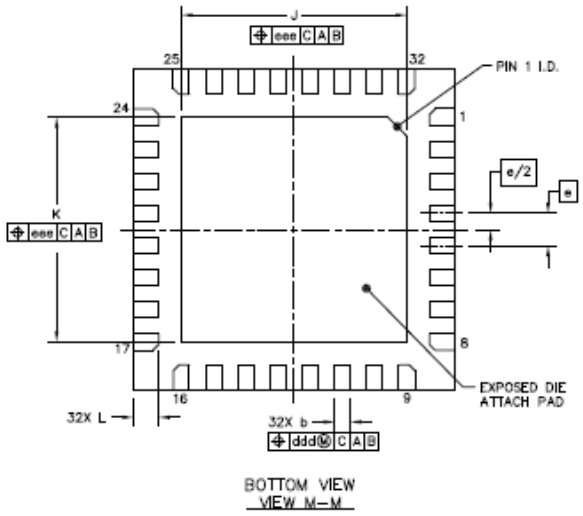
Package Information

QFN 32L 5X5 mm2, Thickness 0.8 mm(Max) ,Pitch 0.5 mm

(Saw Type) EP SIZE 3.5X3.5 mm







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Version History

VERSION	DATE	PAGE	DESCRIPTION
0.1	11/20/2014	NA	Preliminary Version
0.2	03/10/2015		Updated the pin-out and pin-descriptions
0.3	04/10/2015	8	Ordering info is added.
0.4	06/15/2015	5, 6	Updated Electrical Characteristics
0.5	07/16/2015	1	Updated the descriptions
0.6	09/28/2015	1, 2, 7, 8	Updated the descriptions and key features Updated the block diagram Changed VIH (input high voltage) Updated the package information
0.7	10/27/2015	9	Updated the package info

Table 1: Version History

Important Notice

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