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RENESAS

MOS INTEGRATED CIRCUIT

μPD17P149

SMALL, GENERAL-PURPOSE 4 BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P149 is a one-time PROM version of the μPD17149. It uses a one-time PROM, which can be written just once, instead of internal masked ROM of the μPD17149.

Since a user program can be written into the PROM, this microcontroller is suited for program evaluation and low-volume production of the μPD17145, μPD17147, μPD17149, or for program evaluation of the μPD17145(A), μPD17147(A), μPD17149(A), μPD17145(A1), μPD17147(A1), and μPD17149(A1). ★

The following user's manual completely describes the functions of the μPD17P149. Be sure to read it before designing an application system.

μPD17145 Sub-Series User's Manual: U10261E

FEATURES

- 17K architecture : General registers, 16-bit instructions
- Pin compatible with the μPD17149 (except for PROM programming function)
- Internal one-time PROM : 8K bytes (4096 × 16 bits)
- Supply voltage : V_{DD} = 2.7 to 5.5 V (when operating at the range between 400 kHz and 2 MHz with ceramic oscillation)
  V_{DD} = 4.5 to 5.5 V (when operating at the range between 400 kHz and 8 MHz with ceramic oscillation)

ORDERING INFORMATION

Part number	Package
μPD17P149CT	28-pin plastic shrink DIP (400 mil)
μPD17P149GT	28-pin plastic SOP (375 mil)

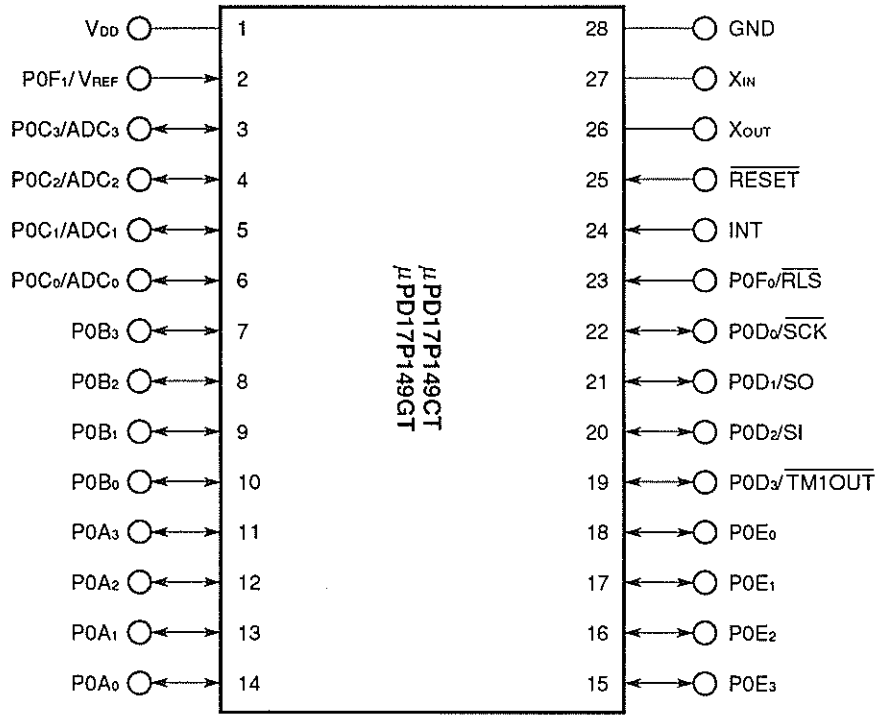
In the program memory write/verify mode, the voltage used for programming is applied to pin No. 23, P0F0/$\overline{RLS}$/V_{PP}. If a voltage of V_{DD} plus 0.3 V or more is applied to this pin in the normal operation mode, the microcontroller may crash. Design the circuit so that a voltage of this magnitude is never applied to the pin.

Document No. U11292EJ2V0DS00 (2nd edition)
(Previous No. IC-3504)
Date Published May 1996 P
Printed in Japan

The mark ★ shows major revised points.

PIN CONFIGURATION (TOP VIEW)

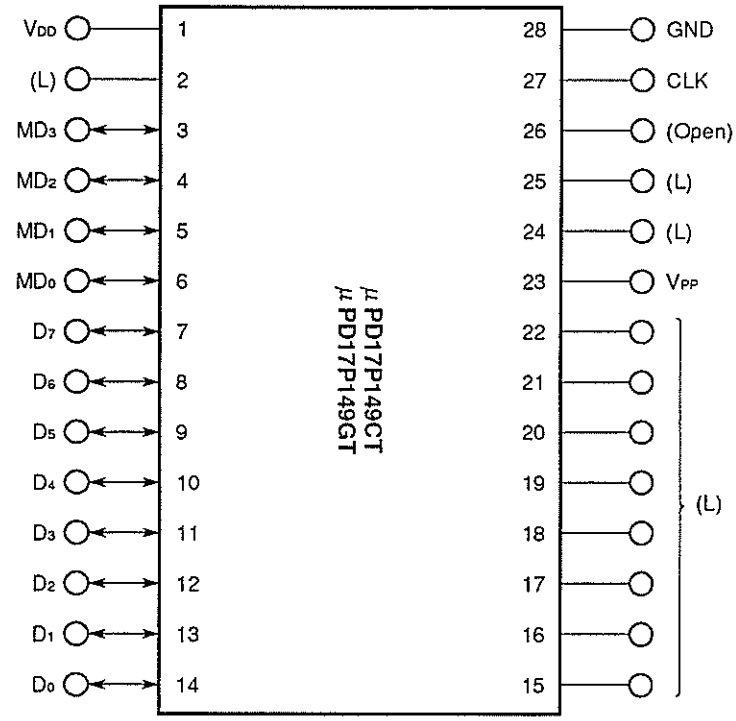
(1) Normal operation mode



ADC_0 - ADC_3	:	Analog input
GND	:	Ground
INT	:	External interrupt input
$P0A_0$ - $P0A_3$	:	Port 0A
$P0B_0$ - $P0B_3$	:	Port 0B
$P0C_0$ - $P0C_3$	:	Port 0C
$P0D_0$ - $P0D_3$	:	Port 0D
$P0E_0$ - $P0E_3$	:	Port 0E
$P0F_0$ and $P0F_1$	:	Port 0F

$\overline{RESET}$	:	Reset input
$\overline{RLS}$	:	Standby release signal input
$\overline{SCK}$	:	Serial clock input/output
SI	:	Serial data input
SO	:	Serial data output
$\overline{TM1OUT}$	:	Timer 1 carry output
V_{DD}	:	Power supply
V_{REF}	:	Reference voltage for the A/D converter
X_{IN}, X_{OUT}	:	System clock oscillation

(2) Program memory write/verify mode



CLK : Input clock for address update

D0 - D7 : Data

GND : Ground

MD0 - MD3 : Operating mode selection

VDD : Power supply

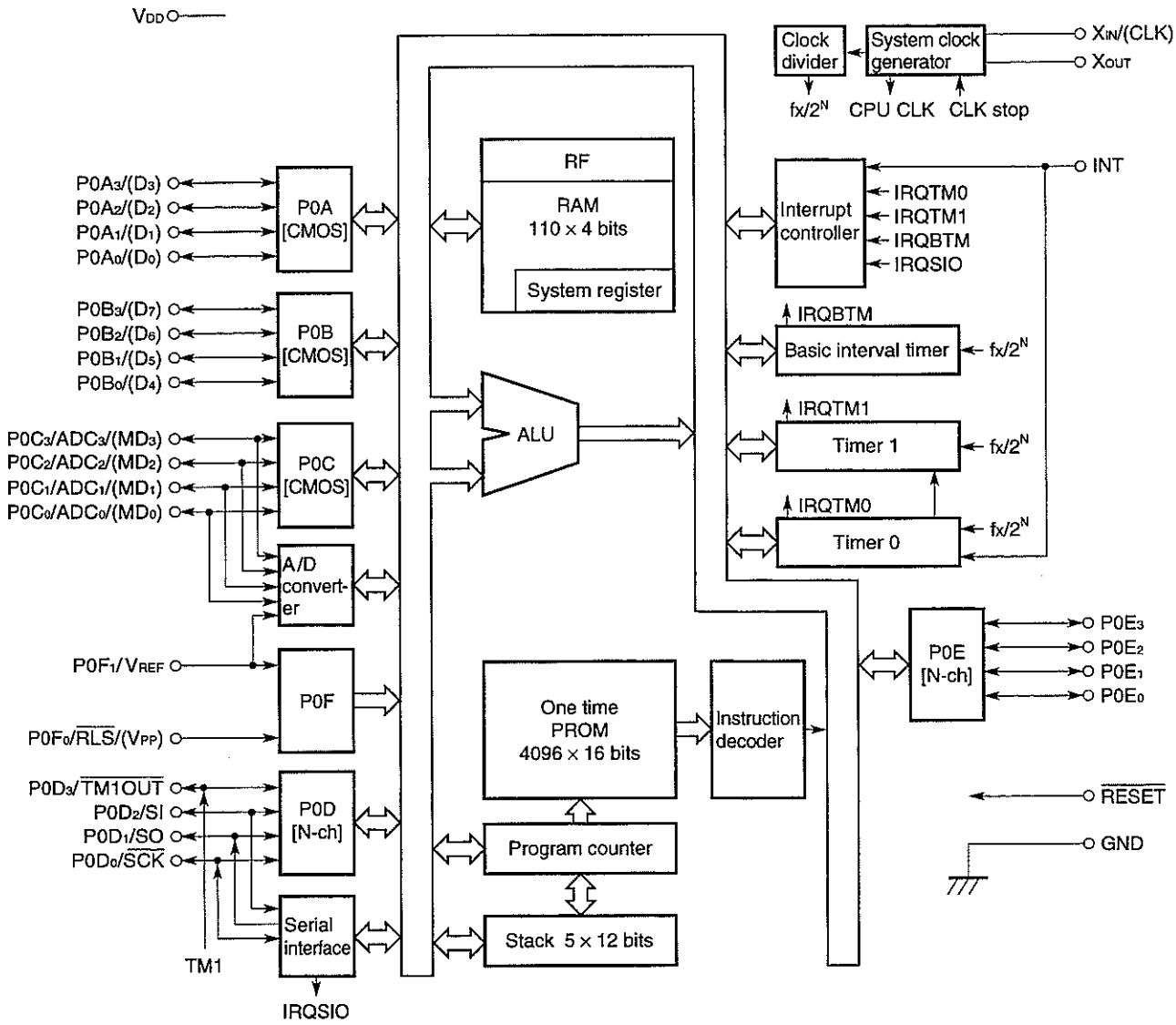
VPP : Programming power supply

Caution Symbols in parentheses denote processing for pins not used in the program memory write/verify mode.

L : Connect these pins separately to the GND pin through pull-down resistors.

Open : Nothing should be connected on these pins.

BLOCK DIAGRAM



Remark ( ) : PROM programming mode

The terms CMOS and N-ch in brackets indicate the output form of the port.

CMOS : CMOS push-pull output

N-ch : N-channel open-drain output

CONTENTS

1. PIN FUNCTIONS

1.1 NORMAL OPERATION MODE

Pin No.	Symbol	Function	Output	Upon reset
1	V_{DD}	Power supply	–	–

2	$P0F_1/V_{REF}$	Port 0F. The reference voltage is supplied to the A/D converter through this pin.
		• $P0F_1$
		  • Bit 1 of 2-bit input port P0F
		• V_{REF}
		  • Reference voltage input for the A/D converter
			Input	Input ($P0F_1$)

3 - 6	$P0C_3/ADC_3$ - $P0C_0/ADC_0$	Port 0C. Analog voltage is supplied to the A/D converter through these pins.
		• $P0C_3$ - $P0C_0$
		  • 4-bit input/output port
		  • Input/output setting allowed in units of 1 bit
		• ADC_3 - ADC_0
		  • Analog input for the A/D converter
			CMOS push-pull	Input (P0C)

7 8 9 10	$P0B_3$ $P0B_2$ $P0B_1$ $P0B_0$	Port 0B • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program in units of 4 bits	CMOS push-pull	Input
11 12 13 14	$P0A_3$ $P0A_2$ $P0A_1$ $P0A_0$	Port 0A • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program in units of 4 bits	CMOS push-pull	Input
15 16 17 18	$P0E_3$ $P0E_2$ $P0E_1$ $P0E_0$	Port 0E • Withstand voltage is V_{DD} (Max.). • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program in units of 4 bits	N-ch open drain	Input

Pin No.	Symbol	Function	Output	Upon reset
19	$P0D_3/\overline{TM1OUT}$	Pin for port 0D, timer 1 output, serial data input, serial data output, and serial clock input/output • Pull-up resistor incorporation specified by program bit by bit • Withstand voltage is V_{DD} (Max.). • $P0D_3$ - $P0D_0$ • 4-bit input/output port • Input/output setting allowed bit by bit • $\overline{TM1OUT}$ • Timer 1 output	N-ch open drain	Input (P0D)
20	$P0D_2$/SI	• SI • Serial data input		
21	$P0D_1$/SO	• SO • Serial data output		
22	$P0D_0/\overline{SCK}$	• $\overline{SCK}$ • Serial clock input/output		
23	$P0F_0/\overline{RLS}$	Pin for port 0F and input for standby mode release signal • $P0F_0$ • Bit 0 of 2-bit input port P0F • $\overline{RLS}$ • Input for standby mode release signal	Input	Input ($P0F_0$)
24	INT	Input for an external interrupt request signal and standby mode release signal.	Input	Input
25	$\overline{RESET}$	System reset input pin	Input	Input
26 27	X_{OUT} X_{IN}	For system clock oscillation The ceramic resonator is connected between X_{IN} and X_{OUT}.	–	–
28	GND	Ground	–	–

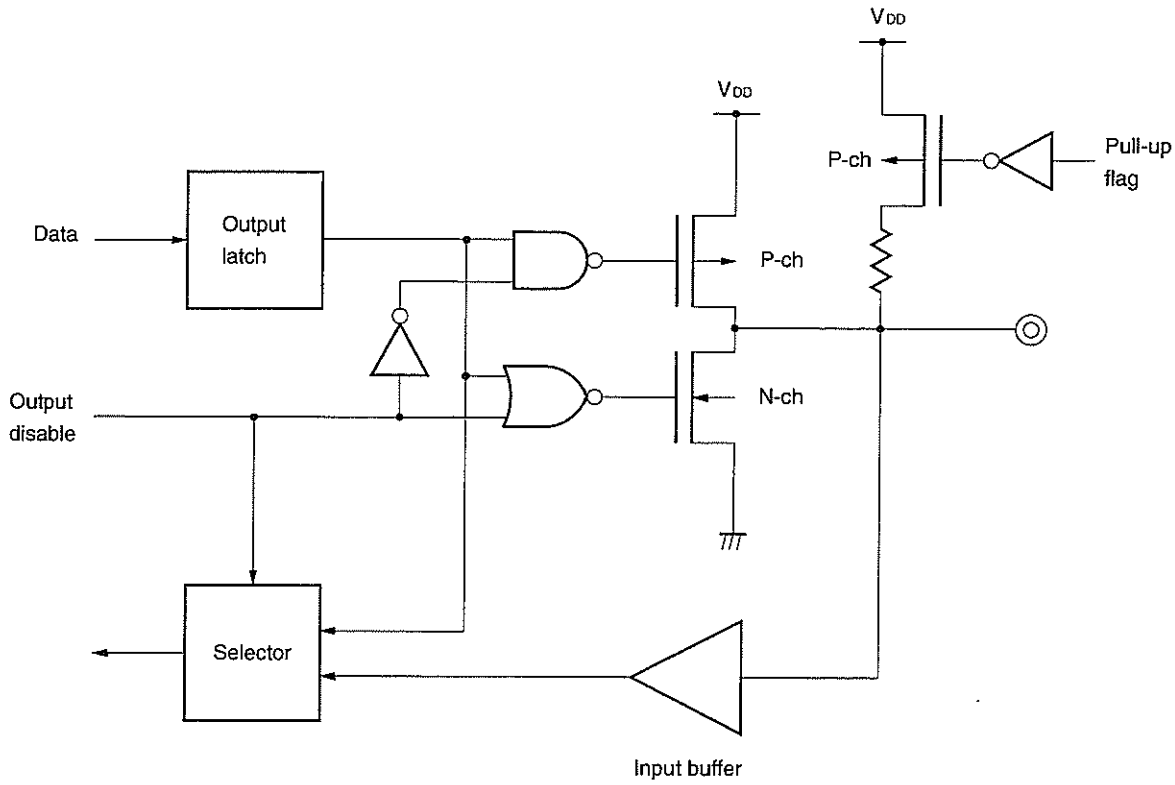
1.2 PROGRAM MEMORY WRITE/VERIFY MODE

Pin No.	Pin name	Function	Input/output
1	V_{DD}	Power supply pin. +6 V is applied to this pin when writing to program memory or verifying its contents.	–
3 to 6	MD_3 to MD_0	Input pins that select an operation mode when writing to program memory or verifying its contents	Input
7 to 14	D_7 to D_0	Input/output pins for 8-bit data used when writing to program memory or verifying its contents	Input/output
23	V_{PP}	Voltage (+12.5 V) is applied to this pin when writing to program memory or verifying its contents.	–
27	CLK	Input pin for address update clocks used when writing to program memory or verifying its contents	Input
28	GND	Ground	–

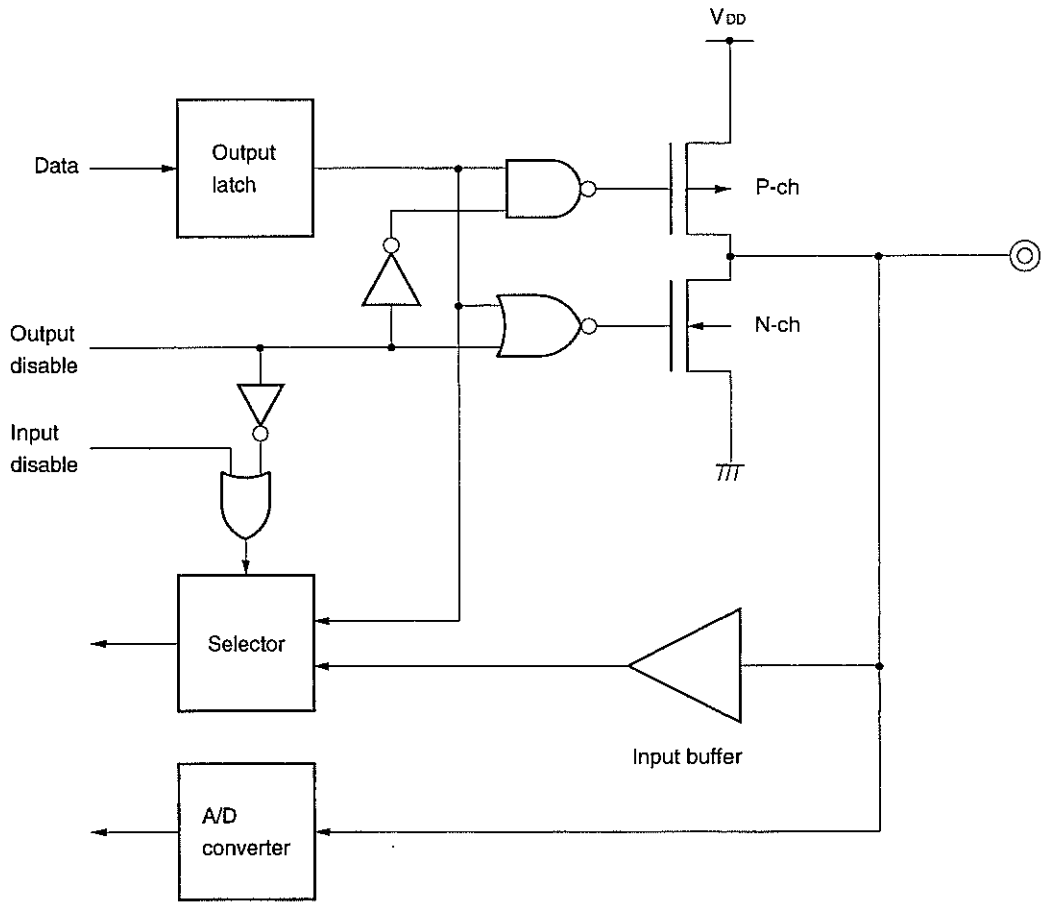
1.3 EQUIVALENT INPUT/OUTPUT CIRCUITS

Below are simplified diagrams of the input/output circuits for each pin.

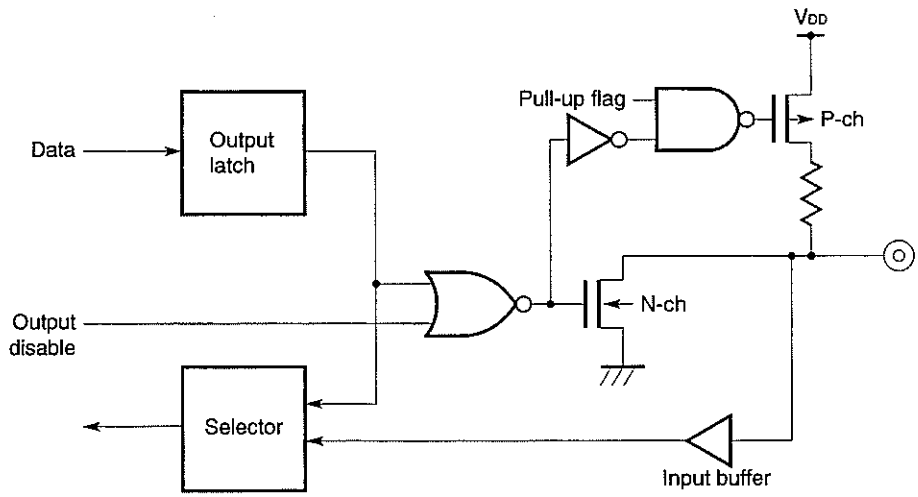
(1) $P0A_0$ - $P0A_3$, $P0B_0$ - $P0B_3$



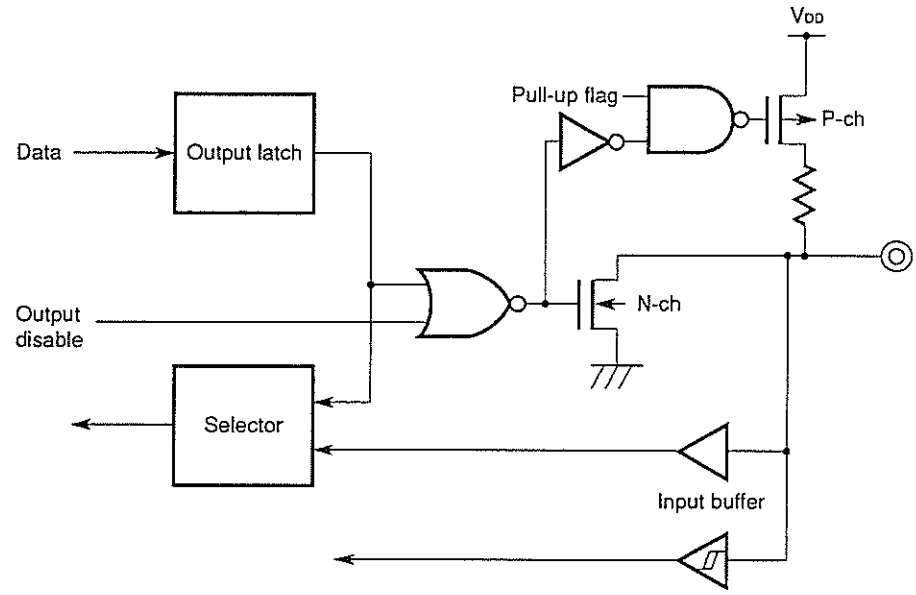
(2) P0C0/ADC0 - P0C3/ADC3



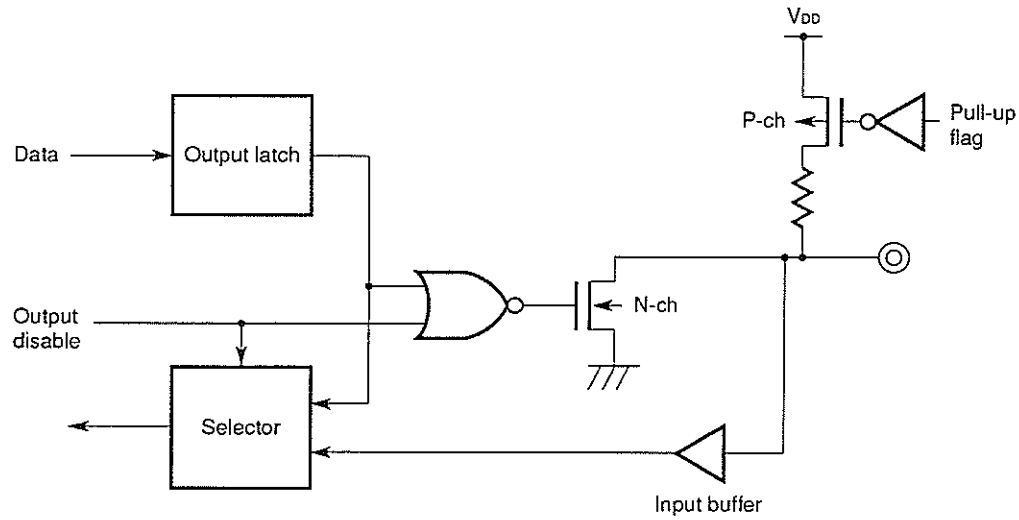
(3) P0D3/$\overline{\text{TM1OUT}}$, P0D1/SO



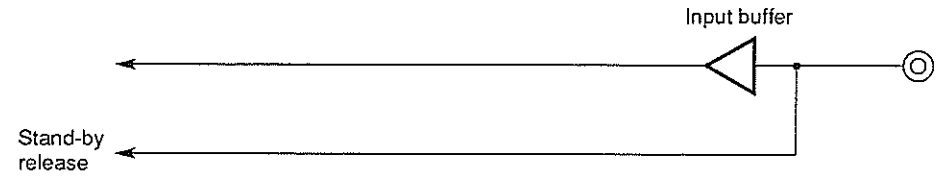
(4) $P0D_2/SI$, $P0D_0/\overline{SCK}$



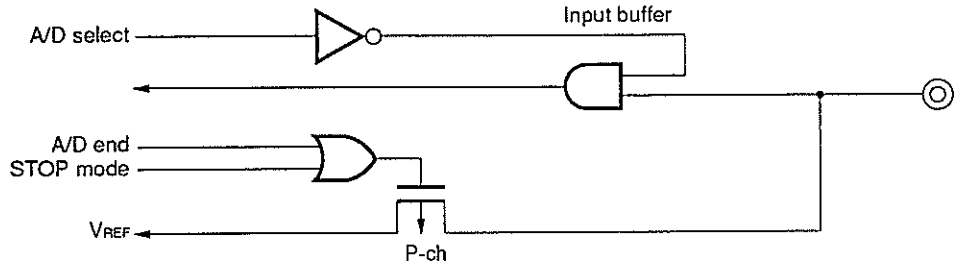
(5) $P0E_0$ - $P0E_3$



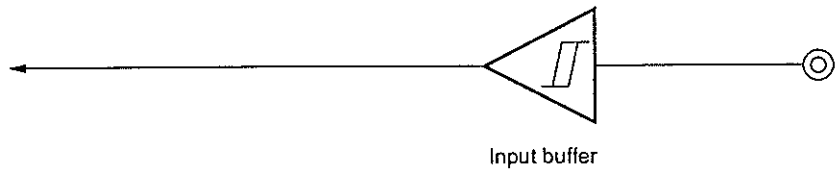
(6) $P0F_0/\overline{RLS}$



(7) P0F1/VREF



(8) $\overline{\text{RESET}}$, INT



1.4 HANDLING UNUSED PINS

Connect unused pins at the normal operation mode as follows:

Table 1-1 Handling Unused Pins ★

Pin			Conditions and handling	
			Internal	External
Port	Input mode	P0A, P0B, P0D, P0E	Pull-up resistors that can be specified with the software are incorporated.	Leave open.
		P0C	—	Connect to V_{DD} or ground through resistors for each pin.Note 1
		$P0F_1$	—	Connect directly to V_{DD} or ground.
		$P0F_0$Note 2	—	Connect directly to ground.
	Output mode	P0A, P0B, P0C (CMOS ports)	—	Leave open.
		P0D (N-ch open-drain port)	Outputs low level.	
		P0E (N-ch open-drain port)	Outputs low level without pull-up resistors that can be specified with the software.	
			Outputs low level with pull-up resistors that can be specified with the software.	
External interrupt (INT)			—	Connect directly to V_{DD} or ground.

Notes 1. When a pin is pulled up to V_{DD} (connected to V_{DD} through a resistor) or pulled down to ground (connected to ground through a resistor) outside the chip, take the driving capacity and maximum current consumption of a port into consideration. When using high-resistance pull-up or pull-down resistors, apply appropriate countermeasures to ensure that noise is not attracted by the resistors. Although the optimum pull-up or pull-down resistor varies with the application circuit, in general, a resistor of 10 to 100 kilohms is suitable.

2. Since the $P0F_0/\overline{RLS}$ pin is also used as the V_{PP} pin for writing and verifying the program memory, connect directly to ground when the pin is not used.

Caution To fix the I/O mode, pull-up resistors that can be specified with the software, and output level of a pin, it is recommended that they should be specified repeatedly within a loop in a program.

1.5 NOTES ON USE OF THE $\overline{\text{RESET}}$ AND P0F0/$\overline{\text{RLS}}$ PINS (ONLY AT THE NORMAL OPERATION MODE)

The $\overline{\text{RESET}}$ pin can be used as the test mode selection pin for testing the internal operation of the μPD17P149 (IC test), besides the usage shown in **Section 1.1.**

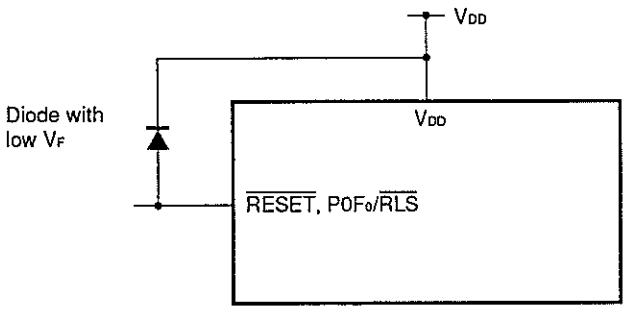
The P0F0/$\overline{\text{RLS}}$ pin can be used as the V_{PP} pin in the program memory write/verify mode.

Applying a voltage exceeding V_{DD} to the $\overline{\text{RESET}}$ or P0F0/$\overline{\text{RLS}}$ pin causes the μPD17P149 to enter the test mode or program memory write/verify mode. When noise exceeding V_{DD} comes in during normal operation, the device may not operate normally.

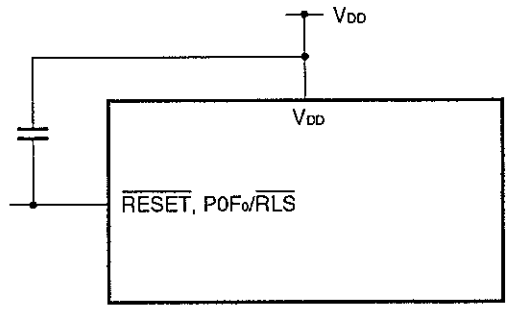
For example, if the wiring from the $\overline{\text{RESET}}$ or P0F0/$\overline{\text{RLS}}$ pin is too long, noise may be induced on the wiring, causing this mode switching.

When installing the wiring, lay the wiring in such a way that noise is suppressed as much as possible. If noise yet arises, use an external part to suppress it as shown below.

- **Connect a diode with low V_F between the pin and V_{DD}.**



- **Connect a capacitor between the pin and V_{DD}.**



2. DIFFERENCES BETWEEN THE μPD17145, μPD17147, μPD17149, AND μPD17P149

The μPD17P149 is a one-time PROM version of the μPD17149, in which the internal mask ROM is replaced with a one-time PROM.

Table 2-1 lists the differences between the μPD17145, μPD17147, μPD17149, and μPD17P149.

The μPD17P149 has the same CPU functions and internal peripheral hardwares as those of μPD17145, μPD17147, and μPD17149 except for its program memory, program size, address register size, and mask option.

Part of electrical characteristics is also different between those products. For details of the electrical characteristics, refer to the data sheet of each product.

Table 2-1 Differences between the μPD17145, μPD17147, μPD17149, and μPD17P149

Item	μPD17145	μPD17147	μPD17149	μPD17P149
Program memory (ROM)	Masked ROM			One-time PROM
	1024 × 16 bits (0000H-03FFH)	2048 × 16 bits (0000H-07FFH)	4096 × 16 bits (0000H-0FFFH)	
Program counter (PC)	10 bits	11 bits	12 bits	
Address register (AR)				
Address stack register				
Pull-up resistors of P0F, $\overline{\text{RESET}}$, and INT pins	Mask option			Not provided
Internal POC circuit	Mask option			Not provided
V_{PP} pin and operating mode selection pin	Not provided			Provided
Quality grade	• Standard μPD17145 • Special μPD17145 (A) μPD17145 (A1)	• Standard μPD17147 • Special μPD17147 (A) μPD17147 (A1)	• Standard μPD17149 • Special μPD17147 (A) μPD17147 (A1)	Standard
Electrical characteristics	Partially differs between these products. Refer to the data sheet of each product for details.			

★ ★

Caution Although a PROM product is highly compatible with a mask ROM product in respect of functions, they differ in internal ROM circuits and part of electrical characteristics. Before changing the PROM product to the mask ROM product in an application system, evaluate the system carefully using the mask ROM product.

3. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P149's internal program memory consists of a 4096 × 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in Table 3-1. Note that address inputs are not used; instead, the address is updated using the clock input from the CLK pin.

Caution The $P0F_0/\overline{RLS}/V_{PP}$ pin is used as the V_{PP} pin when writing to program memory or verifying its contents. If an voltage equal to or more than V_{DD} + 0.3 V is applied to the $P0F_0/\overline{RLS}$ pin in normal operation mode, the microcontroller may cause a system crash. Protect the pins from high voltages.

Table 3-1 Pins Used When Writing to Program Memory or Verifying Its Contents

Pin	Function
V_{PP}	Pin for applying programming supply voltage. Voltage (+12.5 V) is applied to this pin.
V_{DD}	Positive power supply pin. +6 V is applied to this pin.
CLK	Input pin for address update clocks. Input of four pulses to this pin updates the address of the program memory.
MD_0 - MD_3	Input pins that select an operation mode
D_0 - D_7	Input/output pins for 8-bit data

3.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V), the μPD17P149 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD_0 through MD_3 pins as follows. The X_{OUT} pin must be left open. Connect each pin not listed in Table 3-1 (including the $\overline{RESET}$ pin) to ground through a resistor.

Table 3-2 Specification of Operating Modes

Operating mode specification						Operating mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

Remark ×: Don't care. L (low) or H (high)

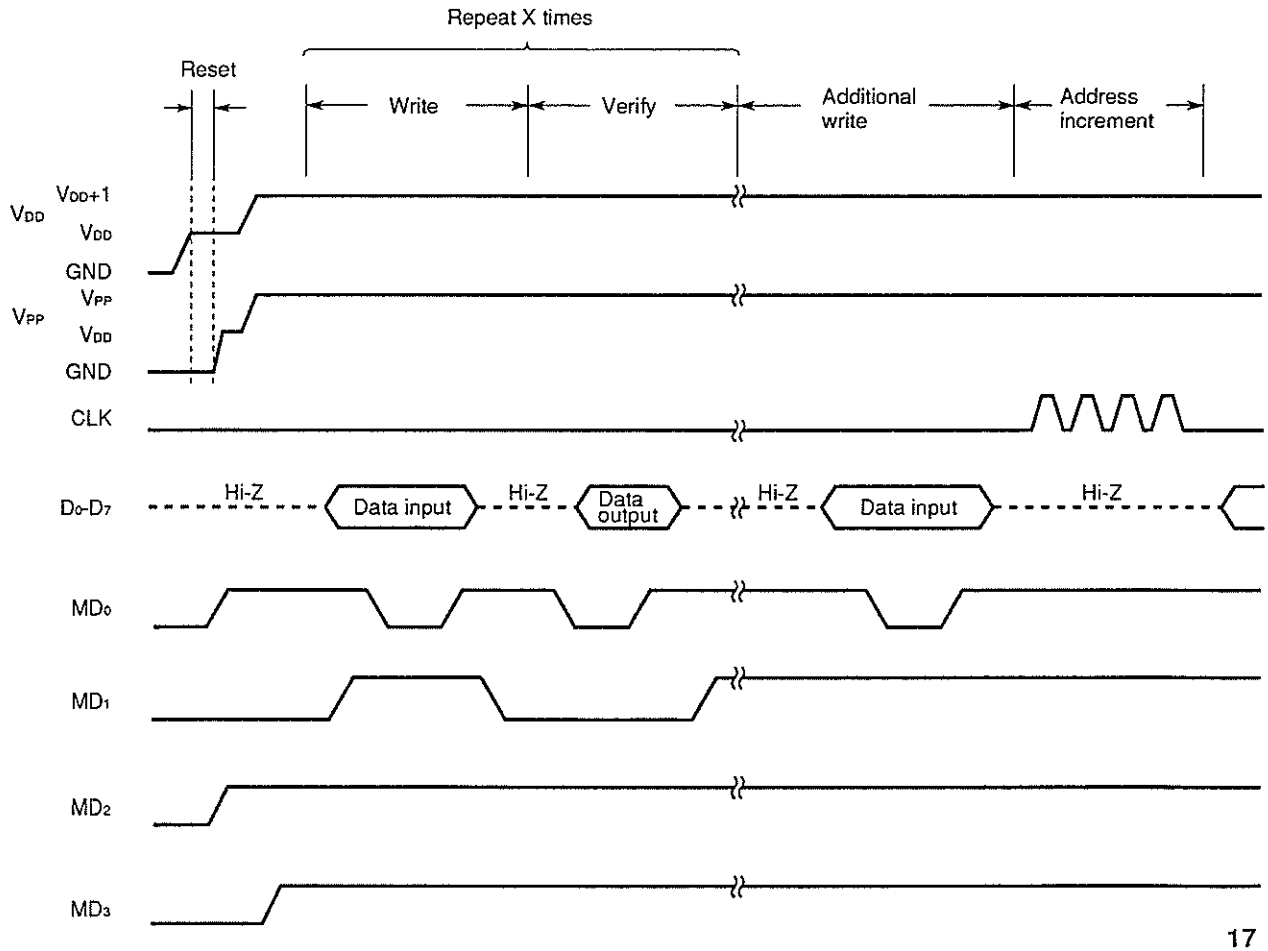
3.2 WRITING TO PROGRAM MEMORY

The procedure for writing to program memory is described below.

(1) Connect all unused pins to GND through resistors (the X_{OUT} pin is left open). Apply a low-level signal to the CLK pin.
(2) Apply 5 V to V_{DD} and apply a low-level signal to the V_{PP} pin.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Write data in 1-ms write mode.
(8) Select program inhibit mode.
(9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
(10) Perform additional write for X (number of repetitions of steps (7) to (9)) × 1 ms.
(11) Select program inhibit mode.
(12) Increment the program memory address by one on reception of four pulses on the CLK pin.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn power off.

A timing chart for program memory writing steps (2) to (12) is shown in Fig. 3-1.

Fig. 3-1 Timing Chart for Program Memory Writing Steps

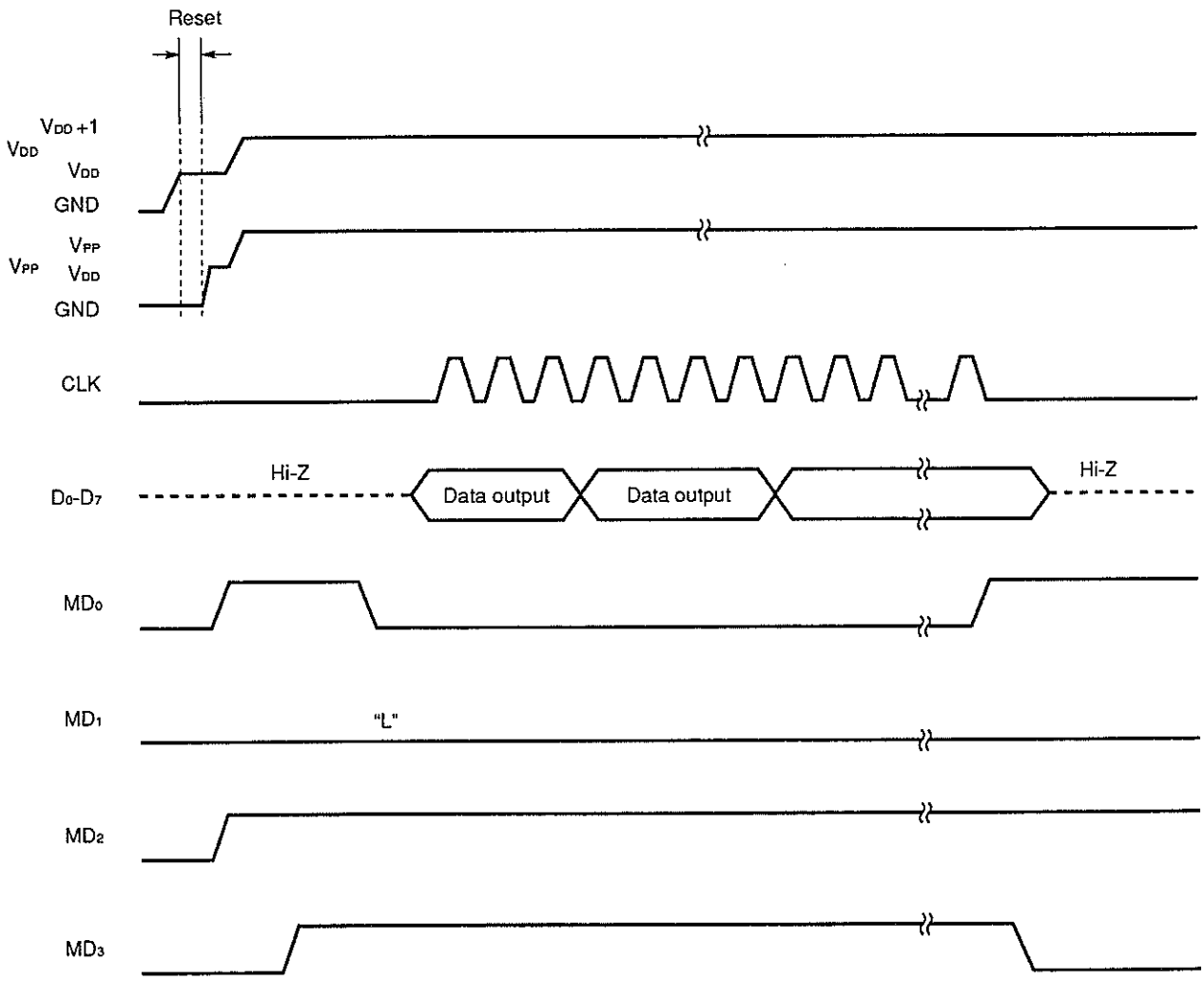


3.3 READING PROGRAM MEMORY

(1) Connect all unused pins to GND through resistors (the X_{OUT} pin is left open). Apply a low-level signal to the CLK pin.
(2) Apply 5 V to V_{DD} and apply a low-level signal to the V_{PP} pin.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for every four input clock pulses on the CLK.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn power off.

A timing chart for program memory reading steps (2) to (9) is shown below.

★ **Fig. 3-2 Timing Chart for Program Memory Reading Steps**



4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions		Rated value	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
PROM supply voltage	V_{PP}			–0.3 to +13.5	V
A/D converter reference voltage	V_{REF}			–0.3 to V_{DD} + 0.3	V
Input voltage	V_I	P0A, P0B, P0C, P0D, P0E, P0F, INT, $\overline{RESET}$, and X_{IN}		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}Note	Each of P0A, P0B, and P0C pins	Peak value	–15	mA
			rms	–7.5	mA
		Total of P0A, P0B, and P0C pins	Peak value	–30	mA
			rms	–15	mA
Low-level output current	I_{OL}Note	Each of P0A, P0B, and P0C	Peak value	15	mA
			rms	7.5	mA
		Each of P0D and P0E	Peak value	30	mA
			rms	15	mA
		Total of P0A, P0B, P0C, P0D, and P0E pins	Peak value	100	mA
			rms	50	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C
Allowable dissipation	P_d	T_A = 85 °C	28-pin plastic shrink DIP	140	mW
			28-pin plastic SOP	85	mW

Note Calculate a root-mean-square value as follows: [rms value] = [peak value] × $\sqrt{duty}$.

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

RECOMMENDED POWER VOLTAGE RANGE (T_A = –40 to +85 °C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	CPU (except A/D converter)	f_X = 400 kHz to 2 MHz	2.7		5.5	V
			f_X = 400 kHz to 4 MHz	3.6		5.5	V
			f_X = 400 kHz to 8 MHz	4.5		5.5	V
		A/D converter	Absolute accuracy: ±1.5 LSB, 2.5 V ≤ V_{REF} ≤ V_{DD}	4.0		5.5	V

DC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_A = −40 to +85 °C)

	Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
	High-level input voltage	V_{IH1}	P0A, P0B, P0C, P0D, P0E, and P0F		0.7V_{DD}		V_{DD}	V
		V_{IH2}	$\overline{RESET}$, SCK, SI, and INT		0.8V_{DD}		V_{DD}	V
		V_{IH3}	X_{IN}		V_{DD} − 0.5		V_{DD}	V
	Low-level input voltage	V_{IL1}	P0A, P0B, P0C, P0D, P0E, and P0F		0		0.3V_{DD}	V
		V_{IL2}	$\overline{RESET}$, SCK, SI, and INT		0		0.2V_{DD}	V
		V_{IL3}	X_{IN}		0		0.4	V
	High-level output voltage	V_{OH}	P0A, P0B, and P0C	4.5 ≤ V_{DD} ≤ 5.5, I_{OH} = −1.0 mA	V_{DD} − 0.3			V
				2.7 ≤ V_{DD} < 4.5, I_{OH} = −0.5 mA	V_{DD} − 0.3			V
	Low-level output voltage	V_{OL1}	P0A, P0B, P0C, P0D, and P0E	4.5 ≤ V_{DD} ≤ 5.5, I_{OL} = 1.0 mA			0.3	V
				2.7 ≤ V_{DD} < 4.5, I_{OL} = 0.5 mA			0.3	V
		V_{OL2}	P0D and P0E, I_{OL} = 15 mA	4.5 ≤ V_{DD} ≤ 5.5			1.0	V
				2.7 ≤ V_{DD} < 4.5			2.0	V
★	High-level input leakage current	I_{LIH}	P0A, P0B, P0C, P0D, P0E, P0F, $\overline{RESET}$, and INT, V_{IN} = V_{DD}				3	μA
★	Low-level input leakage current	I_{LIL}	P0A, P0B, P0C, P0D, P0E, P0F, $\overline{RESET}$, and INT, V_{IN} = 0 V				−3	μA
	High-level output leakage current	I_{LOH}	P0A, P0B, P0C, P0D, and P0E, V_{OUT} = V_{DD}				3	μA
	Low-level output leakage current	I_{LOL}	P0A, P0B, P0C, P0D, and P0E, V_{OUT} = 0 V				−3	μA
	Built-in pull-up resistance[Note 1]	R_{PULL}	P0A, P0B, and P0E		50	100	200	kΩ
			P0D		3	10	30	kΩ
	Power supply current[Note 2]	I_{DD1}	Normal operation mode	fx = 8.0 MHz, V_{DD} = 5 V ±10%		5.5	8.0	mA
				fx = 4.0 MHz, V_{DD} = 5 V ±10%		3.3	5.5	mA
				fx = 2.0 MHz, V_{DD} = 3 V ±10%		1.0	2.5	mA
				fx = 400 kHz, V_{DD} = 5 V ±10%		2.0	4.7	mA
				fx = 400 kHz, V_{DD} = 3 V ±10%		0.7	2.4	mA
		I_{DD2}	HALT mode	fx = 8.0 MHz, V_{DD} = 5 V ±10%		3.5	5.0	mA
				fx = 4.0 MHz, V_{DD} = 5 V ±10%		2.7	4.1	mA
				fx = 2.0 MHz, V_{DD} = 3 V ±10%		0.8	2.0	mA
				fx = 400 kHz, V_{DD} = 5 V ±10%		1.8	3.8	mA
				fx = 400 kHz, V_{DD} = 3 V ±10%		0.6	2.2	mA
		I_{DD3}	STOP mode	V_{DD} = 5 V ±10%		12	50	μA
				V_{DD} = 3 V ±10%		10	45	μA

Notes 1. Pull-up resistors are not incorporated for the P0F, $\overline{RESET}$, and INT pins.

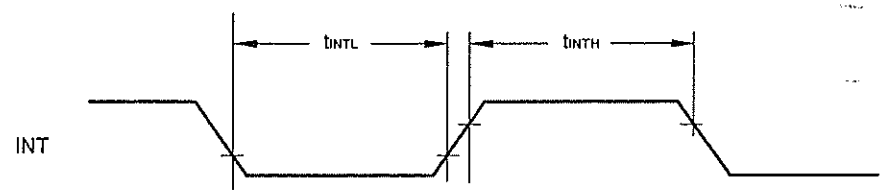
2. This current excludes the current which flows through the A/D converter and built-in pull-up resistors.

AC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_A = −40 to +85 °C)

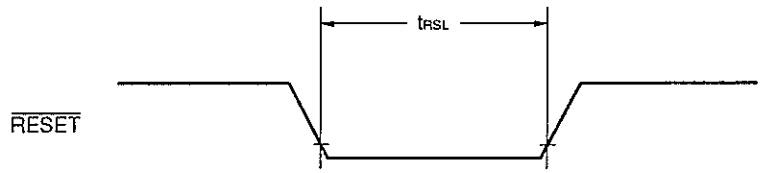
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CPU clock cycle time (instruction execution time)	t_{CY}	V_{DD} = 4.5 to 5.5 V	1.9		41	μs
		V_{DD} = 3.6 to 5.5 V	3.9		41	μs
			7.9		41	μs
INT input frequency (TM0 count clock input)	f_{INT}		0		400	kHz
INT high/low level width (external interrupt input)	t_{INTH}, t_{INTL}	V_{DD} = 4.5 to 5.5 V	10			μs
			50			μs
$\overline{RESET}$ low-level width	t_{RSL}	V_{DD} = 4.5 to 5.5 V	10			μs
			50			μs
$\overline{RLS}$ low-level width	t_{RLSL}	V_{DD} = 4.5 to 5.5 V	10			μs
			50			μs

Remark t_{CY} = 16/fx (fx: frequency of system clock oscillator)

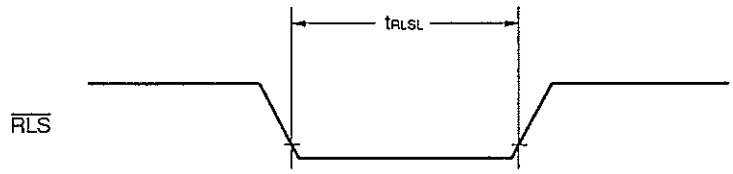
Interrupt input timing



$\overline{RESET}$ input timing



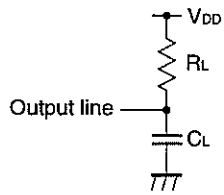
$\overline{RLS}$ input timing



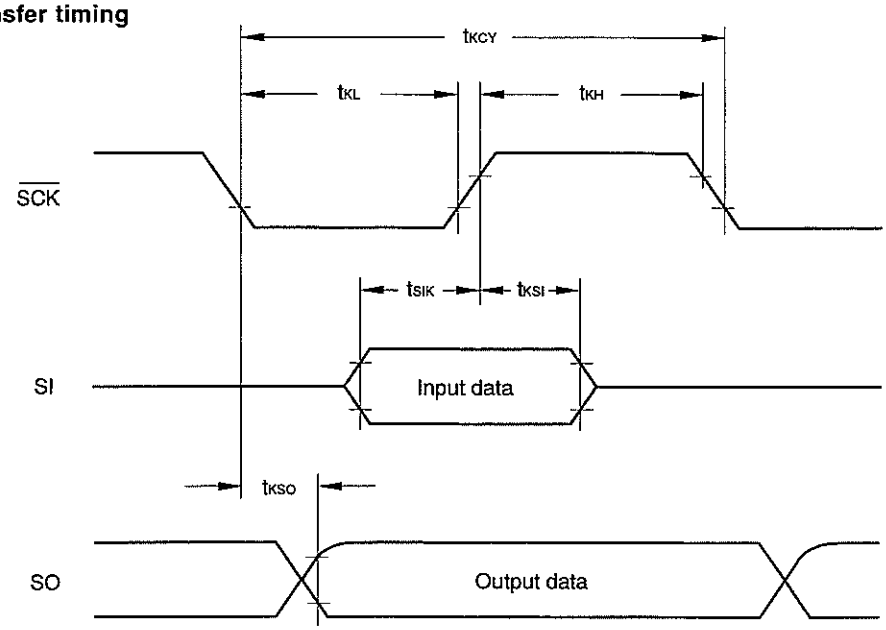
SERIAL TRANSFER OPERATION (V_{DD} = 2.7 to 5.5 V, T_A = −40 to +85 °C)

Parameter	Symbol		Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	Input	V_{DD} = 4.5 to 5.5 V		2.0			μs
					10			μs
		Output	R_L = 1 kΩ, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V	2.0			μs
					8			μs
			Built-in pull-up resistor, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V	32			μs
					64			μs
$\overline{SCK}$ high/low level width	t_{KH}, t_{KL}	Input	V_{DD} = 4.5 to 5.5 V		1.0			μs
					5.0			μs
		Output	R_L = 1 kΩ, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V	t_{KCY}/2-0.6			μs
					t_{KCY}/2-1.2			μs
			Built-in pull-up resistor, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V	t_{KCY}/2-12			μs
					t_{KCY}/2-24			μs
SI setup time (with respect to $\overline{SCK}$↑)	t_{SIK}				100			ns
SI hold time (with respect to $\overline{SCK}$↑)	t_{KSI}				100			ns
Delay from $\overline{SCK}$↓ to SO	t_{KSO}		R_L = 1 kΩ, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V			0.8	μs
							1.4	μs
			Built-in pull-up resistor, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V			14	μs
							26	μs

Remark R_L: a resistive load for the output line
C_L: a capacitive load for the output line



Serial transfer timing



A/D CONVERTER CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = −40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution			8	8	8	bit
Absolute accuracy[Note 1]		2.5 V ≤ V_{REF} ≤ V_{DD}			±1.5	LSB
Conversion time[Note 2]	t_{CONV}				25t_{CY}	μs
Analog signal input voltage	V_{ADIN}		0		V_{REF}	V
Reference input voltage	V_{REF}		2.5		V_{DD}	V
A/D converter circuit current	I_{ADC}	When A/D converter is operating		1.0	2.0	mA
V_{REF} pin current	I_{REF}			0.1	0.3	mA

Notes 1. Absolute accuracy excluding quantization error (±0.5 LSB)

2. Time from conversion start instruction execution to conversion end (ADCEND = 1) (at fx = 8 MHz, 50 μs)

Remark t_{CY} = 16/fx (fx: frequency of system clock oscillator)

SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_A = −40 to +85 °C)

Resonator[Note]	Parameter	Conditions	Min.	Typ.	Max.	Unit
Ceramic resonator	Oscillation frequency (fx)		0.39		2.04	MHz
		V_{DD} = 3.6 to 5.5 V	0.39		4.08	MHz
		V_{DD} = 4.5 to 5.5 V	0.39		8.16	MHz

Note Do not use a resonator having an oscillation generation time of 2 ms or more.

DC PROGRAMMING CHARACTERISTICS (T_A = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH1}	Except CLK	0.7V_{DD}		V_{DD}	V
	V_{IH2}	CLK	V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	Except CLK	0		0.3V_{DD}	V
	V_{IL2}	CLK	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
High-level output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} –1.0			V
Low-level output voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} power supply current	I_{DD}				30	mA
V_{PP} power supply current	I_{PP}	MD_0 = V_{IL}, MD_1 = V_{IH}			30	mA

Cautions 1. V_{PP} must be under +13.5 V including overshoot.

2. V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

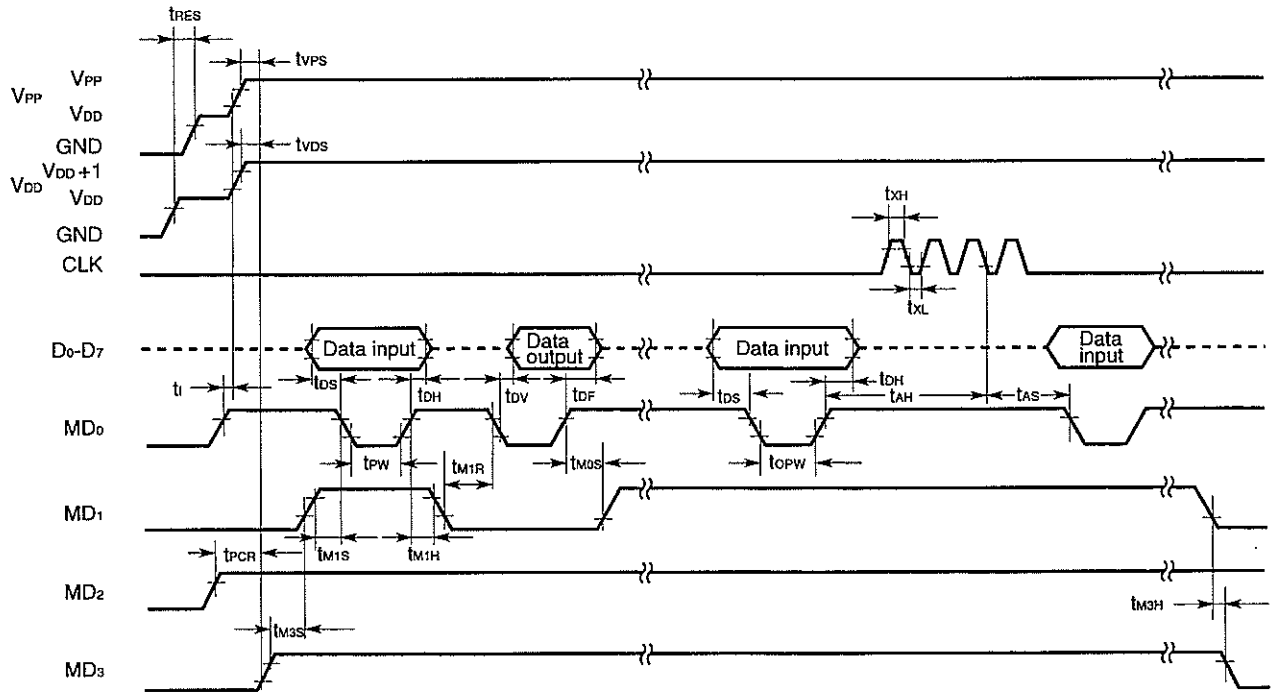
AC PROGRAMMING CHARACTERISTICS (T_A = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

Parameter	Symbol	Note 1	Conditions	Min.	Typ.	Max.	Unit
Address setup time[Note 2] to MD_0↓	t_{AS}	t_{AS}		2			μs
MD_1 setup time to MD_0↓	t_{M1S}	t_{OES}		2			μs
Data setup time to MD_0↓	t_{DS}	t_{DS}		2			μs
Address hold time[Note 2] to MD_0↑	t_{AH}	t_{AH}		2			μs
Data hold time to MD_0↑	t_{DH}	t_{DH}		2			μs
Data output float delay time from MD_0↑	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time to MD_3↑	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time to MD_3↑	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD_0 setup time to MD_1↑	t_{M0S}	t_{CES}		2			μs
Data output delay time from MD_0↓	t_{DV}	t_{DV}	$MD_0 = MD_1 = V_{IL}$			1	μs
MD_1 hold time to MD_0↑	t_{M1H}	t_{OEH}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
MD_1 recovery time to MD_0↓	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	–		10			μs
CLK input high, low level range	t_{XH}, t_{XL}	–		0.125			μs
CLK input frequency	fx	–				2	MHz
Initial mode set time	t_I	–		2			μs
MD_3 setup time to MD_1↑	t_{M3S}	–		2			μs
MD_3 hold time to MD_1↓	t_{M3H}	–		2			μs
MD_3 setup time to MD_0↓	t_{M3SR}	–	When reading program memory	2			μs
Data output delay time from address[Note 2]	t_{DAD}	t_{ACC}				2	μs
Data output hold time from address[Note 2]	t_{HAD}	t_{OH}		0		130	ns
MD_3 hold time to MD_0↑	t_{M3HR}	–		2			μs
Data output float delay time from MD_3↓	t_{DFR}	–				2	μs
Reset setup time	t_{RES}	–		10			μs

Notes 1. Symbols used for μPD27C256A (The μPD27C256A is used only for maintenance.)

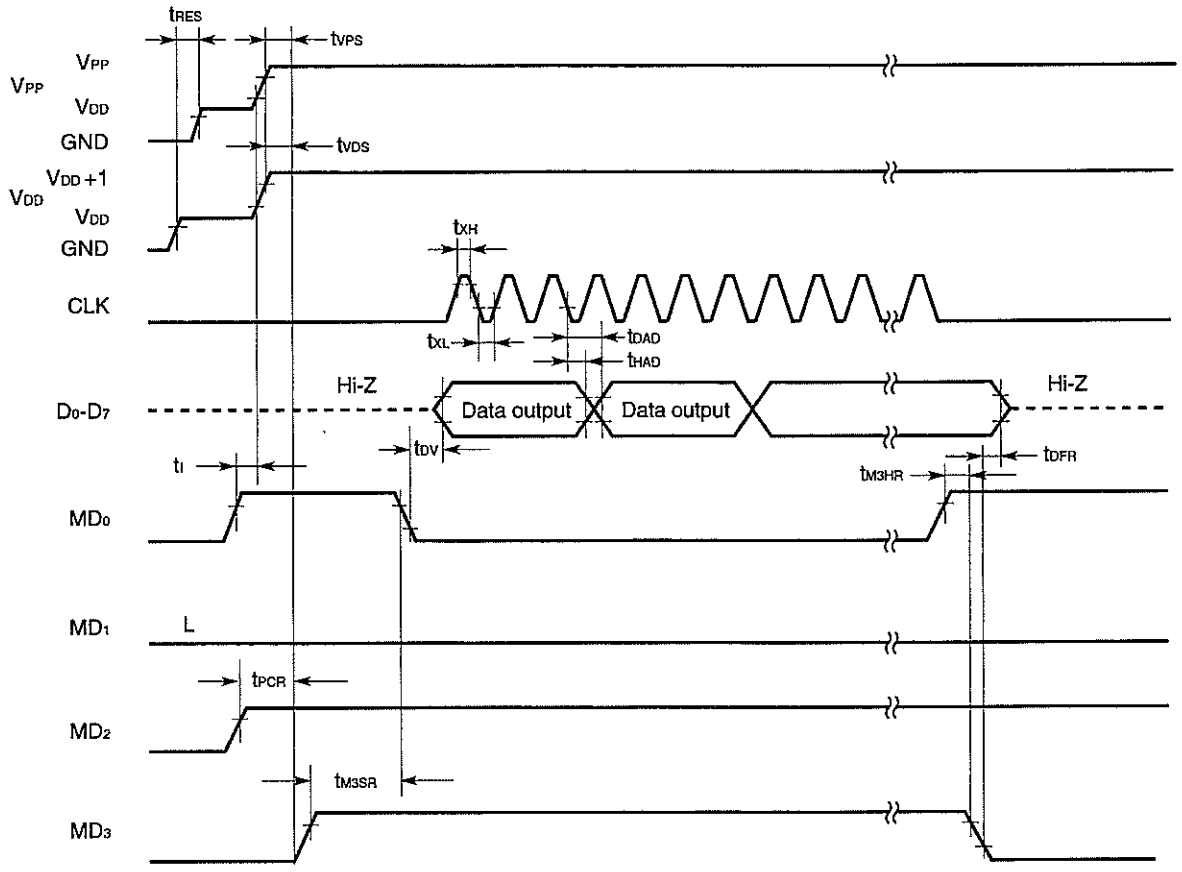
2. Internal address signal is incremented by one at the falling edge of the third CLK input.

Write program memory timing



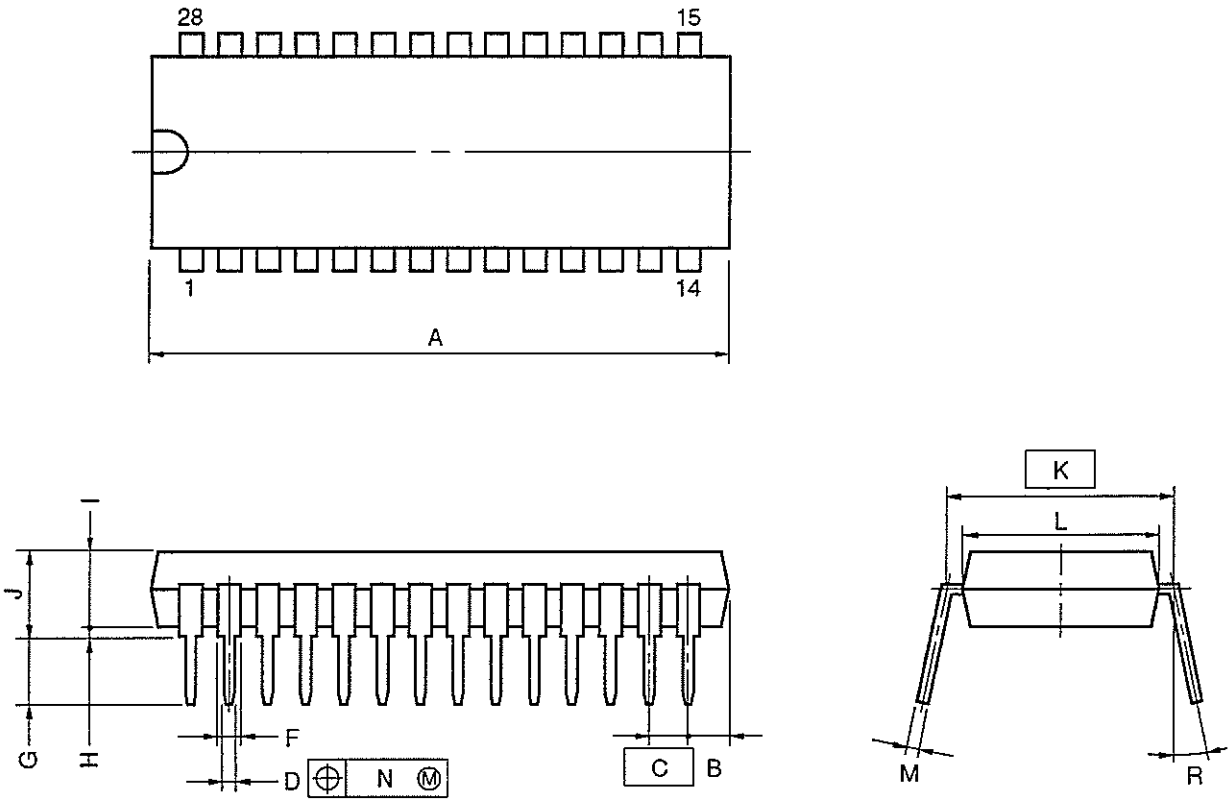
Remark The dashed line indicates high-impedance.

Read program memory timing



5. PACKAGE DRAWINGS

28 PIN PLASTIC SHRINK DIP (400 mil)



NOTES

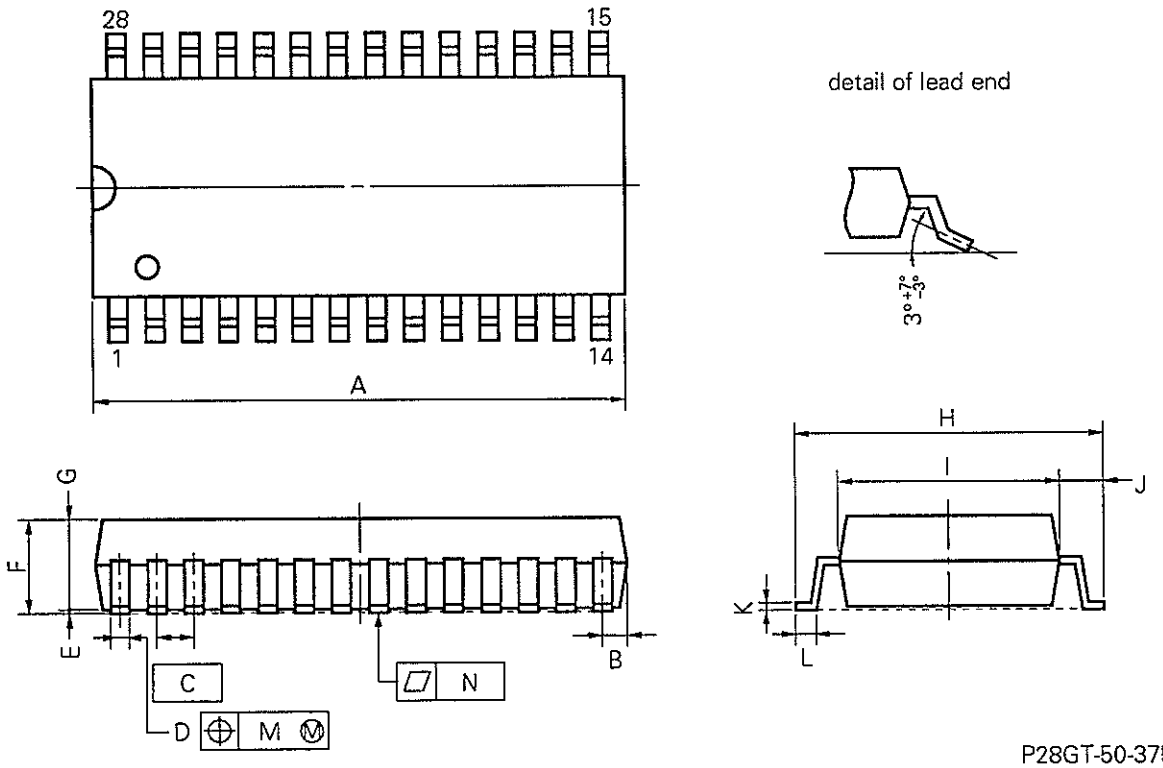
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

S28C-70-400B-1

28 PIN PLASTIC SOP (375 mil)



P28GT-50-375B-1

ITEM	MILLIMETERS	INCHES
A	18.2 MAX.	0.717 MAX.
B	0.845 MAX.	0.034 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.125±0.075	0.005±0.003
F	2.9 MAX.	0.115 MAX.
G	2.50±0.2	$0.098^{+0.009}_{-0.008}$
H	10.3±0.3	$0.406^{+0.012}_{-0.013}$
I	7.2±0.2	$0.283^{+0.009}_{-0.008}$
J	1.6±0.2	0.063±0.008
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

6. RECOMMENDED SOLDERING CONDITIONS ★

The conditions listed below shall be met when soldering the μPD17P149.

For details of the recommended soldering conditions, refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 6-1 Soldering Conditions for Surface-Mount Devices

μPD17P149GT: 28-pin plastic SOP (375 mil)

Soldering process	Soldering conditions	Recommended conditions
Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or less (at 210 °C or more) Number of reflow processes: 1 Exposure limit[Note]: 3 days (20 hours of pre-baking is required at 125 °C afterward.)	IR30-203-1
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Number of reflow processes: 1 Exposure limit[Note]: 3 days (20 hours of pre-baking is required at 125 °C afterward.)	VP15-203-1
Wave soldering	Solder temperature: 260 °C or less Flow time: 10 seconds or less Number of flow processes: 1 Preheating temperature: 120°C max. (measured on the package surface) Exposure limit[Note]: 3 days (20 hours of pre-baking is required at 125 °C afterward.)	WS60-203-1
Partial heating method	Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for one side of a device)	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: Temperature of 25 °C and maximum relative humidity at 65 % or less

Caution Do not apply more than a single process at once, except for "Partial heating method."

Table 6-2 Soldering Conditions for Through Hole Mount Devices

μPD17P149CT: 28-pin plastic shrink DIP (400 mil)

Soldering process	Soldering conditions
Wave soldering (only for terminals)	Solder temperature: 260 °C or less Flow time: 10 seconds or less
Partial heating method	Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for each terminal)

Caution In wave soldering, apply solder only to the terminals. Care must be taken that jet solder does not come in contact with the main body of the package.

APPENDIX A. μPD17145 SUB-SERIES PRODUCTS LIST

Item \ Product	μPD17145	μPD17147	μPD17149	μPD17P149
ROM	Masked ROM			One-time PROM
	2K bytes (1024 × 16 bits)	4K bytes (2048 × 16 bits)	8K bytes (4096 × 16 bits)	
RAM	110 × 4 bits			
Stack	5 address stacks, 3 interrupt stacks			
Number of I/O ports	23 { • 20 I/O ports • 2 general input ports • 1 sensor input port (INT pin[Note])			
A/D converter input	4 channels (shared with ports) with an absolute accuracy of ±1.5 LSB or less			
Timer	3 channels { • 2 channels for 8-bit timer counter (They can be used together as one 16-bit timer.) • 1 channel for 7-bit basic interval timer (can be used as a watchdog timer)			
Serial interface	1 channel (3-wire type)			
Interrupt	• Up to 3 levels of multiple hardware interrupt • 1 external interrupt (INT) { Detection of the rising edge / Detection of the falling edge / Detection of both edges } Selectable • 4 internal interrupts { • Timer 0 (TM0) • Timer 1 (TM1) • Basic interval timer (BTM) • Serial interface (SIO)			
Execution time of an instruction	2 μs (at fx = 8 MHz with ceramic oscillation)			
Standby function	HALT/STOP			
POC circuit	Mask option (Can be used in an application circuit where V_{DD} is 5 V ±10% and the clock frequency (fx) ranges from 400 kHz to 4 MHz.)			Not provided.
Supply voltage	V_{DD} = 2.7 V to 5.5 V (at fx = 400 kHz to 2 MHz) V_{DD} = 4.5 V to 5.5 V (at fx = 400 kHz to 8 MHz)			
Package	28-pin plastic shrink DIP (400 mil) 28-pin plastic SOP (375 mil)			

Note The INT pin can be used as an input pin (sensor input) when the external interrupt is not used. The status of the pin is read with the INT flag of the control register, not with the port register.

APPENDIX B. DEVELOPMENT TOOLS

The following support tools are available for developing programs for the μPD17P149.

Hardware

Name	Description
In-circuit emulator [IE-17K IE-17K-ET[Note 1] EMU-17K[Note 2]]	The IE-17K, IE-17K-ET, and EMU-17K are in-circuit emulators applicable to the 17K series. The IE-17K and IE-17K-ET are connected to the PC-9800 series (host machine) or IBM PC/AT™ through the RS-232-C interface. The EMU-17K is inserted into the extension slot of the PC-9800 series (host machine). Use the system evaluation board (SE board) corresponding to each product together with one of these in-circuit emulators. *SIMPLEHOST*®, a man machine interface, implements an advanced debug environment. The EMU-17K also enables user to check the contents of the data memory in real time.
SE board (SE-17145)	The SE-17145 is an SE board for the μPD17145 sub-series. It is used solely for evaluating the system. It is also used for debugging in combination with the in-circuit emulator.
Emulation probe (EP-17K28CT)	The EP-17K28CT is an emulation probe for the 17K series 28-pin shrink DIP (400 mil).
Emulation probe (EP-17K28GT)	The EP-17K28GT is an emulation probe for the 17K series 28-pin SOP (375 mil). Use this probe together with the conversion adapter EV-9500GT-28[Note 3], to check the target system with the corresponding SE board.
Conversion adapter (EV-9500GT-28[Note 3])	The EV-9500GT-28 is an adapter for the 28-pin SOP (375 mil). Use this conversion adapter to connect the emulation probe, EP-17K28GT, to the target system.
PROM Programmer [AF-9703[Note 4] AF-9704[Note 4] AF-9705[Note 4] AF-9706[Note 4]]	The AF-9703, AF-9704, AF-9705, and AF-9706 are PROM writers for the μPD17P149. Use one of these PROM writers with the program adapter, AF-9808M, to program the μPD17P149. ★
Programmer adapter[Note 4] (AF-9808M)	The AF-9808M is a socket unit for the μPD17P149. It is used with the AF-9703, AF-9704, AF-9705, or AF-9706.

Notes 1. Low-end model, operating on an external power supply

2. The EMU-17K is a product of I.C Corporation. Contact I.C Corporation. (Tokyo, 03-3447-3793) for details.

3. An EP-17K28GT is supplied together with two EV-9500GT-28s. A set of five EV-9500GT-28s is also available.

4. The AF-9703, AF-9704, AF-9705, and AF-9806 are products of Ando Electric Co., Ltd. Contact Ando Electric Co., Ltd. (Tokyo, 03-3733-1163) for details.

Software

Name	Description	Host machine	OS		Distribution media	Part number
17K series assembler (AS17K)	AS17K is an assembler applicable to the 17K series. In developing μPD17P149 programs, AS17K is used in combination with a device file (AS17145).	PC-9800 series	MS-DOS™		5.25-inch, 2HD	μS5A10AS17K
					3.5-inch, 2HD	μS5A13AS17K
		IBM PC/AT	PC DOS™		5.25-inch, 2HC	μS7B10AS17K
					3.5-inch, 2HC	μS7B13AS17K
Device file (AS17145)	AS17145 is a device file for the μPD17145, μPD17147, and μPD17149. This is used together with the assembler (AS17K) which is applicable to the 17K series.	PC-9800 series	MS-DOS		5.25-inch, 2HD	μS5A10AS17145
					3.5-inch, 2HD	μS5A13AS17145
		IBM PC/AT	PC DOS		5.25-inch, 2HC	μS7B10AS17145
					3.5-inch, 2HC	μS7B13AS17145
Support software (*SIMPLEHOST*)	*SIMPLEHOST*, running on the Windows™, provides man-machine-interface in developing programs by using a personal computer and the in-circuit emulator.	PC-9800 series	MS-DOS	Windows	5.25-inch, 2HD	μS5A10IE17K
					3.5-inch, 2HD	μS5A13IE17K
		IBM PC/AT	PC DOS		5.25-inch, 2HC	μS7B10IE17K
					3.5-inch, 2HC	μS7B13IE17K

Remark The following table lists the versions of the operating systems described in the above table.

OS	Versions
MS-DOS	Ver. 3.30 to Ver. 5.00A[Note]
PC DOS	Ver. 3.1 to Ver. 5.0[Note]
Windows	Ver. 3.0 to Ver. 3.1

Note MS-DOS versions 5.00 and 5.00A and PC DOS Ver. 5.0 are provided with a task swap function. This function, however, cannot be used in these software packages.

Cautions on CMOS Devices

① **Countermeasures against static electricity for all MOSs**

Caution When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins.

Also handle boards on which MOS devices are mounted in the same way.

② **CMOS-specific handling of unused input pins**

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

③ **Statuses of all MOS devices at initialization**

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

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MS-DOS and Windows are trademarks of Microsoft Corporation.

PC/AT and PC DOS are trademarks of IBM Corporation.

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