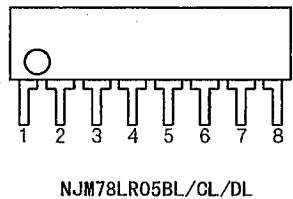
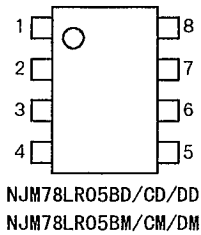
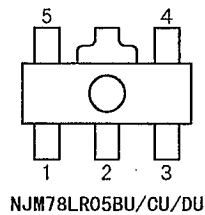


PIN CONFIGURATION



- PIN FUNCTION
- 1. INPUT
 - 2. NC
 - 3. Cd
 - 4. NC
 - 5. GND
 - 6. RESET-OUTPUT
 - 7. NC
 - 8. OUTPUT



- PIN FUNCTION
- 1. Cd
 - 2. GND
 - 3. RESET-OUTPUT
 - 4. OUTPUT
 - 5. INPUT

ABSOLUTE MAXIMUM RATINGS (T a = 25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT
Input Voltage	V IN	+ 2 0	V
Power Dissipation	P D	(DIP8) 5 0 0 (DMP8) 5 0 0※ (SIP8) 8 0 0 (SOT-89) 3 5 0	mW
Operating Temperature Range	T o p r	- 4 0 ~ + 8 5	°C
Storage Temperature Range	T s t g	- 5 0 ~ + 1 5 0	°C

※At on PC board.

RECOMMENDED OPERATING CONDITIONS (T a = 25°C)

PARAMETER	SYMBOL	CONDITIONS	UNIT
Input Voltage	V IN	7. 5 ~ 1 8	V
Output Current	I o	1 ~ 1 0 0	m A

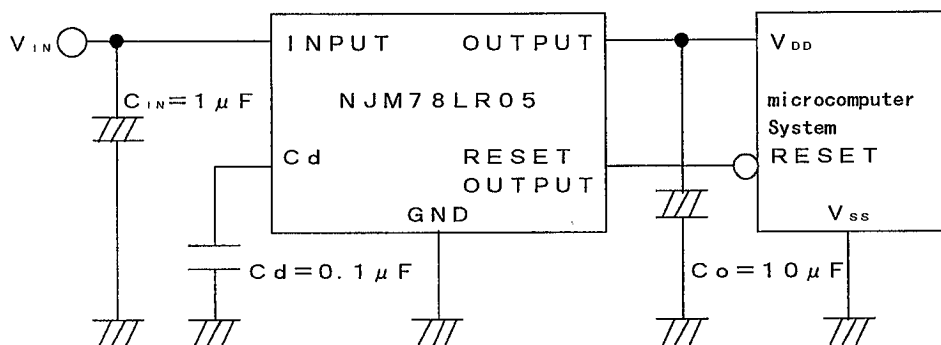
■ ELECTRICAL CHARACTERISTICS ($V_{IN}=10V$, $I_O=40mA$, $C_{IN}=1\mu F$, $C_O=10\mu F$, $T_a=25^\circ C$)
[Power Supply Block]

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_O	$I_O=1mA$	4.80	5.00	5.20	V
Quiescent Current	I_Q	$I_O=100mA$	—	1.40	3.40	mA
Output Short Current	I_{OSC}	OUTPUT-GND short	150	300	450	mA
Line Regulation 1	$\Delta V_O/V_{IN1}$	$7V \leq V_{IN} \leq 18V$	—	6.0	65.0	mV
Line Regulation 2	$\Delta V_O/V_{IN2}$	$8V \leq V_{IN} \leq 18V$	—	3.0	42.0	mV
Load Regulation 1	$\Delta V_O/I_{O1}$	$I_O=1 \sim 100mA$	—	9.0	60.0	mV
Load Regulation 2	$\Delta V_O/I_{O2}$	$I_O=1 \sim 40mA$	—	3.0	30.0	mV
Ripple Rejection	RR	$f=120Hz$, $e_{iL}=1V_{P-P}$, $V_{IN}=8 \sim 18V$	—	79	—	dB
Output Noise Voltage	V_{NO}	$10Hz \leq f \leq 100kHz$, $I_O=1mA$	—	80	—	μV
Dropout Voltage	ΔV_{I-O}		—	1.5	2.2	V

[Reset Block]

(H) Reset Output Voltage	V_{ORH}		4.80	5.00	5.20	V
(L) Reset Output Voltage	V_{ORL}	$V_{IN}=3V$, $I_O=1mA$	—	10	200	mV
Reset Threshold Voltage	V_{RT}	B Version	4.12	4.30	4.48	V
		C Version	4.03	4.20	4.37	
		D Version	3.84	4.00	4.16	
Reset Threshold Hysteresis Voltage	V_{RTH}		50	100	200	mV
Reset Output Delay Time	t_d	$C_d=0.1\mu F$	7.50	10.0	12.5	ms

■ APPLICATION CIRCUIT

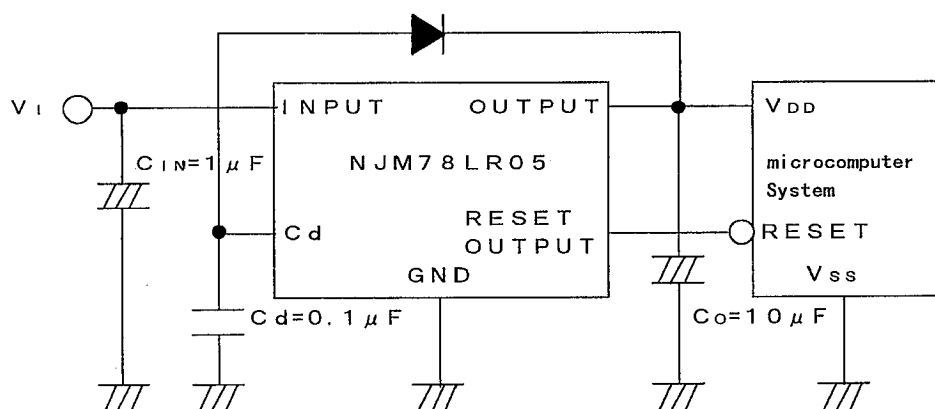


$$t_d [\text{ms}] = 100 \times C_d [\mu\text{F}]$$

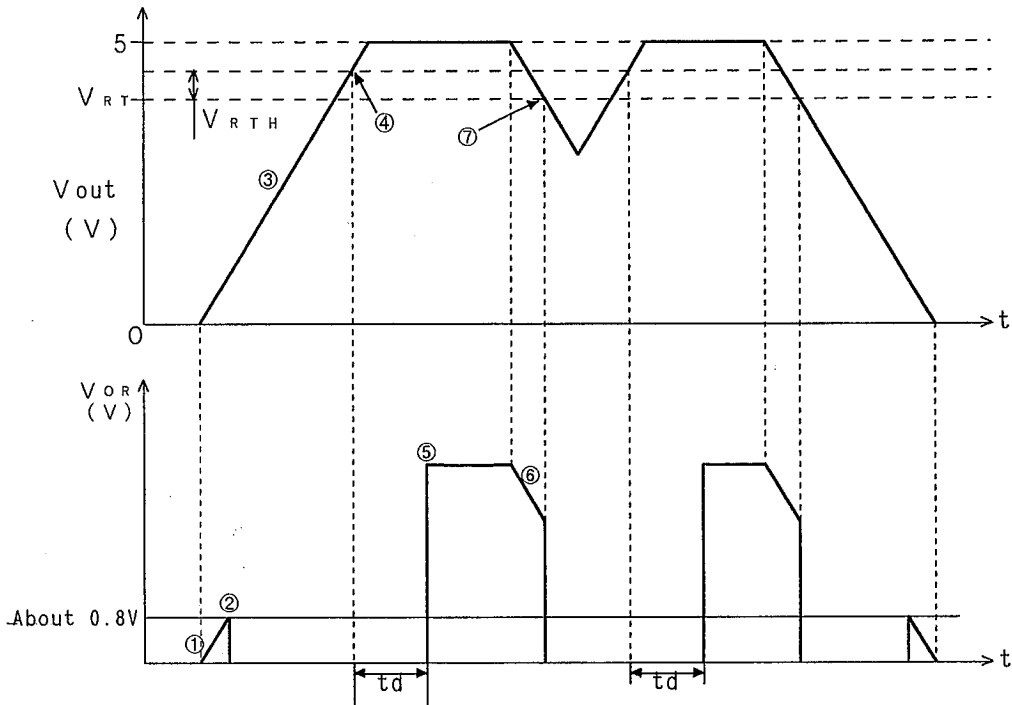
Note1: When the capacitance C_d is too large, the actual delay time is shorter than the calculated result because an electrical charge of C_d is discharged incompletely.

Solution of above problem:

- (1) Connect SBD between output terminal and C_d terminal. Please refer to the following circuit.
- (2) Select larger capacitance, C_{IN} than C_d .

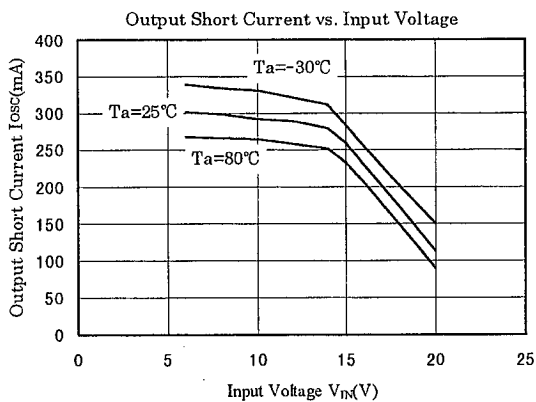
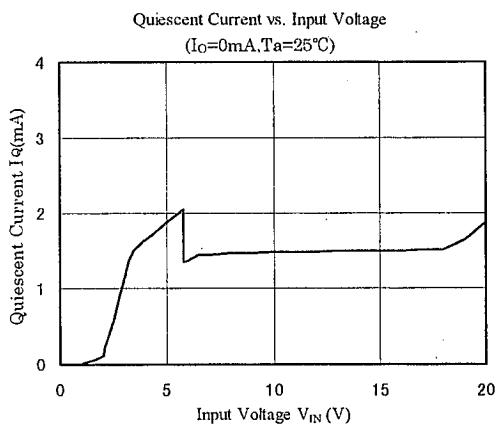
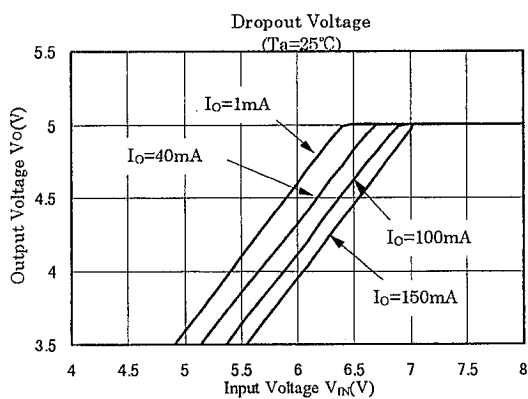
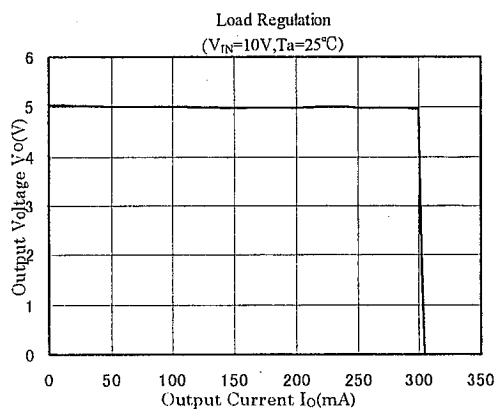
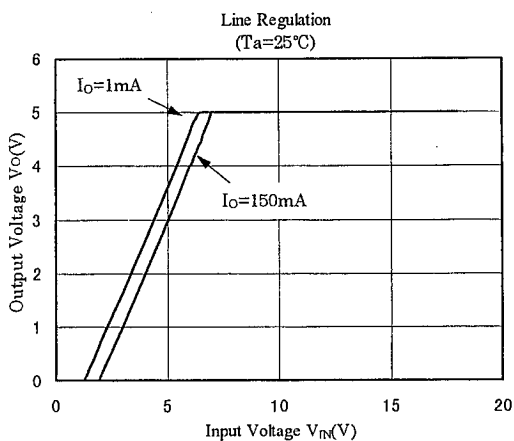
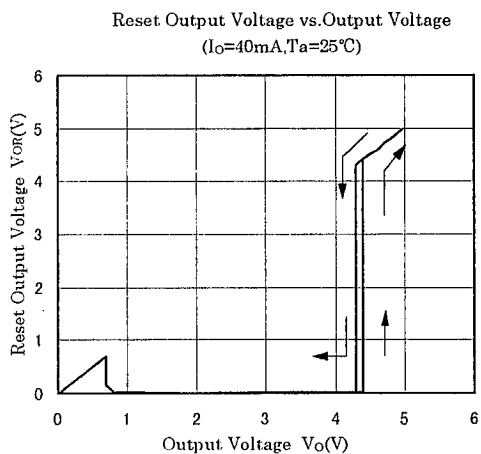


■ TIMING CHART

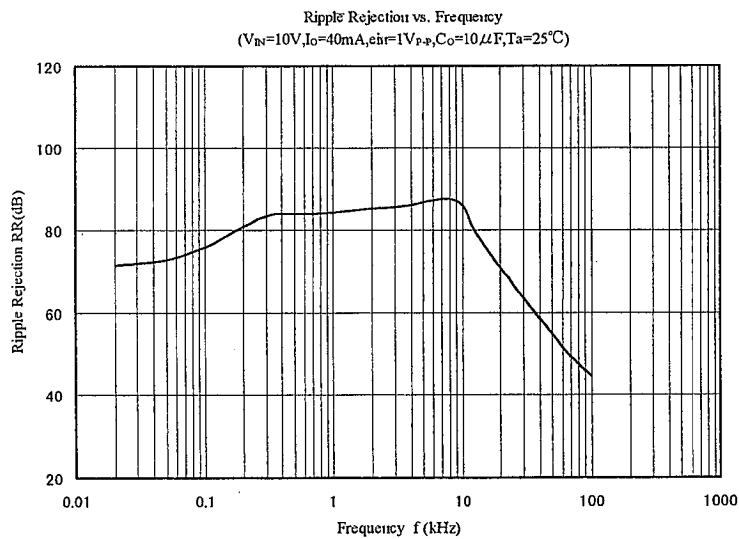
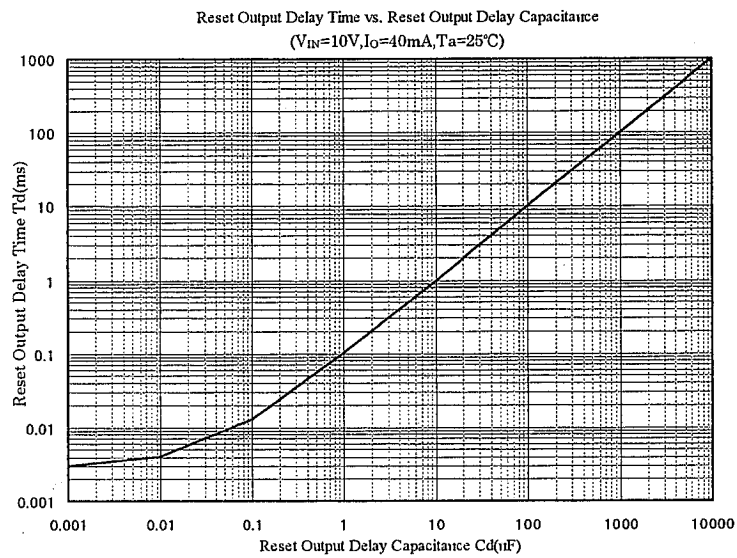


- ① When the input voltage is up to about 0.8V, some voltage is outputted at the reset output because the NJM78LR05 operation is unstable.
- ② When the input voltage goes over about 0.8V, the reset output becomes "L".
- ③ The output voltage is rising up with the input voltage.
- ④ When the output voltage goes over $(V_{RT} + V_{RTH})$, the delay circuit of reset output activates.
 V_{RT} : Reset Threshold Voltage
 V_{RTH} : Reset Threshold Hysteresis Voltage
- ⑤ After the reset output delay time t_d has passed, the reset output becomes "H".
- ⑥ The output voltage is falling down with the input voltage.
- ⑦ When the output voltage is less than V_{RT} , the reset output becomes "L".

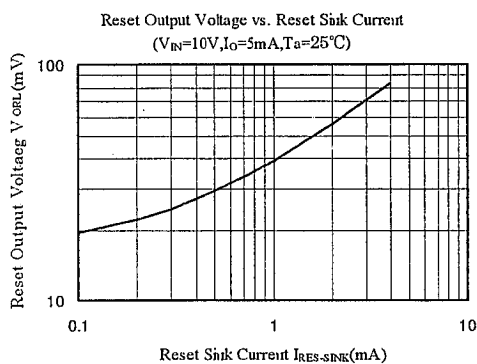
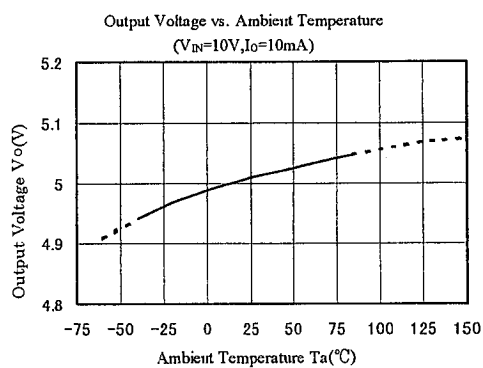
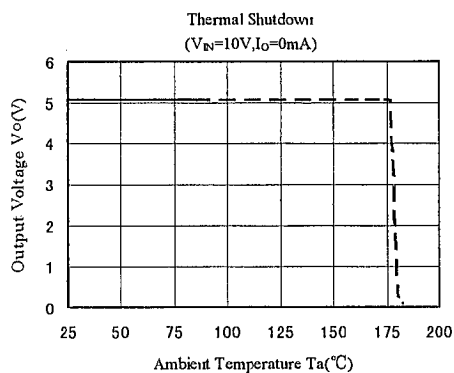
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



MEMO

[CAUTION]

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