



## TPD4E1U06 Quad-Channel, High-Speed ESD Protection Device

### 1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - $\pm 15$ -kV Contact Discharge
  - $\pm 15$ -kV Air-Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 3 A (8/20  $\mu$ s)
- IO Capacitance 0.8 pF (Typical)
- DC Breakdown Voltage 6.5 V (Minimum)
- Ultra Low Leakage Current 10 nA (Maximum)
- Low ESD Clamping Voltage
- Industrial Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Small, Easy-to-Route DCK, and DBV Package

### 2 Applications

- USB 2.0
- Ethernet
- HDMI Control Lines
- MIPI Bus
- LVDS
- SATA

### 3 Description

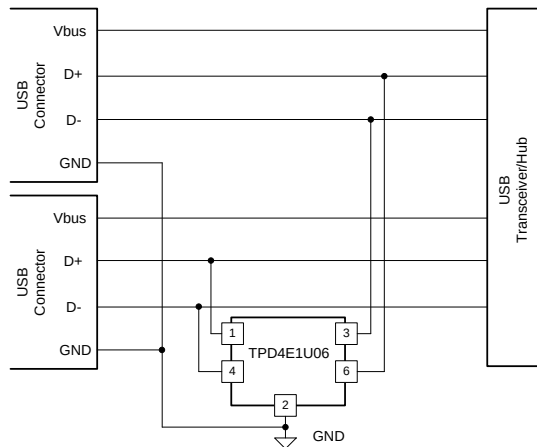
The TPD4E1U06 is a quad-channel unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode with ultra low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. Its 0.8-pF line capacitance makes it suitable for a wide range of applications. Typical application areas include HDMI, USB2.0, MHL, and DisplayPort.

#### Device Information<sup>(1)</sup>

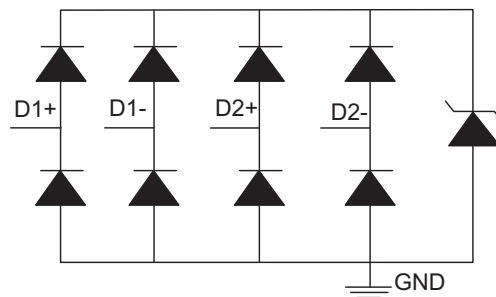
| PART NUMBER  | PACKAGE | BODY SIZE (NOM)          |
|--------------|---------|--------------------------|
| TPD4E1U06DCK | SC70    | 2.00 mm $\times$ 1.25 mm |
| TPD4E1U06DBV | SOT-23  | 2.90 mm $\times$ 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Simplified Schematic**



**Circuit Schematic Diagram**



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## 4 Revision History

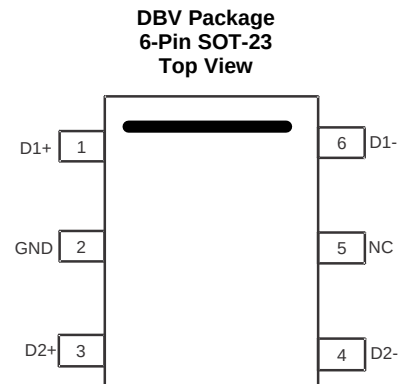
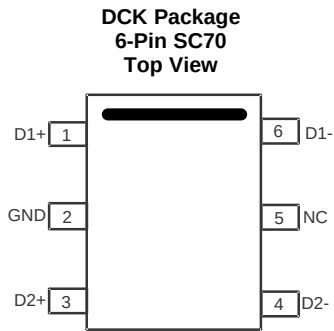
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (October 2014) to Revision D                  | Page |
|-----------------------------------------------------------------------|------|
| • Updated DCK and DBV Pinout image .....                              | 3    |
| • Added 61000-4-5 spec to <i>Absolute Maximum Ratings</i> table ..... | 4    |
| • Added <i>IEC 61000-4-5 Surge Protection</i> section .....           | 8    |
| • Added <i>IEC 61000-4-4 EFT Protection</i> section .....             | 8    |

| Changes from Revision B (February 2013) to Revision C                                                                                                                                                                                                                                                                                                                                                    | Page |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Added <i>Pin Configuration and Functions</i> section, <i>Handling Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | 1    |

| Changes from Revision A (December 2012) to Revision B | Page |
|-------------------------------------------------------|------|
| • Added C <sub>CROSS</sub> data for DBV package.....  | 5    |

## 5 Pin Configuration and Functions



### Pin Functions

| PIN  |     | I/O | DESCRIPTION                                                                       |
|------|-----|-----|-----------------------------------------------------------------------------------|
| NAME | NO. |     |                                                                                   |
| D1+  | 1   | I/O | ESD protected channel. Connect to data line as close to the connector as possible |
| D1–  | 6   | I/O |                                                                                   |
| D2–  | 4   | I/O |                                                                                   |
| D2+  | 3   | I/O |                                                                                   |
| GND  | 2   | GND | Ground. Connect to ground                                                         |
| NC   | 5   | I/O | No connect. Can be left floating, grounded, or connected to VCC                   |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                  |                                                             | MIN | MAX | UNIT |
|------------------|-------------------------------------------------------------|-----|-----|------|
|                  | IEC 61000-4-4 EFT protection (5/50 ns)                      |     | 80  | A    |
| I <sub>PP</sub>  | IEC 61000-4-5 surge protection (8/20 μs) peak pulse current |     | 3   | A    |
| P <sub>PP</sub>  | IEC 61000-4-5 surge protection (8/20 μs) peak pulse power   |     | 45  | W    |
|                  | Operating temperature                                       | –40 | 125 | °C   |
| T <sub>stg</sub> | Storage temperature                                         | –65 | 115 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                                            |                                                                                          | VALUE | UNIT |
|--------------------------------------------|------------------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±4000 | V    |
|                                            | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±1500 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings—IEC Specification

|                                            |                           | VALUE  | UNIT |
|--------------------------------------------|---------------------------|--------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | IEC 61000-4-2 contact ESD | ±15000 | V    |
|                                            | IEC 61000-4-2 air-gap ESD | ±15000 |      |

### 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                 |                                | MIN | MAX | UNIT |
|-----------------|--------------------------------|-----|-----|------|
| V <sub>IO</sub> | Input pin voltage              | 0   | 5.5 | V    |
| T <sub>A</sub>  | Operating free-air temperature | –40 | 125 | °C   |

### 6.5 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TPD4E1U06    |             | UNIT |
|-------------------------------|----------------------------------------------|--------------|-------------|------|
|                               |                                              | DBV (SOT-23) | DCK (SC-70) |      |
|                               |                                              | 6 PINS       | 6 PINS      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 224.3        | 274.3       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 166.1        | 113.8       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 68.4         | 76.7        | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 57.3         | 3.6         | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 67.9         | 75.9        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER              | TEST CONDITIONS                                                                                                                             | MIN | TYP   | MAX   | UNIT     |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|-------|----------|
| $V_{RWM}$              | Reverse stand-off voltage<br>$I_{IO} = 10 \mu A$                                                                                            |     |       | 5.5   | V        |
| $V_{CLAMP}$            | Clamp voltage with ESD strike<br>$I_{PP} = 1 A$ , $t_p = 8/20 \mu s$ , from I/O to GND <sup>(1)</sup>                                       |     | 11    |       | V        |
|                        | $I_{PP} = 3 A$ , $t_p = 8/20 \mu s$ , from I/O to GND <sup>(1)</sup>                                                                        |     | 15    |       | V        |
| $R_{DYN}$              | Dynamic resistance<br>Pin x to GND pin <sup>(2)</sup>                                                                                       |     | 1.0   |       | $\Omega$ |
|                        | GND to pin x                                                                                                                                |     | 0.6   |       |          |
| $C_L$                  | Line capacitance<br>$f = 1 MHz$ , $V_{BIAS} = 2.5 V$ , $25^\circ C$                                                                         |     | 0.8   | 1     | pF       |
| $C_{CROSS}$            | Channel to channel input capacitance<br>Pin 2 = 0 V, $f = 1 MHz$ , $V_{BIAS} = 2.5 V$ , between channel pins                                |     | 0.006 | 0.015 | pF       |
|                        |                                                                                                                                             |     | 0.01  | 0.025 |          |
| $\Delta C_{IO-TO-GND}$ | Variation of channel input capacitance<br>Pin 2 = 0 V, $f = 1 MHz$ , $V_{BIAS} = 2.5 V$ , channel_x pin to ground – channel_y pin to ground |     | 0.025 | 0.07  | pF       |
| $V_{BR}$               | Break-down voltage, IO to GND<br>$I_{IO} = 1 mA$                                                                                            | 6.5 |       | 8.5   | V        |
| $I_{LEAK}$             | Leakage current<br>$V_{IO} = 2.5 V$                                                                                                         |     | 1     | 10    | nA       |

(1) Non-repetitive current pulse 8/20  $\mu s$  exponentially decaying waveform according to IEC61000-4-5.

(2) Extraction of  $R_{DYN}$  using least squares fit of TLP characteristics between  $I = 10 A$  and  $I = 20 A$ .

## 6.7 Typical Characteristics

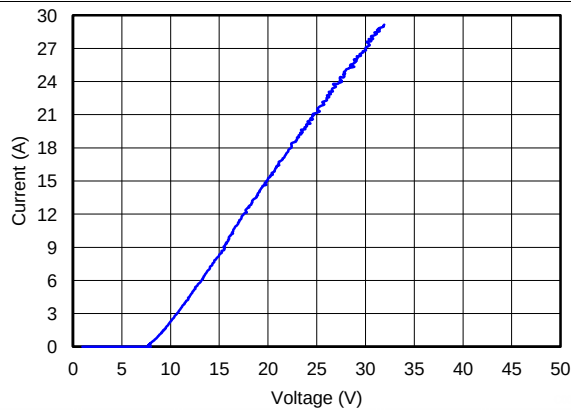


Figure 1. TLP, Data to GND

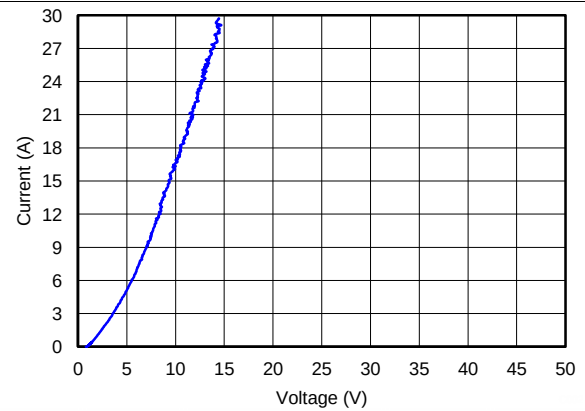


Figure 2. TLP, GND to Data

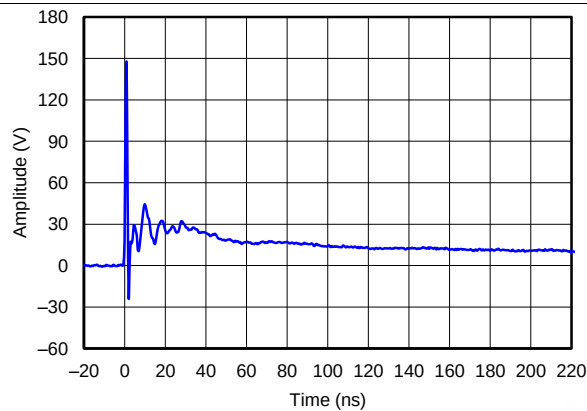


Figure 3. IEC 61000-4-2 Clamping Voltage, 8-kV Contact

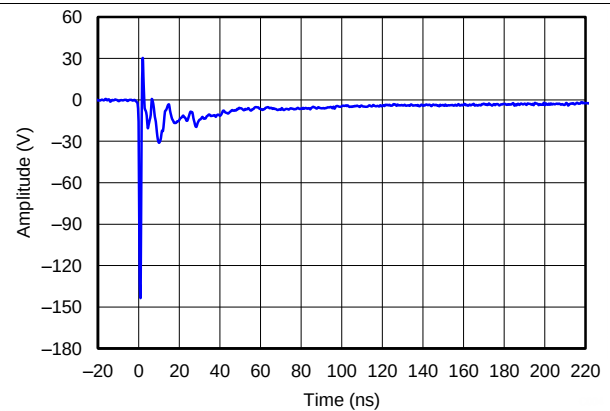


Figure 4. IEC 61000-4-2 Clamping Voltage, -8-kV Contact

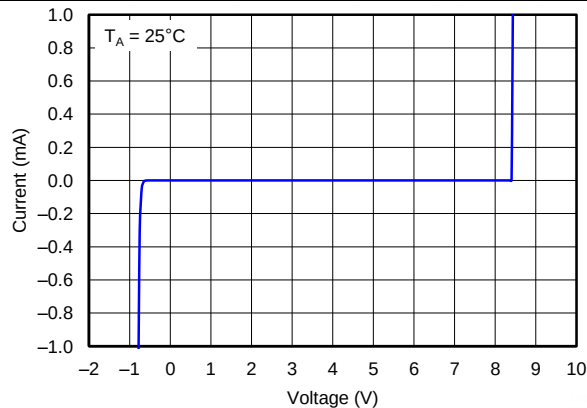


Figure 5. Diode Curve

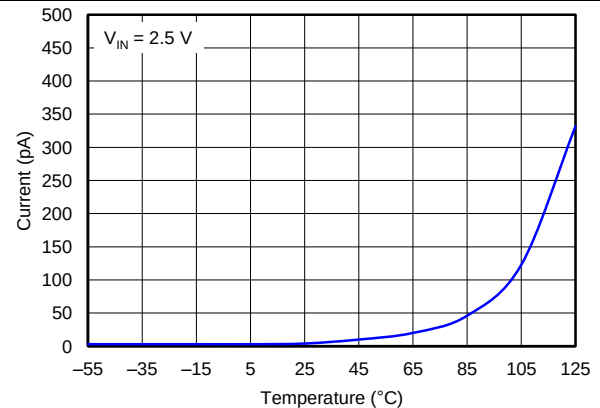
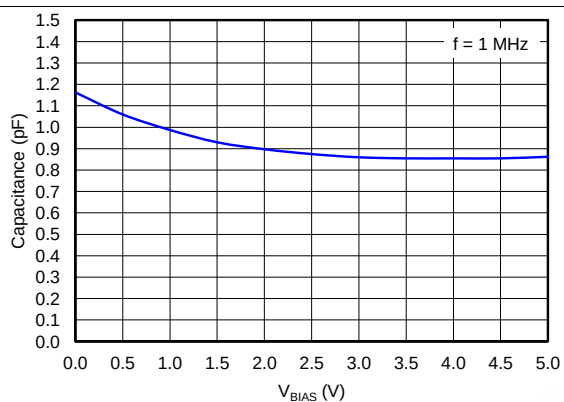
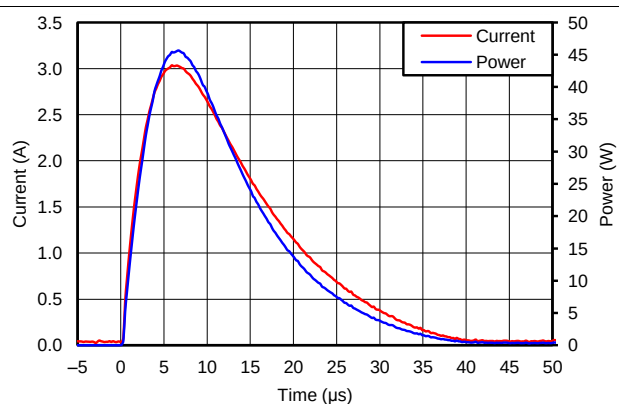


Figure 6. I<sub>LEAK</sub> vs Temperature

## Typical Characteristics (continued)



**Figure 7. Capacitance Across V<sub>BIAS</sub>**



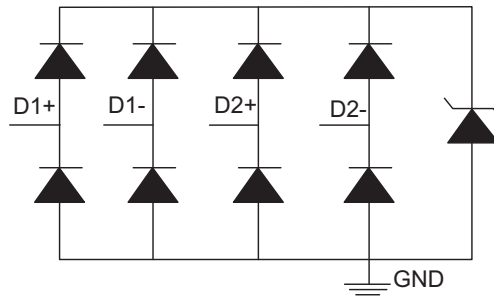
**Figure 8. Surge Curve (tp = 8/20 μs), Pin IO to GND**

## 7 Detailed Description

### 7.1 Overview

The TPD4E1U06 is a quad channel unidirectional TVS ESD protection diode with ultra low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. Typical application areas include HDMI, USB2.0, MHL, and DisplayPort. Its 0.8-pF line capacitance makes it suitable for a wide range of applications.

### 7.2 Functional Block Diagram



**Figure 9. Circuit Schematic Diagram**

### 7.3 Feature Description

#### 7.3.1 IEC 61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to  $\pm 15$ -kV contact and air. An ESD/surge clamp diverts the current to ground.

#### 7.3.2 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 3 A and 45 W (8/20- $\mu$ s waveform). An ESD-surge clamp diverts this current to ground.

#### 7.3.3 IEC 61000-4-4 EFT Protection

The IO pins can withstand an electrical fast transient burst of up to 80 A (5/50-ns waveform, 4 kV with 50- $\Omega$  impedance). An ESD-surge clamp diverts the current to ground.

#### 7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.8 pF.

#### 7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5.5 V.

#### 7.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (Maximum) with a bias of 2.5 V.

#### 7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 11 V ( $I_{PP} = 1$  A).

#### 7.3.8 Industrial Temperature Range

This device features an industrial operating range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .



## **Feature Description (continued)**

### **7.3.9 Small, Easy-to-Route Packages**

The layout of this device makes it simple to add protection to the design. Industry standard packages allow for easy additions to the board and easy layout.

### **7.4 Device Functional Modes**

The TPD4E1U06 is a passive integrated circuit that triggers when voltages are above  $V_{BR}$  or below the forward diode drop. During ESD events, voltages as high as  $\pm 15$  kV can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E1U06 (usually within 10s of nano-seconds) the device reverts to passive.

## 8 Application and Implementation

### NOTE

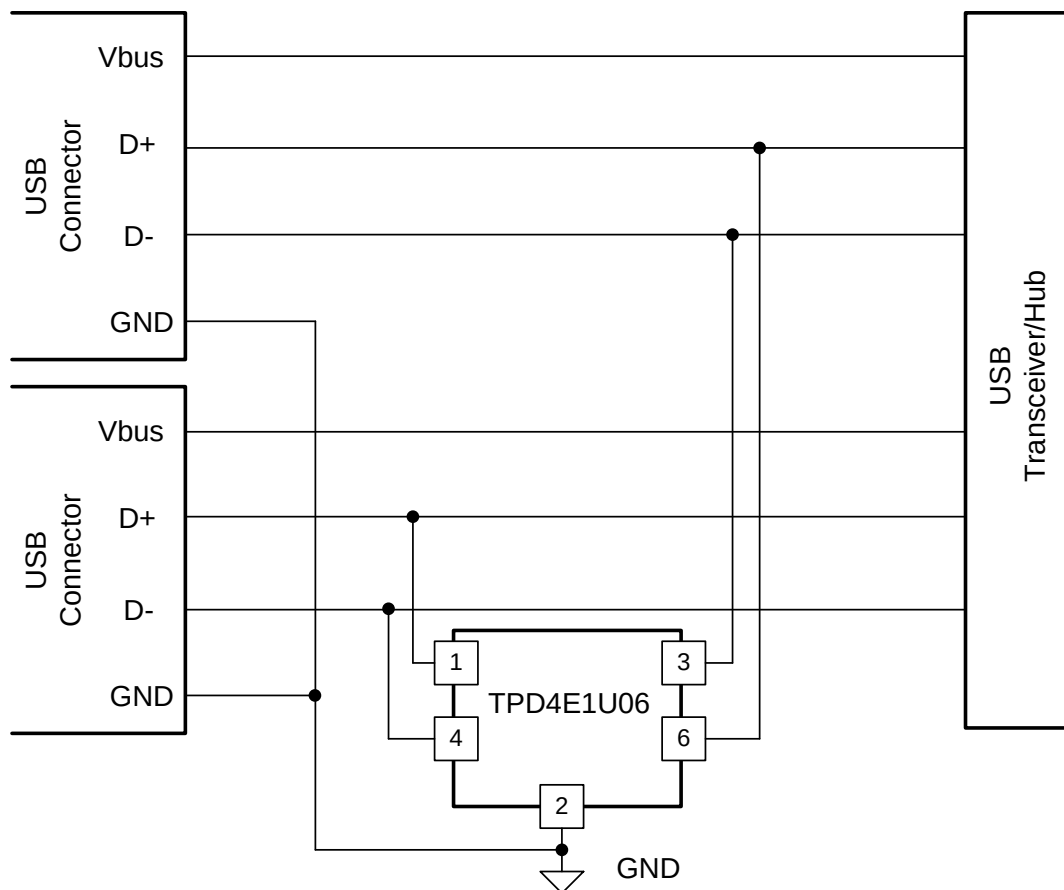
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPD4E1U06 is a TVS diode array which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage,  $V_{CLAMP}$ , to a safe level for the protected IC.

### 8.2 Typical Application

For this design example, one TPD4E1U06 device is being used in a dual USB 2.0 application. This provides a complete port protection scheme.



**Figure 10. Dual USB 2.0 Application**

## Typical Application (continued)

### 8.2.1 Design Requirements

Given the USB 2.0 application, the parameters in [Table 1](#) are known.

**Table 1. Design Parameters**

| DESIGN PARAMETER                   | VALUE      |
|------------------------------------|------------|
| Signal range on pins 1, 3, 4, or 6 | 0 V to 5 V |
| Operating frequency                | 240 MHz    |

### 8.2.2 Detailed Design Procedure

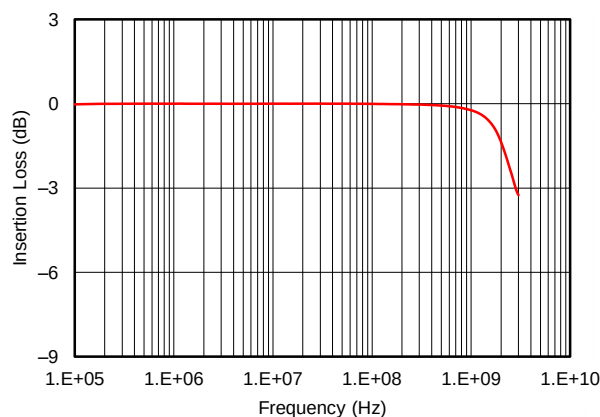
#### 8.2.2.1 Signal Range on Pins 1, 3, 4, or 6

The TPD4E1U06 has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 I/O channels protect which signal lines. Any I/O supports a signal range of 0 to 5.5 V.

#### 8.2.2.2 Operating Frequency

The TPD4E1U06 has a capacitance of 0.8 pF (typical), supporting USB 2.0 data rates.

### 8.2.3 Application Curve



**Figure 11. Insertion Loss Graph**

## 9 Power Supply Recommendations

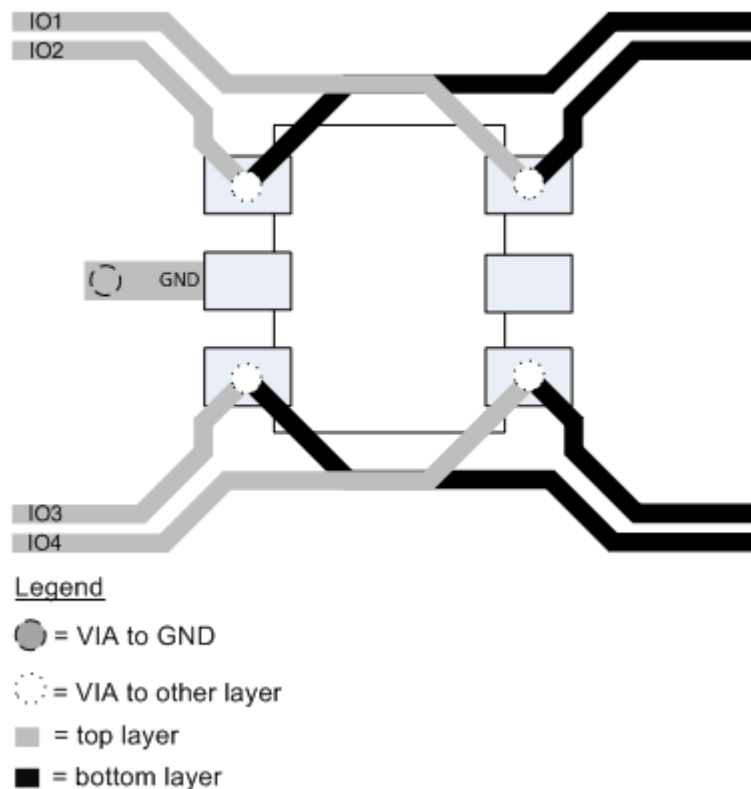
This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (0 V to 5.5 V) to ensure the device functions properly.

## 10 Layout

### 10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

### 10.2 Layout Example



**Figure 12. PCB Layout Recommendation**

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- [Reading and Understanding an ESD Protection Datasheet](#)
- [ESD Layout Guide](#)
- [TPD4E1U06DCK EVM User's Guide](#)
- [TPD4E1U06DBV EVM User's Guide](#)

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](#). In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                |
|-------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------------|
| <a href="#">TPD4E1U06DBVR</a> | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | (NG4, NG4P)                        |
| TPD4E1U06DBVR.B               | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | (NG4, NG4P)                        |
| <a href="#">TPD4E1U06DCKR</a> | Active        | Production           | SC70 (DCK)   6   | 3000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | (BP6, BP8, BPI)<br>(BPP, BPP, BPS) |
| TPD4E1U06DCKR.B               | Active        | Production           | SC70 (DCK)   6   | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | (BP6, BP8, BPI)<br>(BPP, BPP, BPS) |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

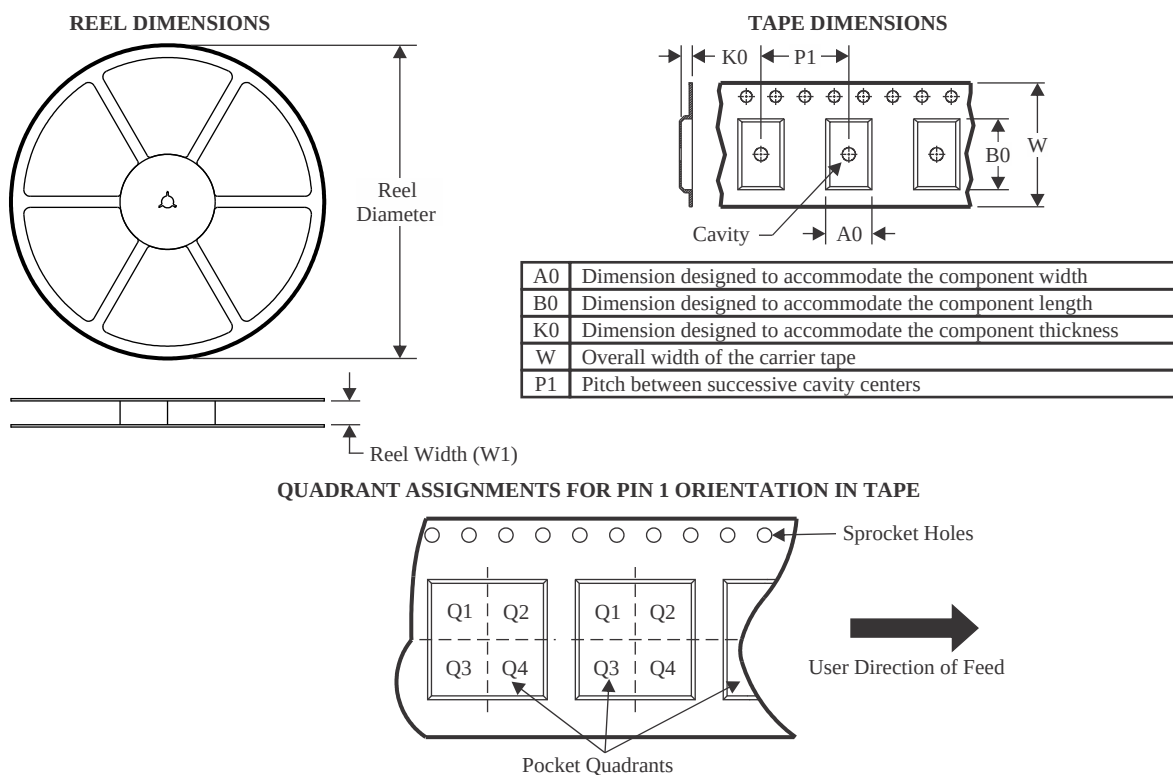
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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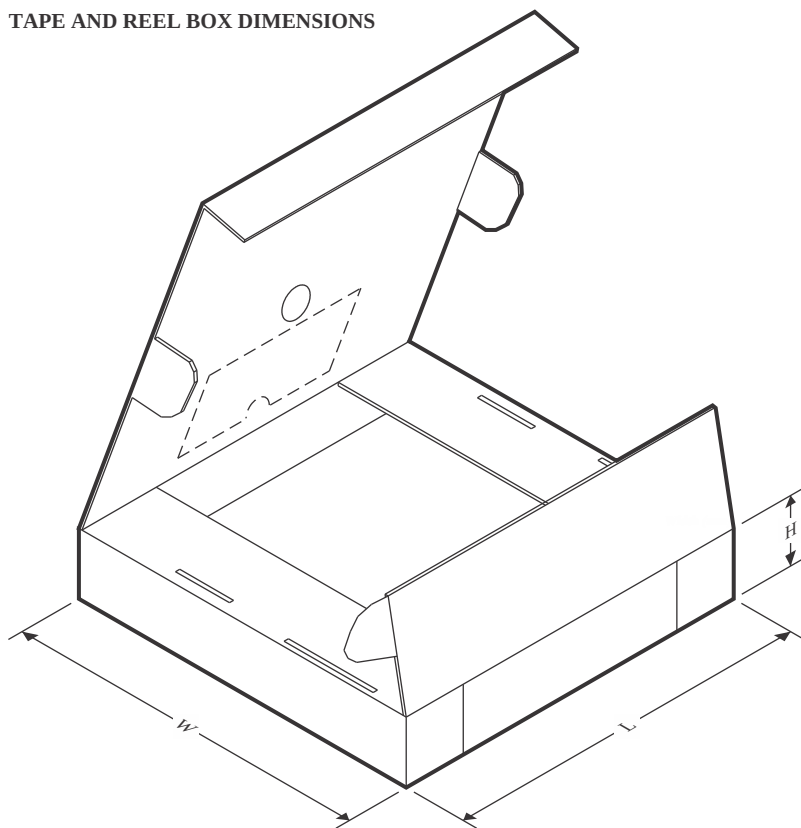
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPD4E1U06DBVR | SOT-23       | DBV             | 6    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TPD4E1U06DCKR | SC70         | DCK             | 6    | 3000 | 180.0              | 8.4                | 2.3     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPD4E1U06DBVR | SOT-23       | DBV             | 6    | 3000 | 210.0       | 185.0      | 35.0        |
| TPD4E1U06DCKR | SC70         | DCK             | 6    | 3000 | 210.0       | 185.0      | 35.0        |





## SOT-23 - 1.45 mm max height

## SMALL OUTLINE TRANSISTOR



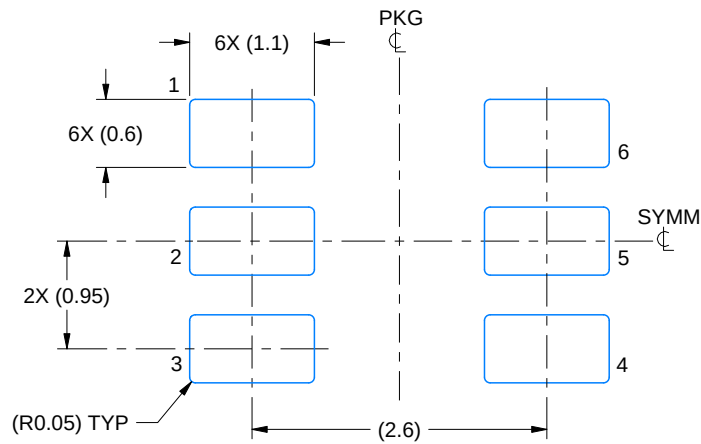
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

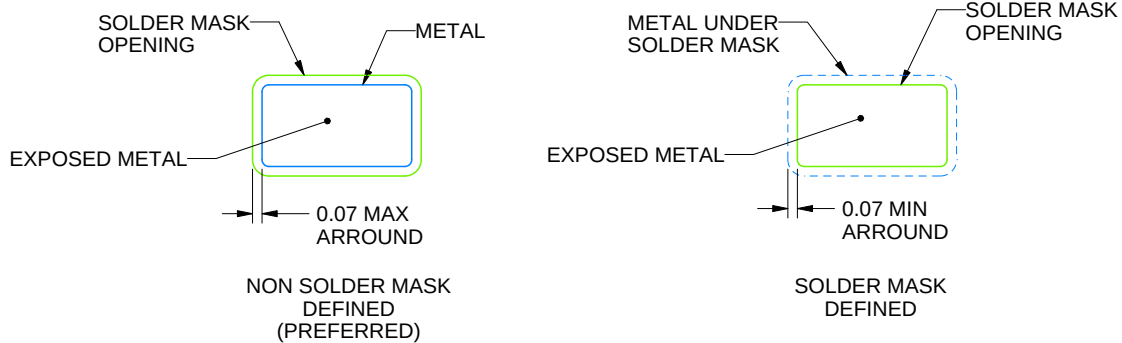
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

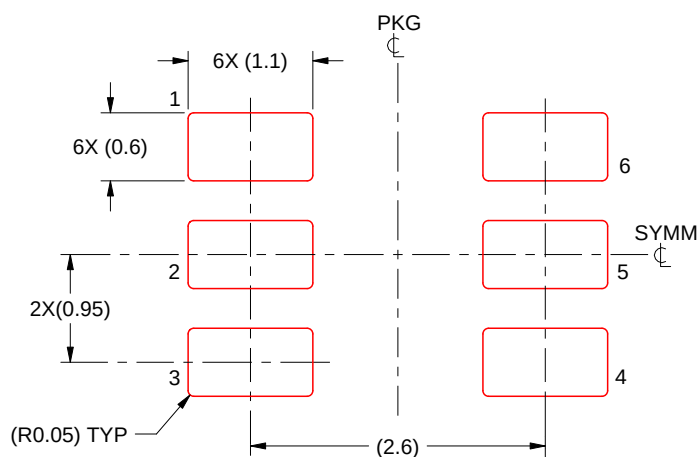
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

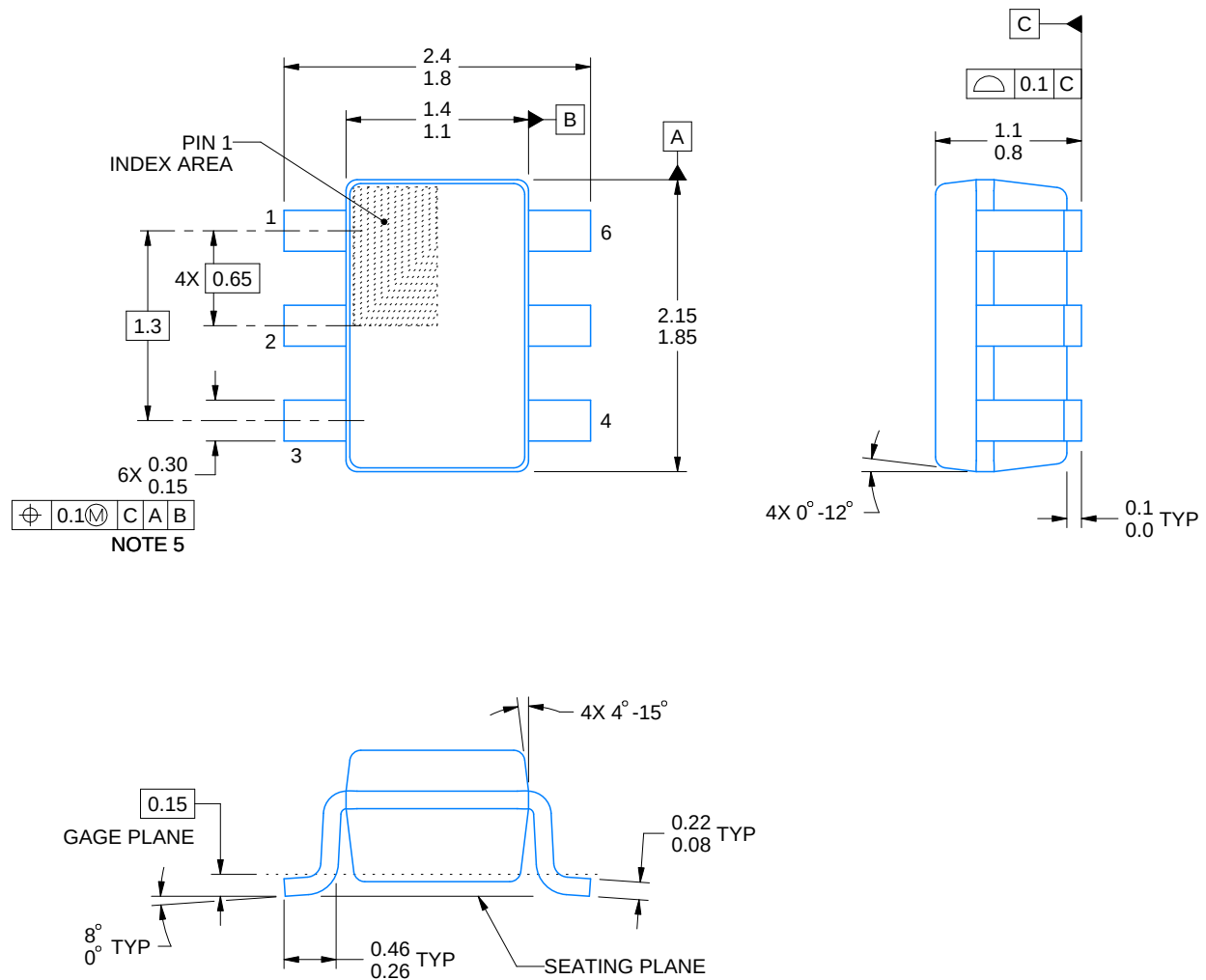


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

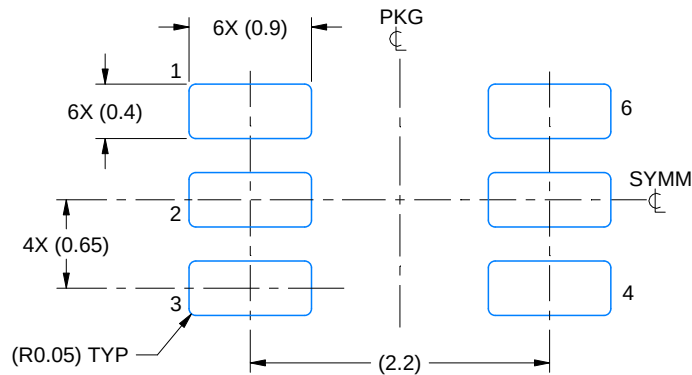
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



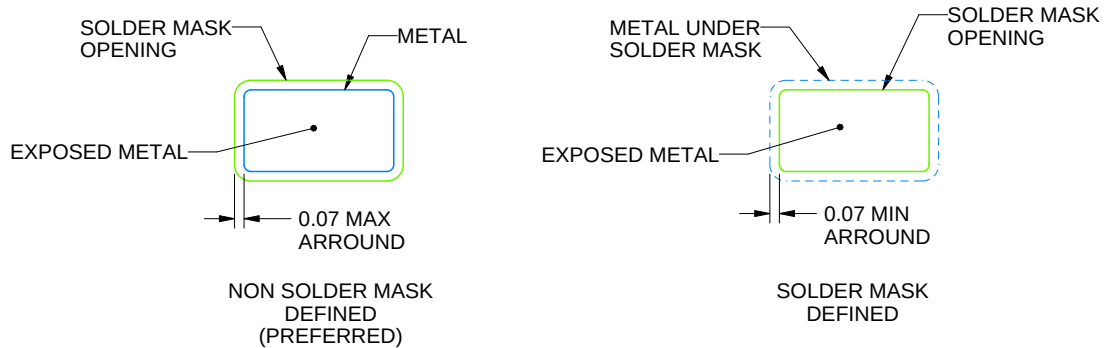
4214835/D 11/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

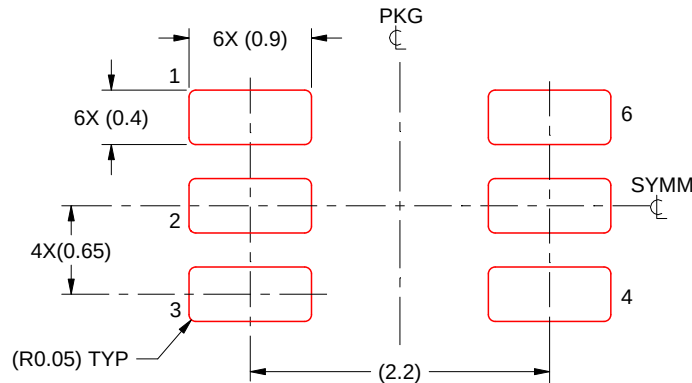


## SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.  
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 THICK STENCIL  
 SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025