To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD16876

SINGLE Pch HIGH-SIDE SWITCH FOR USB

DESCRIPTION

The μPD16876 is a power switch IC with an overcurrent limiter that is used for the power bus of a Universal Serial Bus (USB). This product has one Pch power MOSFET circuits, which has a low-on resistance (100 mΩ TYP.), in its switching block. This product boasts an operating current consumption of as low as 100 μA (MAX.).

In addition, the IC is also equipped with an overcurrent detector that is essential for a host/hub controller conforming to the USB Standard, so that the IC can report an overcurrent to the controller. Moreover, a thermal shutdown circuit and an undervoltage lockout circuit are also provided as the protection circuits of the IC.

This product has one channel of power switch, control input pin, and flag output pin to simultaneously control one USB port with a single IC.

FEATURES

- One P-ch power MOSFET circuit
- Overcurrent detector that outputs active-low control signal from detection report pin
- Overcurrent limiter to prevent system voltage drop
- Thermal shutdown circuit
- Undervoltage lockout circuit
- This control circuit can be turned on and off independently of the others by a control pin.
- 8-pin SOP package

ORDERING INFORMATION

Part Number	Package
μPD16876G	8-pin SOP (5.72 mm (225))

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

Document No. S14288EJ1V0DS00 (1st edition)
Date Published April 2001 N CP(K)
Printed in Japan

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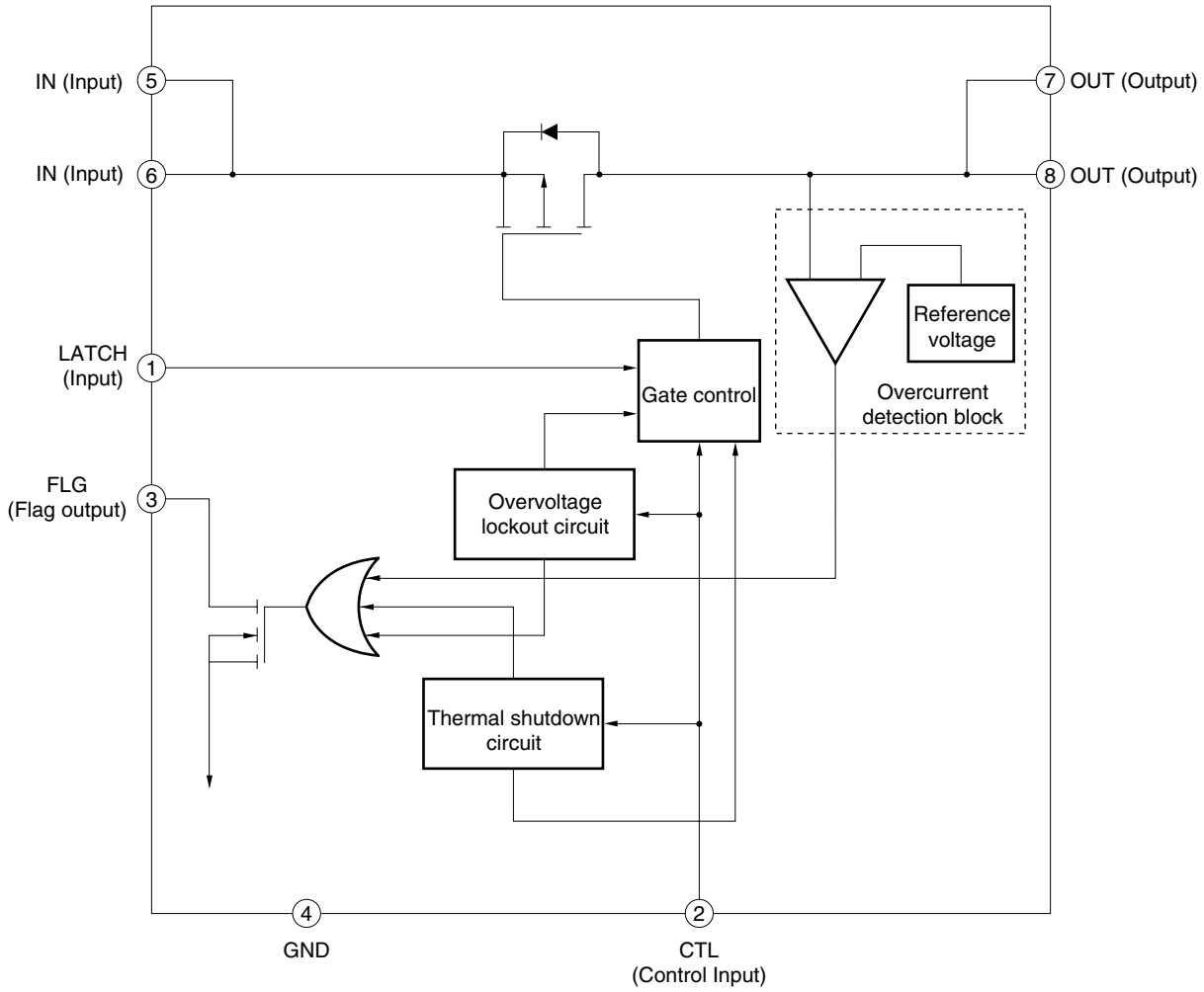
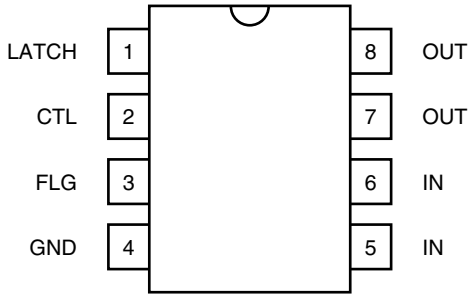
BLOCK DIAGRAM



NOTES ON CORRECT USE

- No internal resistor is connected to input pins LATCH (pin 1) and CTL (pin 2). When using the μPD16876, therefore, be sure to set the voltage level of these input pins to “H” or “L”.
- Plural terminal (IN, OUT) is not only 1 terminal and connect all terminals.

PIN CONFIGURATION (Top View)



8-pin SOP

PIN DESCRIPTION

Pin No.	Pin Name	Pin Function
1	LATCH	Select LATCH function. “H” is effective LATCH function.
2	CTL	Control input: Active-low, TTL input
3	FLG	Detection flag (output): Active-low, Nch open-drain
4	GND	Ground
5/6	IN	Power input: Source of MOSFET for output. Power supply to internal circuitry of IC
7/8	OUT	Switch output: Drain of MOSFET for output. Usually, connected to load.

TRUTH TABLE (H: High level, L: Low level, ON: Output on, OFF: Output off, X: H or L)

CTL (In)	FLG (Out)	OUT (Out)	Operation mode
L	H	ON	Normal operation
H	H	OFF	Switch OFF/Stand by mode
L	L	ON	Overcurrent detection
X	L	OFF	Thermal shutdown circuit operation
X	L	OFF	Undervoltage lockout circuit operation

LATCH	Operation mode
H (LATCH mode)	After overcurrent detection circuit operates, output is latched.
L (non LATCH mode)	After overcurrent detection circuit operates, output is operated limited current function.

ABSOLUTE MAXIMUM RATINGS (Unless otherwise specified, T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V_{IN}		−0.3 to +6	V
Flag voltage	V_{FLG}		−0.3 to +6	V
Flag current	I_{FLG}		50	mA
Output voltage	V_{OUT}		V_{IN}+0.3	V
Output current	I_{OUT}	DC	+0.5 (V_{IN} = V_{CTL} = 5 V) −0.1 (V_{IN} = 0 V, V_{OUT} = 5 V)	A
		Pulse width ≤ Single 100 μs pulse	+3	
Control input	V_{CTL}		−0.3 to +6	V
Total power dissipation	P_D		300	mW
Operating temperature range	T_A		−40 to +85	°C
Junction temperature[Note]	$T_{CH\ MAX}$		+150	°C
Storage temperature	T_{stg}		−55 to +150	°C

Note This product has an internal thermal shutdown circuit (operating temperature: 150°C or higher TYP.)

RECOMMENDED OPERATING RANGE (Unless otherwise specified, T_A = 25°C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Input voltage	V_{IN}	+3		+5.5	V
Operating temperature range	T_A	0		+70	°C

ELECTRICAL SPECIFICATIONS

DC Characteristics (Unless otherwise specified, V_{IN} = +5 V, T_A = +25°C)

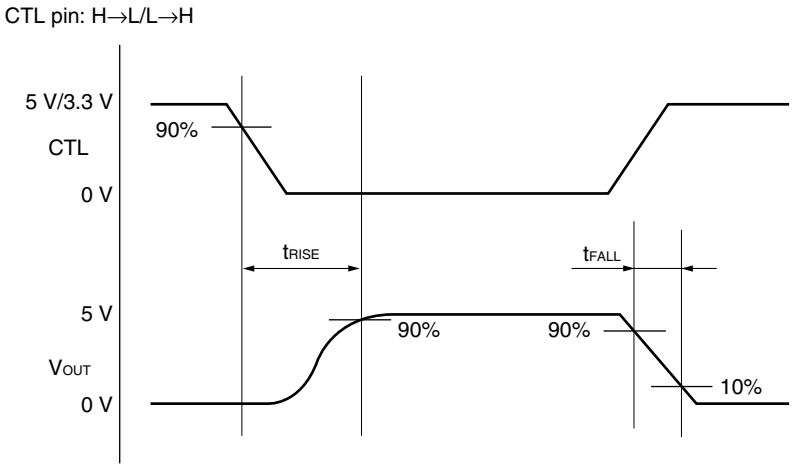
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Current consumption	I_{DD}	V_{CTL} = V_{IN}, OUT: Open		1	5	μA
		V_{CTL} = 0 V, OUT: open			80	μA
Input voltage, low	V_{IL}	CTL pin			1.0	V
Input voltage, high	V_{IH}	CTL pin	2.0			V
LATCH input voltage, low	V_{IL}	LATCH pin			1.5	V
LATCH input voltage, high	V_{IH}	LATCH pin	3.5			V
Control input current	I_{CTL}	V_{CTL} = 0 V		0.01	1	μA
		V_{CTL} = V_{IN}		0.01	1	μA
Output MOSFET on-resistance	R_{ON}	T_A = 0 to +70°C, I_{OUT} = 500 mA		100	140	mΩ
		V_{IN} = 3 to 5 V, T_A = 0 to 70°C I_{OUT} = 500 mA			200	mΩ
Output leakage current	$I_{O\ LEAK}$				10	μA
Overcurrent detector threshold	I_{TH}	T_A = 0 to +70°C	0.6	0.9	1.25	A
		V_{IN} = 3 to 5 V, T_A = 0 to 70°C	0.5		1.25	A
Flag output resistance	$R_{ON\ F}$	I_L = 10 mA		10	25	Ω
Flag leakage current	$I_{O\ LEAK\ F}$	V_{FLAG} = 5 V		0.01	1	μA
Undervoltage lockout circuit operating voltage	V_{UVLO}	V_{IN}: When rising	2.2	2.5	2.8	V
		V_{IN}: When falling	2.0	2.3	2.6	V
		Hysteresis width	0.05		0.25	V

AC Characteristics (Unless otherwise specified, V_{IN} = +5 V, T_A = +25°C)

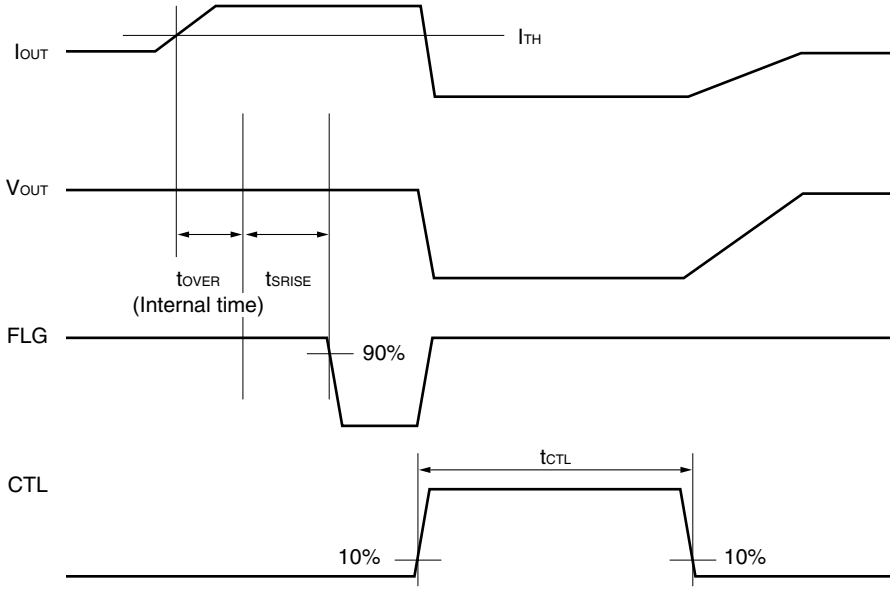
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output transition rise time (ON)	t_{RISE}	R_L = 10 Ω per output	2.5	5	8	ms
Output transition fall time (OFF)	t_{FALL}	R_L = 10 Ω per output			10	μs
Overcurrent detection delay time	t_{OVER}			20		μs
Overcurrent detection output rise time	t_{SRISE}	R_L = 10 Ω per output	2.5	5	8	ms
Minimum CTL high time	t_{CTL}	CTL : L→H→L	20			μs
CTL → FLG Delay time	$t_{C\text{-}F\ Delay}$	Over Current Detect CTL1 → FLG4		10		μs

POINTS OF MEASUREMENT

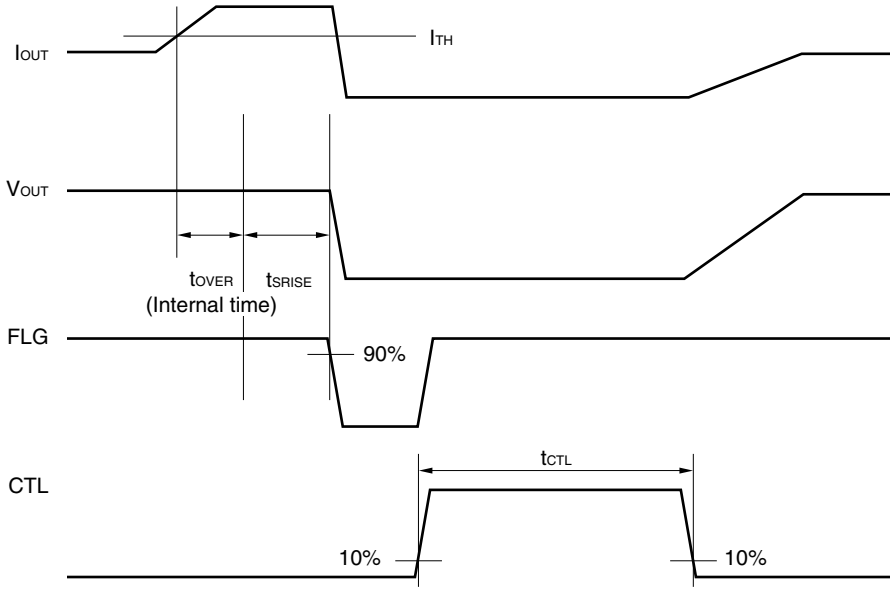
Output Transition Rise Time (ON)/Output Transition Fall Time (OFF)



Overcurrent Detection Delay Time/Minimum CTL High Time (LATCH = "L")



Overcurrent Detection Delay Time/Minimum CTL High Time (LATCH = "H")



FUNCTIONAL DESCRIPTION REFERENCE TABLE

Function	Characteristics	Reference Value (TYP.)		Refer to:
Overcurrent detection	Overcurrent detection Threshold	0.9 A		p.8 1. Overcurrent detection
	Overcurrent detection delay time	20 μs		p.8 1. Overcurrent detection p.11 On Detection of Overcurrent
	Slow-start repeat time	5 ms		p.11 On Detection of Overcurrent
Under voltage lockout circuit (UVLO)	UVLO operating voltage	V_{DD} L→H	2.5 V	p.8 2. Under Voltage Lockout Circuit (UVLO)
		V_{DD} H→L	2.3 V	
Operation when power is turned on/off	Output rise time	t_{RISE}	5 ms	p.9 3. Behavior When Power Is Turned ON/OFF
	Output fall time	t_{FALL}	1 μs	
Thermal shutdown circuit	Thermal shutdown circuit operating temperature	150°C or higher		p.12 When Thermal Shutdown Circuit Operates

DESCRIPTION OF FUNCTIONS

1. Overcurrent Detection

This IC detects an overcurrent in a range of 0.6 to 1.25 A (0.9 A TYP.) (the USB Standard defines that an overcurrent is 0.5 A MAX.). When the IC detects an overcurrent, the FLG pin goes low (active) and reports the result of detection to the control IC. At this time, the switch is kept ON and the current limiter is activated. In this way, an overcurrent status that lasts for a long time can be prevented.

By deasserted the CTL pin inactive by the control IC, the switch is turned OFF and the FLG pin goes back high. Therefore, the CTL signal must be deasserted inactive as soon as the controller IC has detected that the FLG pin has gone low, to avoid overheating this IC. Once the switch has been turned OFF, it turns back ON again only when the CTL signal is asserted active while the FLG pin is high.

To prevent an inrush current being detected by mistake, a deadband time (overcurrent detection delay time) is set to elapse before the overcurrent detector is activated. The duration of this deadband time is 20 μs TYP.

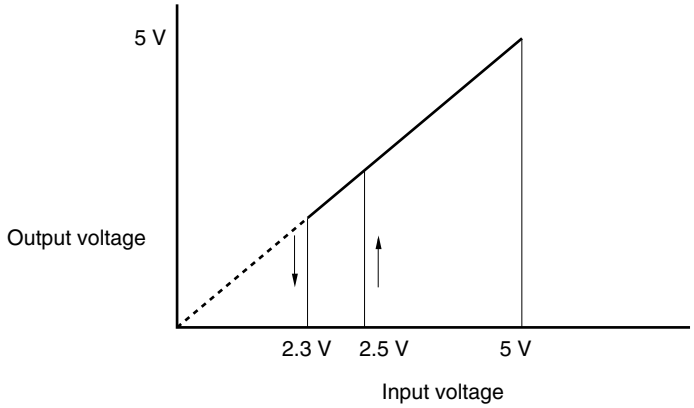
While the overcurrent limiter is activated, the power consumption of the device may abruptly increase. As a result, the junction temperature may also rise. Make sure that the CTL signal is deasserted inactive and that the switch is turned OFF before the absolute maximum rating is exceeded.

2. Undervoltage Lockout Circuit (UVLO)

This circuit prevents malfunctioning of the switch due to fluctuation in supply voltage.

When power is turned on (2.5 V or less TYP.) or off (2.3 V or less TYP.), the OUT and FLG pins have the following status:

OUT: OFF
FLG: “L” (= 0 V)



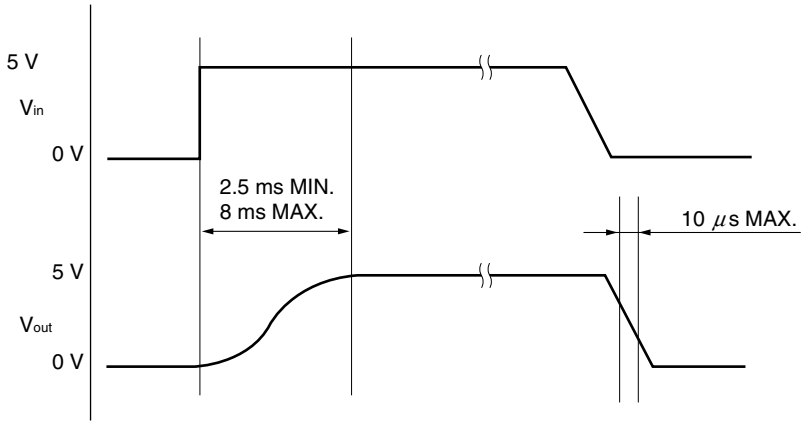
The above figure does not show the actual waveform. For the related characteristic waveform, refer to Major Characteristic Curves.

3. Behavior When Power Is Turned ON/OFF

This IC performs a soft-start operation on power application. This is to prevent an overcurrent from flowing through the IC on power application while the high-capacity capacitor connected to the output pin is charged.

Power ON: Soft start (2.5 to 8 ms)

Power OFF: No control (10 μs MAX.)



The above figure does not show the actual waveform. For the related characteristic waveform, refer to Major Characteristic Curves.

4. Output Latch Functional Change

LATCH = "H": This IC has the control terminal (LATCH terminal) which latches the output current limitation after over current detection.

An output latch function is explained below.

The output switch is turned off irrespective of the state of a CTL terminal after over current detection.

Again, in order to make a switch into an ON state, it is necessary that a CTL terminal is setting to Low level.

This function can be used, when you want to make a CTL terminal "L" fixation and to always consider as an ON state, or when a USB controller to switch-ON/OFF control is unnecessary.

LATCH = "L": A current limitation circuit operates after over current detection.

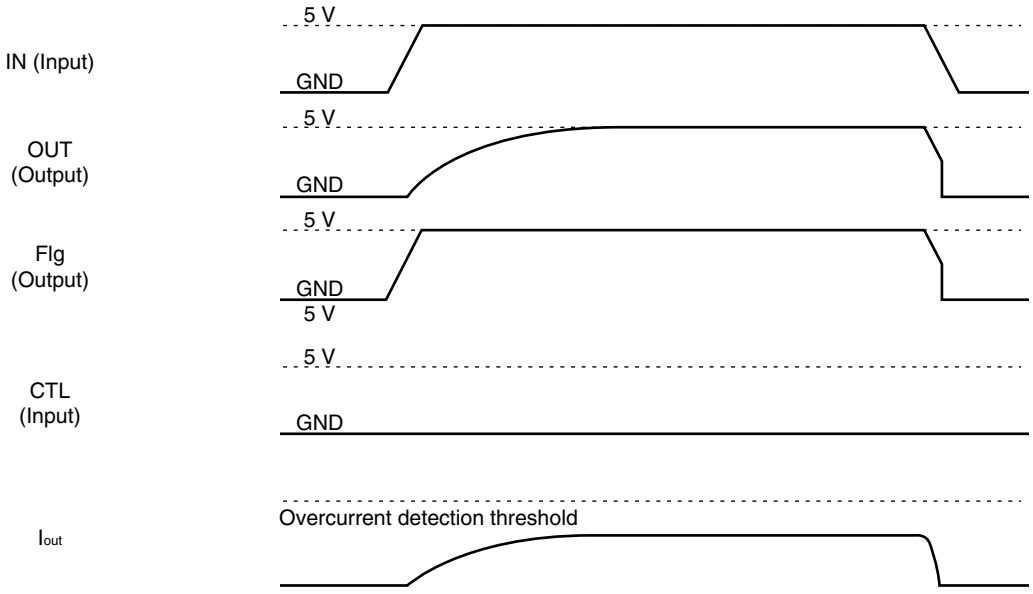
A limitation function is continued until the over current is eliminated.

After current detection, when abnormal condition is eliminated, output returns to an ON state.

This function serves as specification which suited USB specification.

OPERATION SEQUENCE

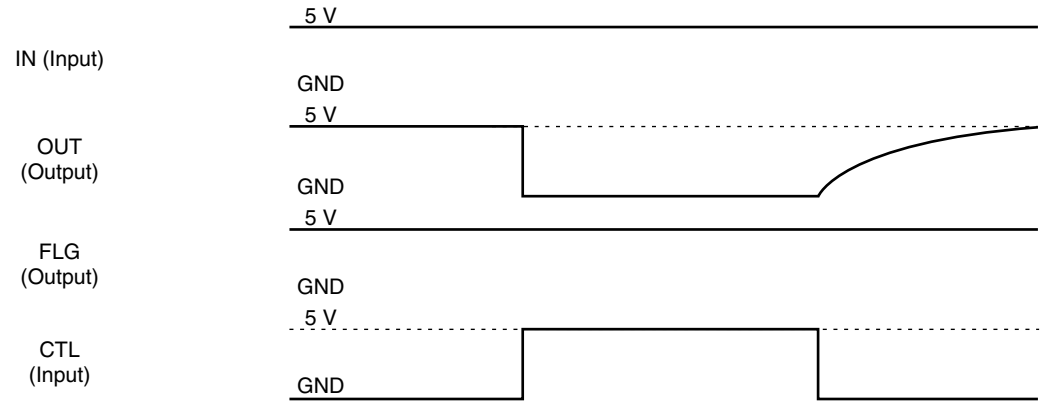
Power ON/OFF



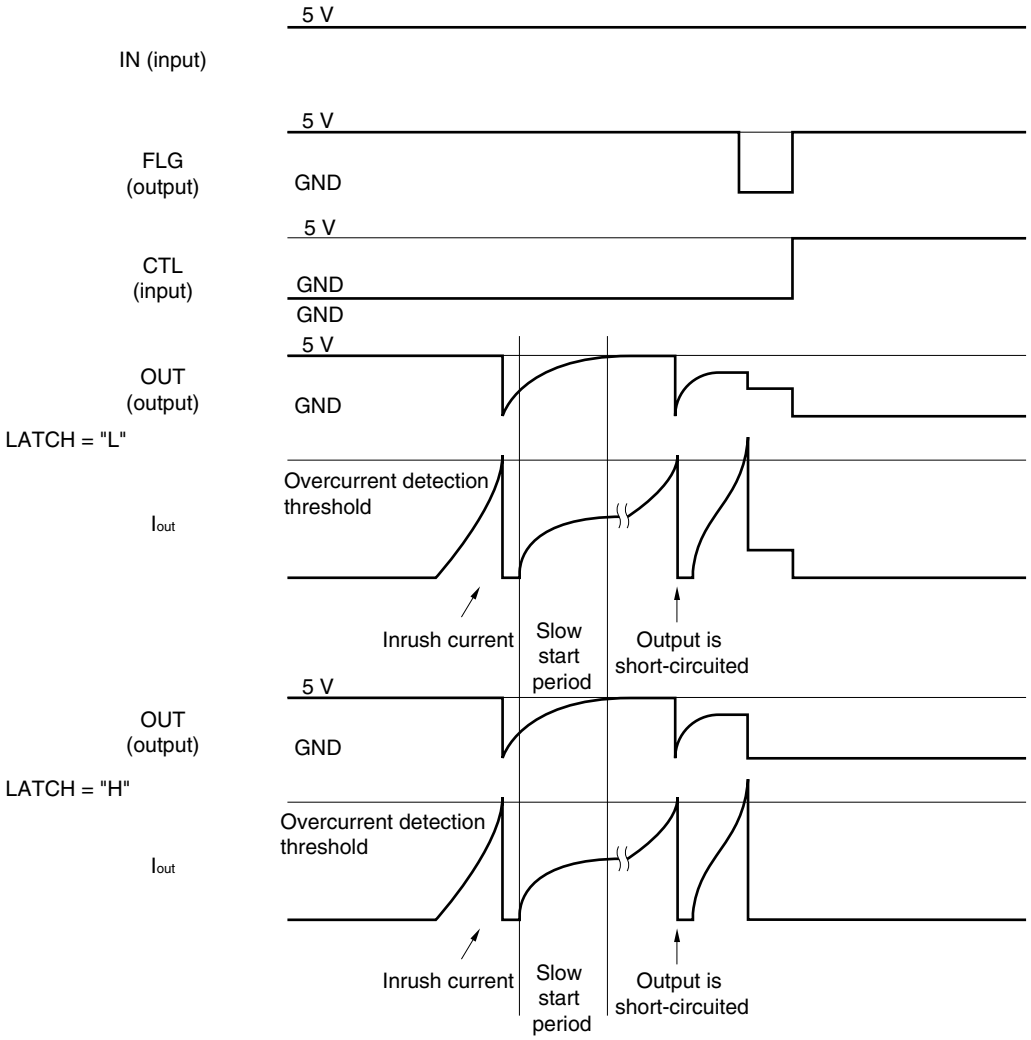
If the CTL signal is asserted active after power has been turned ON, OUT executes the soft-start operation (output transition time: 8 ms MAX.). In addition, FLG output is fixed to "L" if the supply voltage is lower than the operating voltage of the undervoltage lockout circuit (UVLO) on power application.

If all the CTL pins are inactive when power is supplied, the IC enters the standby status (IDD = 5 μA MAX.).

When Control Signals Are Input



On Detection of Overcurrent

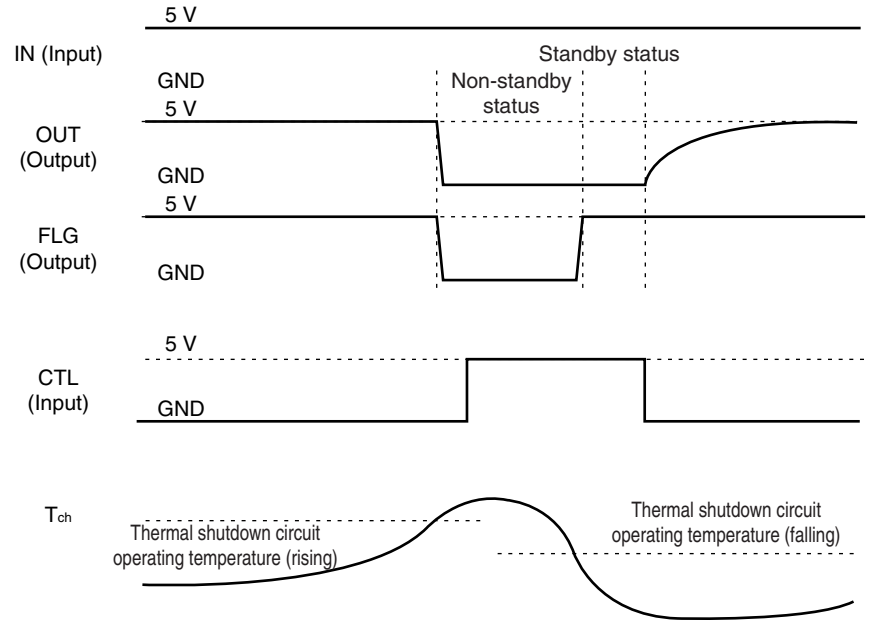


If an overcurrent is detected after the overcurrent detection delay time of 20 μs, the IC executes a slow-start operation (output rise time: 5 ms TYP.) again.

If an overcurrent is detected while the IC is executing the slow-start operation again, it is assumed that the output is short-circuited and the FLG pin goes low. When the CTL signal is deasserted inactive, OUT is turned OFF and FLG goes high. If the CTL signal is asserted active, OUT is turned back ON unless the undervoltage lockout circuit or thermal shutdown circuit is activated.

When LATCH = “H”, output is turned off at the timing of FLG = “L”.

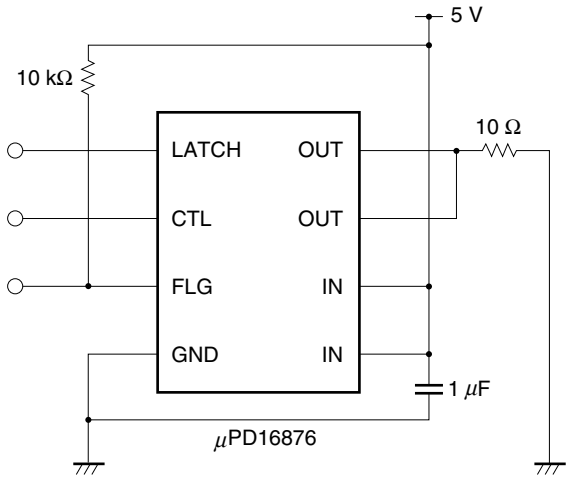
When Thermal Shutdown Circuit Operates



While the thermal shutdown circuit is activated, the output pins are in the OFF status. However, the IC does not enter the standby status even if all the CLT pins are deasserted inactive at the same time.

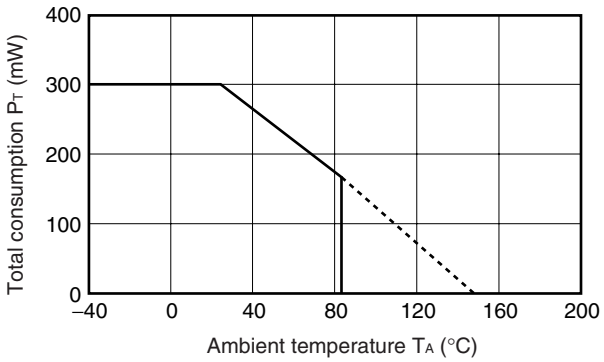
The thermal shutdown circuit is not activated even if the junction temperature exceeds 150°C TYP. while the IC is in the standby mode (when CTL1 and CTL2 pins are inactive).

TEST CIRCUIT

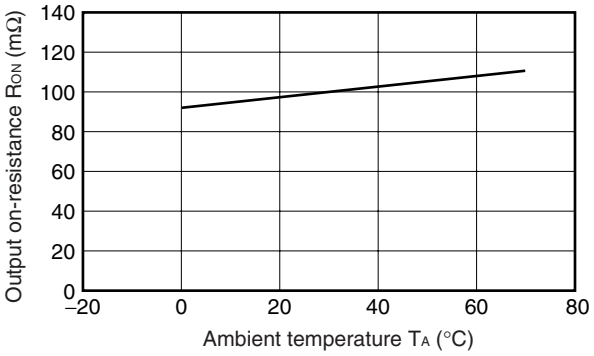


MAJOR CHARACTERISTIC CURVES (Unless otherwise specified, T_A = 25°C, V_{IN} = 5 V)

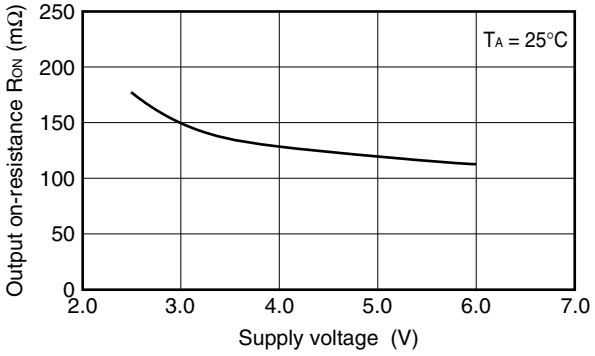
Total Power Dissipation P_T vs. Ambient Temperature T_A



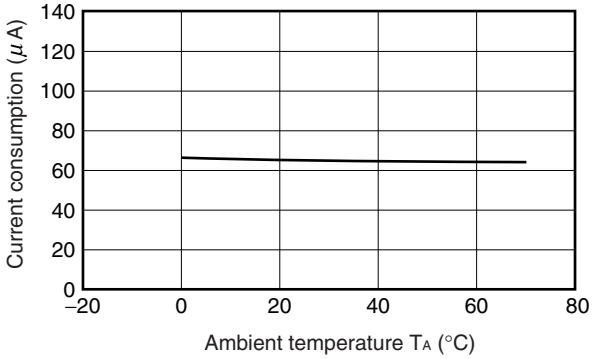
Output On-Resistance R_{ON} vs. Ambient Temperature T_A



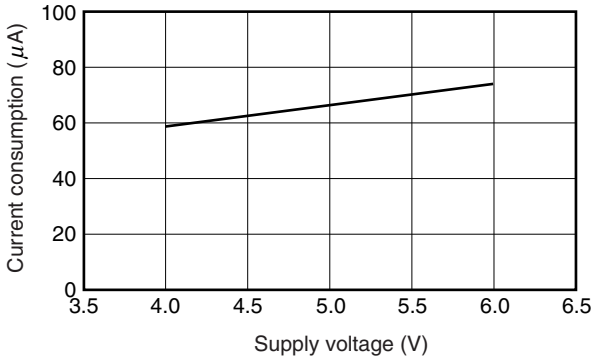
Output On-Resistance R_{ON} vs. Supply Voltage V_{IN}



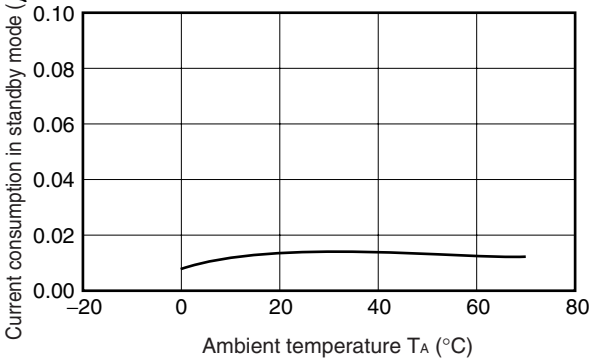
Current Consumption I_{DD} vs. Ambient Temperature T_A



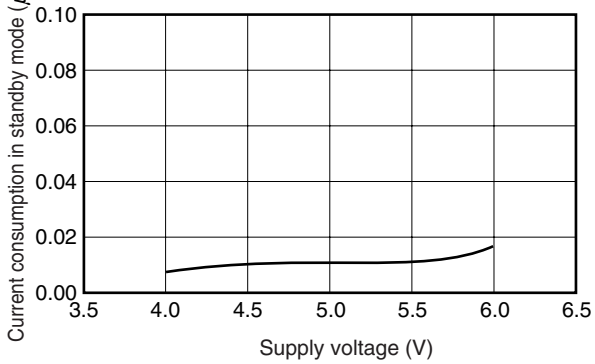
Current Consumption I_{DD} vs. Supply Voltage V_{IN}



Current Consumption (Standby) I_{DD} vs. Ambient Temperature T_A

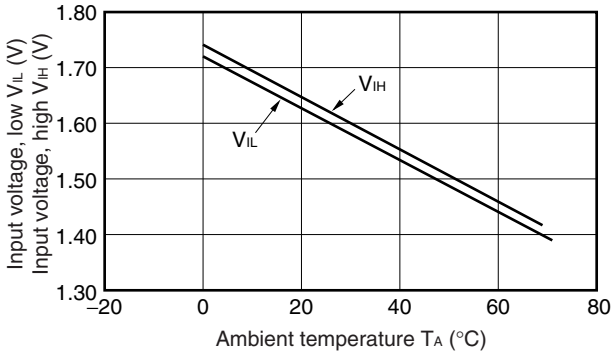


Current Consumption (Standby) I_{DD} vs. Supply Voltage V_{IN}

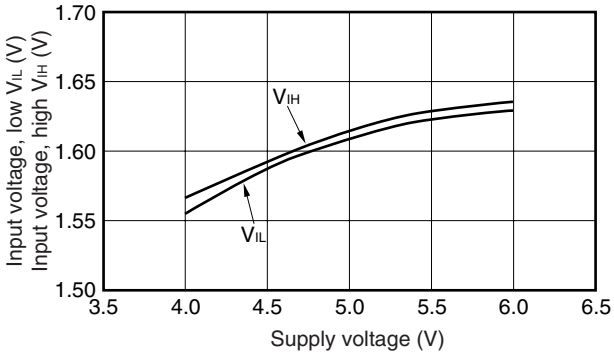


MAJOR CHARACTERISTIC CURVES (Unless otherwise specified, T_A = 25°C, V_{IN} = 5 V)

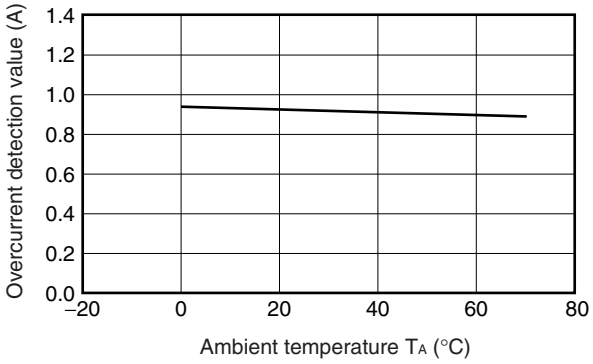
Input Voltage V_I vs. Ambient Temperature T_A



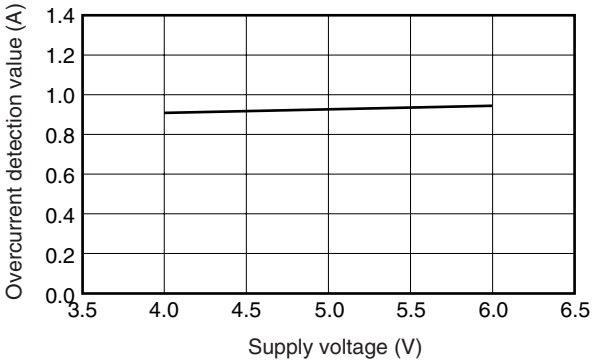
Input Voltage V_I vs. Supply Voltage V_{IN}



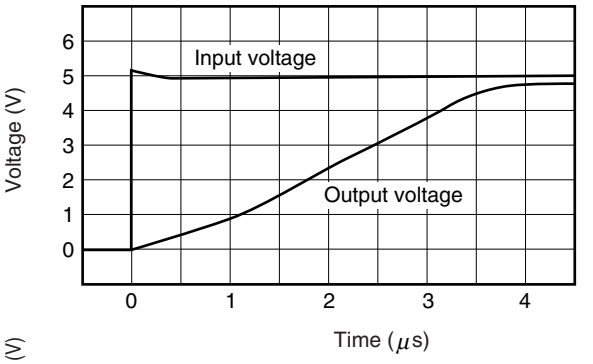
Overcurrent Threshold I_{TH} vs. Ambient Temperature T_A



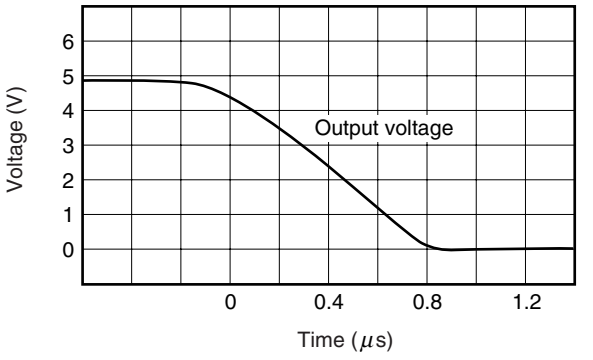
Overcurrent Threshold I_{TH} vs. Supply Voltage V_{IN}



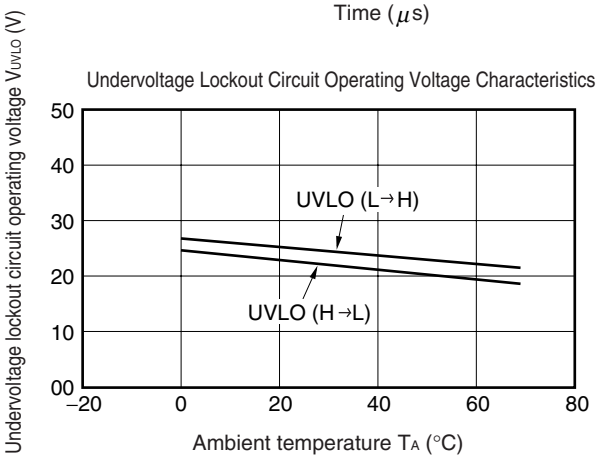
Output Rise Delay Time Characteristics



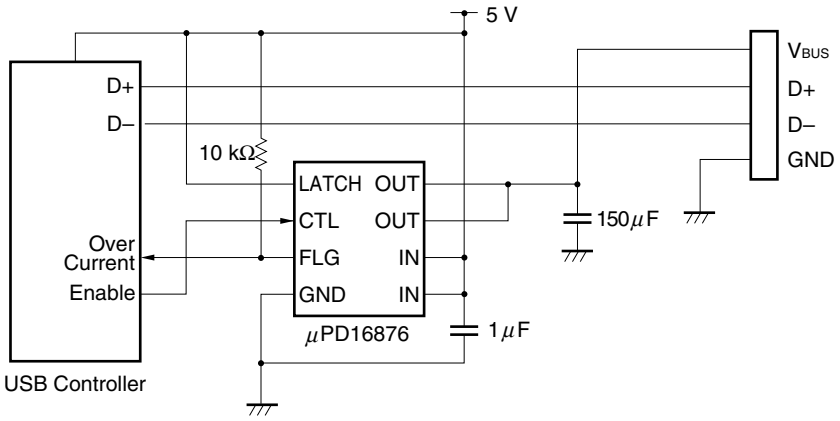
Output Fall Delay Time Characteristics



Undervoltage Lockout Circuit Operating Voltage Characteristics



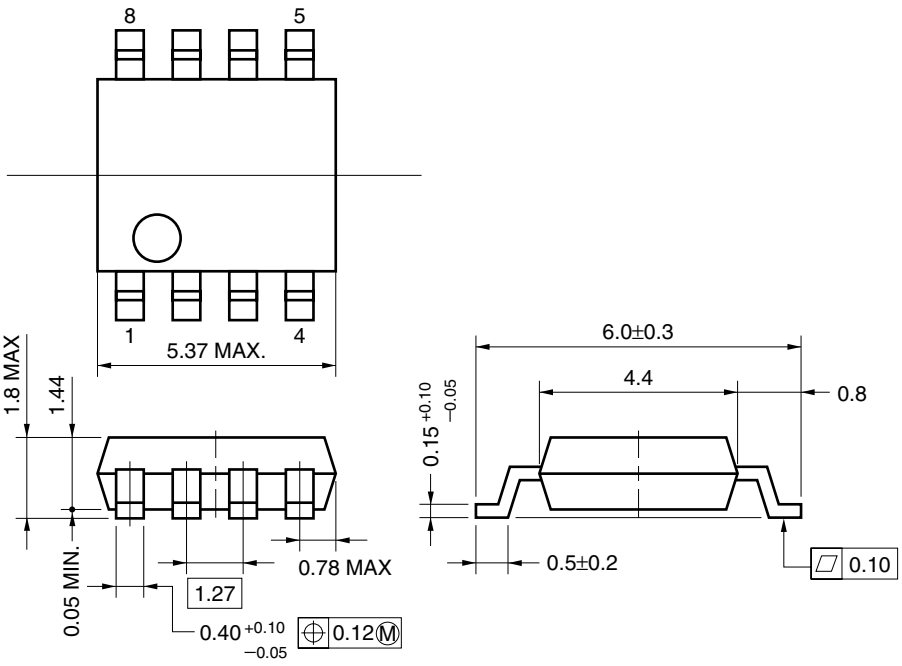
APPLICATION CIRCUIT



The application circuits and their parameters are for references only and are not intended for use in actual designin's.

PACKAGE DRAWING

8-Pin Plastic SOP (5.72 mm (225)) (Unit: mm)



RECOMMENDED SOLDERING CONDITIONS

The μPD16876 should be soldered and mounted under the following recommended conditions.
For soldering methods and conditions other than those recommended, contact your NEC sales representative.

Surface Mount Type

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

μPD16876G

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: two times, Exposure limit: Not limited[Note]	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: two times, Exposure limit: Not limited[Note]	VP15-00-2
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 sec. Max., Count: once, Exposure limit: not limited[Note]	WS60-00-1
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max., Exposure limit: not limited[Note]	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Cautions Do not use different soldering methods together (except for partial heating).

REFERENCE

Quality Grades on NEC semiconductor Devices	C11531E
Semiconductor Device Mounting Technology Manual	C10535E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Semiconductor Selection Guide	X13769E

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Tel: 02-2719-2377
Fax: 02-2719-5951

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Electron Devices Division
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