

MN101D02D , MN101D02F , MN101D02G , MN101D02H

VTR Servo

Type	MN101D02D	MN101D02F	MN101D02G	MN101D02H
ROM (×8-bit)	72 K	96 K	128 K	160 K
RAM (×8-bit)	2 K	3 K	4 K	5 K
Package	QFP100-P-1818B *Pb free			
Minimum Instruction Execution Time	With main clock operated	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz)		
	When sub-clock operated	71.5 μs (at 2.2 V to 5.5 V fixed to 14.32 MHz internal frequency division)		
		61 μs (at 2.2 V to 5.5 V, 32.768 kHz)		
Interrupts	• RESET • Runaway • External 0, 1, 2, 3, 4/key input (p50 to 54) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 6 • Capstan FG • Control • HSW • Cylinder FG • Servo VSYNC • Synchronous output • OSD • XDS • Serial 0 • Serial 1 • Serial 2 • A/D (common with PWM 14 reference frequency) • OSDVSYNC			
Timer Counter	Timer counter 0: 16-bit × 1 (timer function, clock function [max. 2 s or max. 36 h at cascade-connecting with timer 6]) Clock source 1/2, 1/4, 1/8, 1/16 of system clock frequency; overflow of timer counter 6; 1/512 of XI oscillation clock or OSC oscillation clock frequency Interrupt source overflow of timer counter 0 Timer counter 1: 16-bit × 1 (timer function, linear timer counter function) Clock source 1/2, 1/4, 1/8, 1/16 of system clock frequency; CTL signal Interrupt source overflow of timer counter 1 Timer counter 2: 16-bit × 1 (timer function, input capture (DCTL specified edge), duty judgment of DCTL signal) Clock source 1/2, 1/4, 1/8, 1/12, 1/16, 1/24 of system clock frequency Interrupt source overflow of timer counter 2; input of DCTL specified edge; underflow of timer 2 shift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shift register compare register Timer counter 3: 16-bit × 1 (timer function, detection of serial indexing, generation of remote control output carrier frequency) Clock source 1/2, 1/4, 1/8, 1/16 of system clock frequency Interrupt source overflow of timer counter 3 Timer counter 4: 16-bit × 1 (timer function, event count [P15 input], generation of serial transmission clock) Clock source 1/8, 1/16 of system clock frequency; external clock input Interrupt source overflow of timer counter 4; coincidence of timer counter 4 with OCR4 Timer counter 5: 17-bit × 1 (watchdog, stable oscillation waiting function) Clock source system clock Watchdog interrupt source · 1/2 ¹⁶ , 1/2 ¹⁹ of timer counter 5 frequency Clear by stable oscillation · after 256 counts by timer counter 5 (2 ¹⁸ counts of OSC oscillation clock) Timer counter 6: 16-bit × 1 (clock function [max. 2 s]) Clock source 1/512 of OSC oscillation clock frequency; XI oscillation clock; 1/4, 1/8, 1/64, 1/128 of system clock frequency Interrupt source 1/2 ¹³ , 1/2 ¹⁴ , 1/2 ¹⁵ overflow of timer counter 6			
Serial Interface	Serial 0: 8-bit × 1 (synchronous type/start-stop synchronous type) (transfer direction of MSB/LSB selectable) Synchronous type clock source · 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 4 output; $\overline{\text{SBT0}}$ pin input Clock for UART 8-division of above clock; 2-division timer 4 output; $\overline{\text{SBT0}}$ pin input Serial 1: 8-bit × 1 (synchronous type/remote control transmission/simple remote control receive) (transfer direction of MSB/LSB selectable, start condition function) Clock source 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 4 output; $\overline{\text{SBT1}}$ pin input Remote control clock 2-division timer output			

Serial Interface (Continue)		Serial 2: 8-Bit × 1 (I ² C) (master transmission/reception, slave transmission/reception) Clock source 1/72, 1/80, 1/84, 1/96, 1/102, 1/112, 1/128, 1/144, 1/160, 1/168, 1/192, 1/224, 1/256, 1/320 of system clock, SCK pin input	
OSD		Accommodation with menu or super impose display Applicable broadcasting system : NTSC, PAL, PAL-M, PAL-N Screen configuration : 24 characters × 2n rows (n = 1 to 6) Character type : max. 512 character types (variable) Character size : 12 × 18 dots Enlarged characters : each × 2, × 3 or × 4 settings in horizontal and vertical Character interpolation : none Background color : 8-hue settable (settable in the row unit at menu display) Background intensity : 8 gradations settable in the row unit Character color : white Character intensity : 8 gradations settable in the row unit Frame function : 1-dot frame in 4 or 8 directions Frame intensity : 4 gradations settable in the row unit Box shade function : settable in the character unit (only at composite output with 128 character types or more) Blinking : none (covered by software) Inverted character : settable in the character unit Halftone : settable in the row unit in 2 intensity gradations (setting in the row unit) Input : composite video signal input (output level: 1 V _[p-p] / 2 V _[p-p]) Clamp method : sync chip clamp, clamp level in 4 levels Output : composite video output : digital output (6 pins) : 8 character and background colors each settable at digital output. Measure against image fluctuation : built-in AFC circuit Sync signal detection function : detection functions for horizontal and vertical sync signals (integral system) with horizontal sync signal interpolation function	
XDS		Built-in U.S. closed caption data slicer (optional 2 line data can be extracted.)	
ROM Correction		Correcting address designation: up to 2 addresses possible Correction method: correction program being saved in internal RAM	
I/O Pins	I/O	73	• Common use: 73 ports 0, 1, 2, 4, 5, 6, 7, A, B (by bit)
	Input	4	• Common use: 4
A/D Inputs		8-bit × 12-ch. (without S/H)	
PWM		13-bit × 2-ch. (at repetition cycle 572 μs, 14.32 MHz), 10-bit × 2-ch. (at repetition cycle 71.5 μs, 14.32 MHz), 14-bit × 1-ch. (at repetition cycle 1144 μs, 14.32 MHz)	
ICR		18-bit × 6-ch.	
OCR		16-bit × 7-ch. , 8-bit × 1-ch.	
Special Ports		Buzzer output; 3-state output (PTO) VLP pin; synchronous output: 7; 3-state synchronous output: 4; remote control receive; CTL amp; built-in FG amp; output of 1/2 OSC oscillation clock (2 V _[p-p]); output of 1/4 OSC oscillation clock (1 V _[p-p])	
Notes		VISS/VASS detection function	

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	14.32 MHz operation without load, VDD = 5 V		60	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load, VDD = 2.7 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	mA
Supply current at STOP	IDSP	Stop of oscillation without load		0	20	μA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	μA

(Ta = 25°C±2°C, VDD = 5.0 V, VSS = 0 V)

A/D Converter Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion relative error	ΔNLAD				±3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		μs
Analog Input Voltage			0		5	V

(Ta = 25°C±2°C, VDD = 5.0 V, VSS = 0 V)

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