

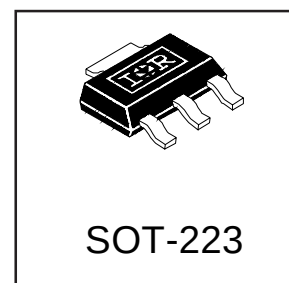
Applications

- High frequency DC-DC converters
- Lead-Free

V_{DSS}	$R_{DS(on)}$ max	I_D
150V	185mΩ@$V_{GS} = 10V$	2.6A

Benefits

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	2.6	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 10V	2.1	
I_{DM}	Pulsed Drain Current ①	21	
P_D @ $T_A = 25^\circ C$	Power Dissipation④	2.8	W
	Linear Derating Factor	0.02	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ⑥	6.3	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state)④	—	45	°C/W

Notes ① through ⑥ are on page 8
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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.19	—	V/°C	Reference to 25°C , $I_D = 1mA$ ③
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	185	mΩ	$V_{GS} = 10V, I_D = 1.6A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 120V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

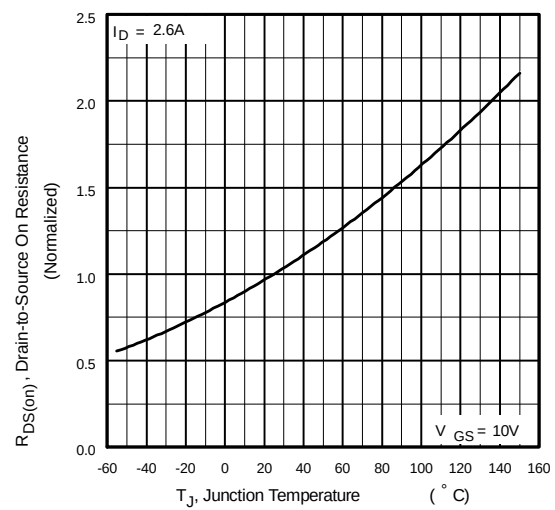
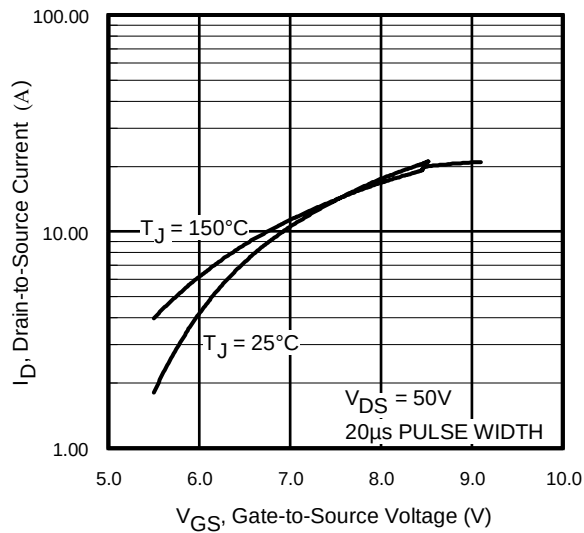
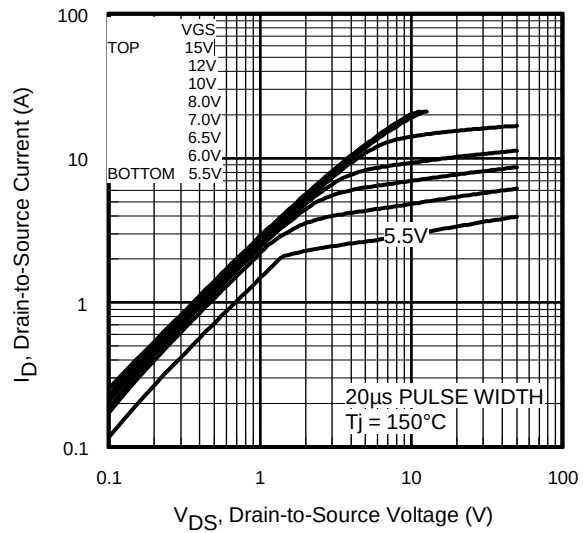
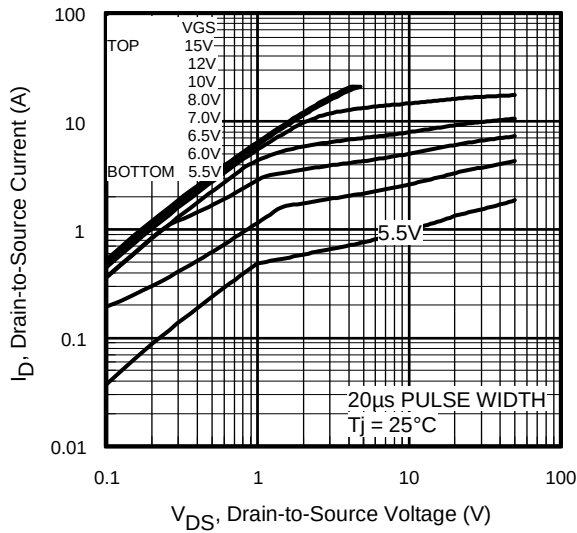
	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	3.5	—	—	S	$V_{DS} = 50V, I_D = 1.6A$
Q_g	Total Gate Charge	—	12	19	nC	$I_D = 1.6A$
Q_{gs}	Gate-to-Source Charge	—	2.1	3.1		$V_{DS} = 120V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	6.8	10		$V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	8.4	—	ns	$V_{DD} = 75V$
t_r	Rise Time	—	21	—		$I_D = 1.6A$
$t_{d(off)}$	Turn-Off Delay Time	—	20	—		$R_G = 15\Omega$
t_f	Fall Time	—	19	—		$V_{GS} = 10V$ ③
C_{iss}	Input Capacitance	—	420	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	100	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	25	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	720	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	48	—		$V_{GS} = 0V, V_{DS} = 120V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	98	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$ ③

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	38	mJ
I_{AR}	Avalanche Current①	—	3.1	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.6	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	21		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 2.1A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	61	91	ns	$T_J = 25^\circ\text{C}, I_F = 1.6A$
Q_{rr}	Reverse Recovery Charge	—	160	240	nC	$di/dt = 100A/\mu s$ ③



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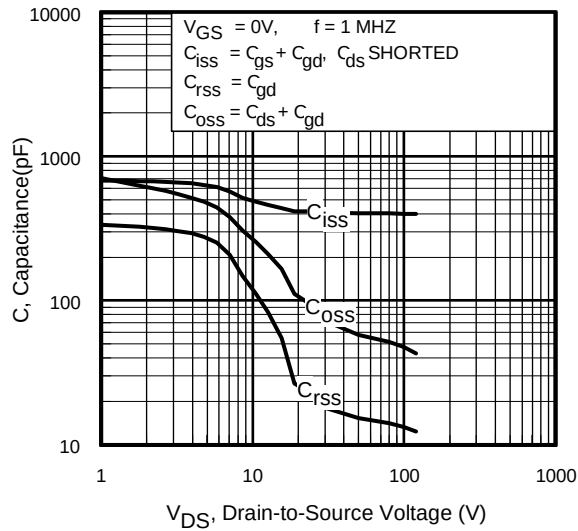


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

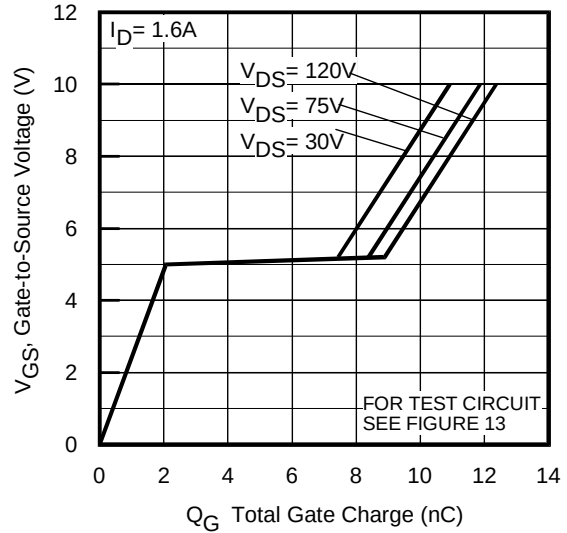


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

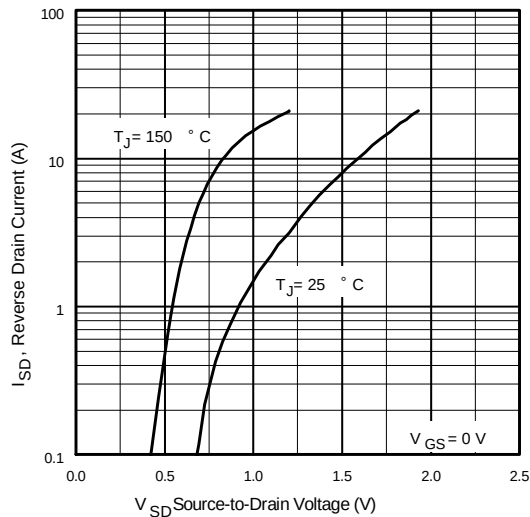


Fig 7. Typical Source-Drain Diode Forward Voltage

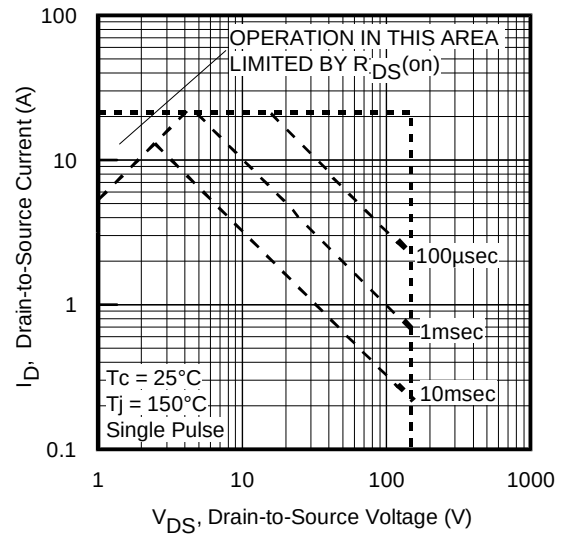


Fig 8. Maximum Safe Operating Area

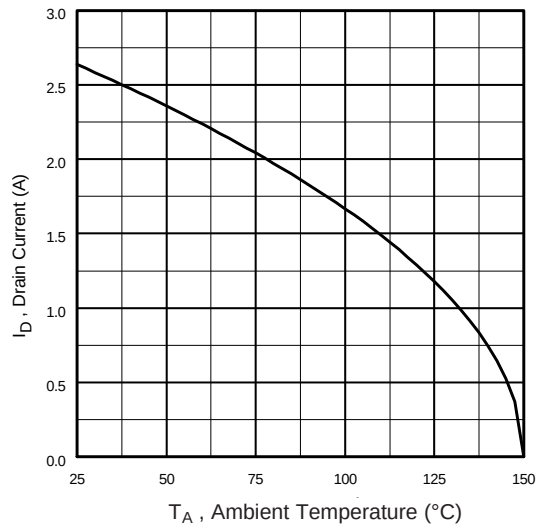


Fig 9. Maximum Drain Current Vs. Ambient Temperature

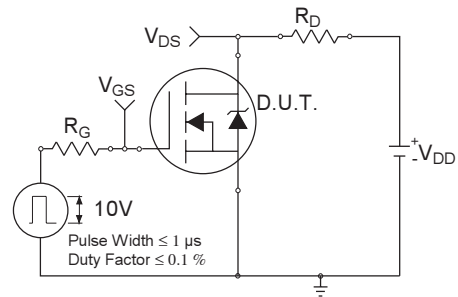


Fig 10a. Switching Time Test Circuit

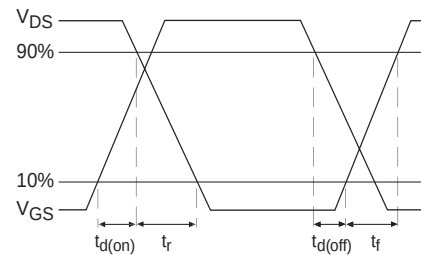


Fig 10b. Switching Time Waveforms

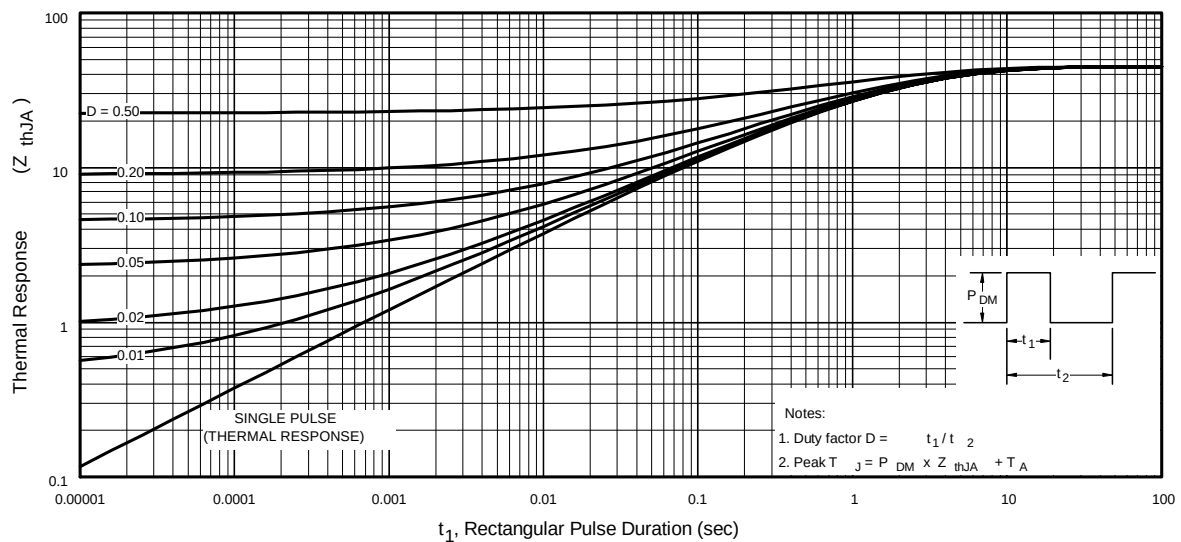


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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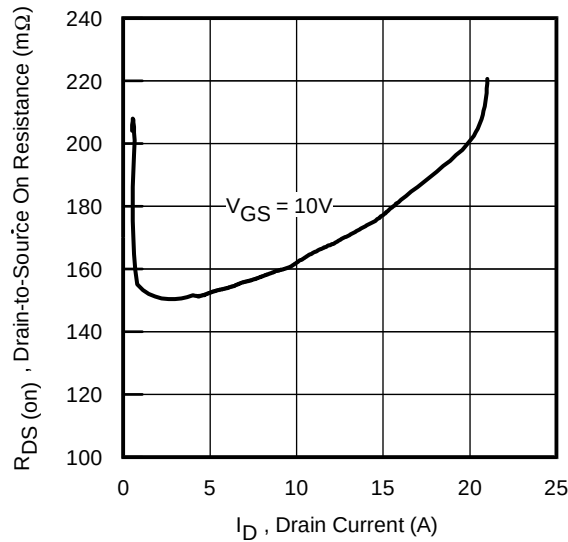


Fig 12. On-Resistance Vs. Drain Current

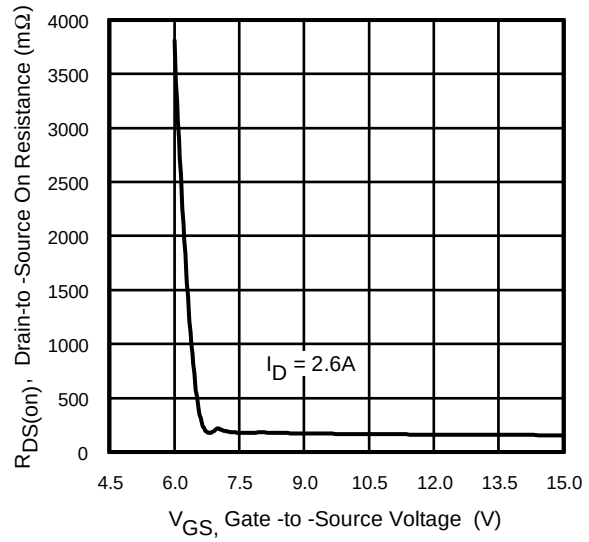


Fig 13. On-Resistance Vs. Gate Voltage

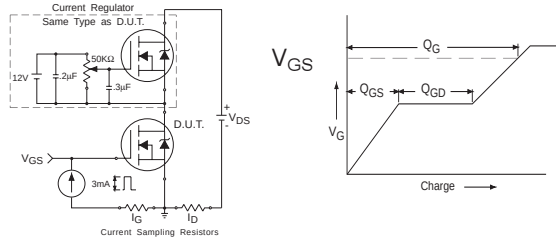


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

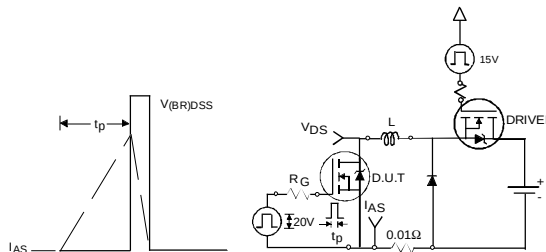


Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

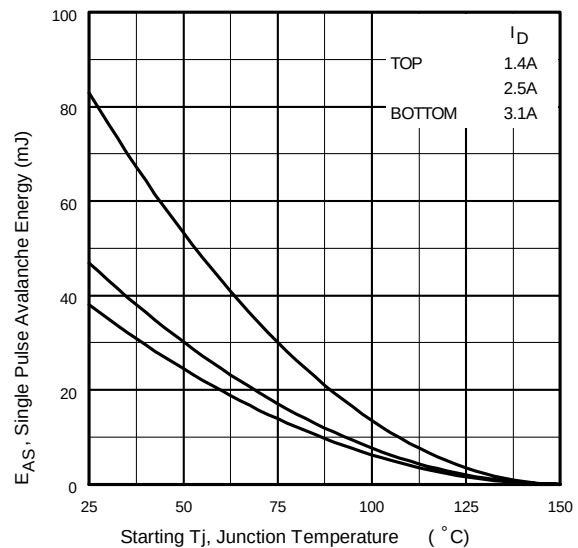
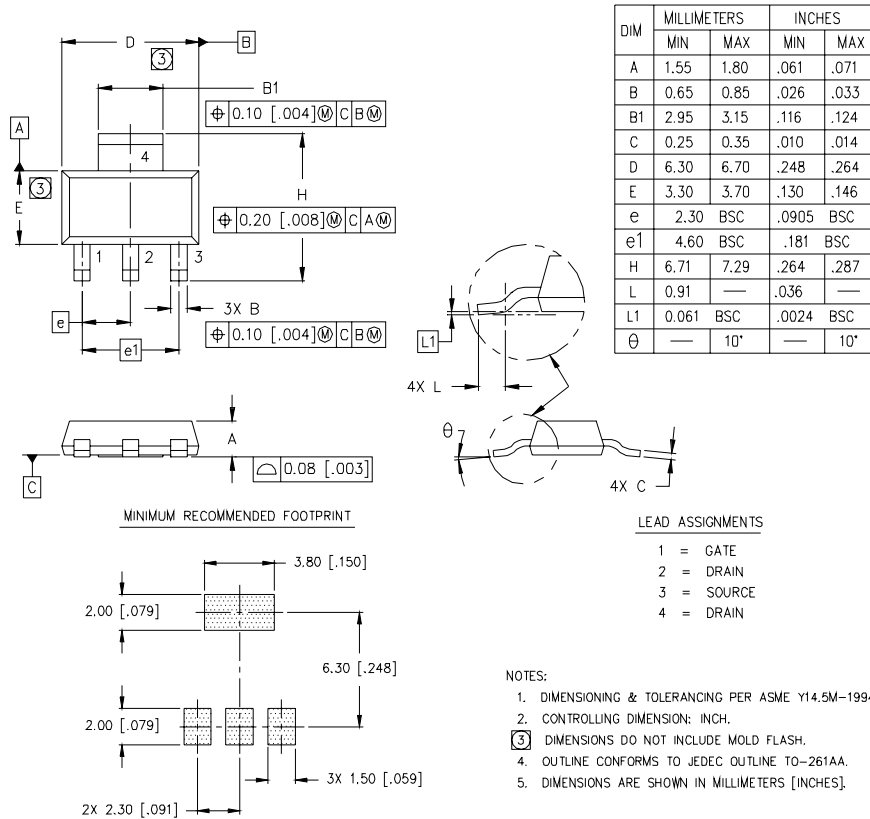


Fig 15c. Maximum Avalanche Energy Vs. Drain Current

SOT-223 (TO-261AA) Package Outline

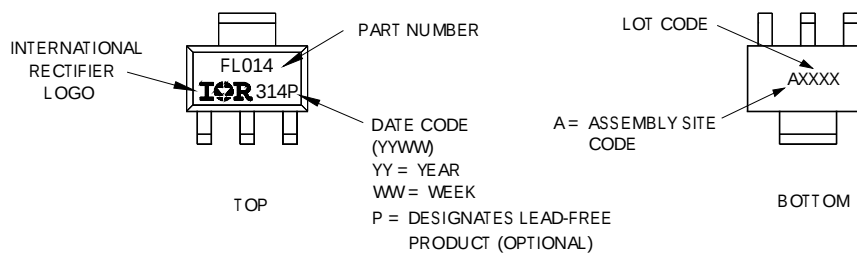
Dimensions are shown in millimeters (inches)



SOT-223 (TO-261AA) Part Marking Information

HEXFET PRODUCT MARKING

EXAMPLE: THIS IS AN IRFL014

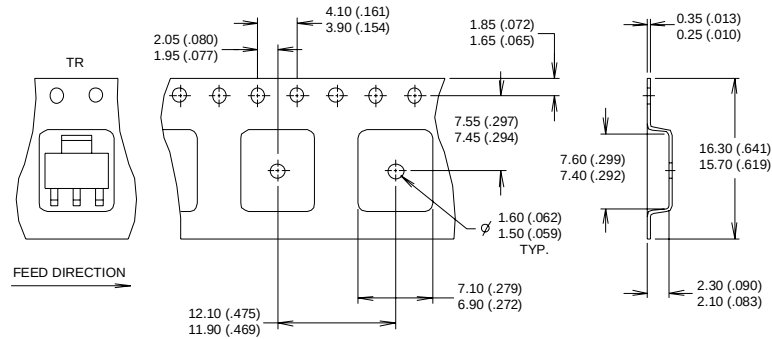


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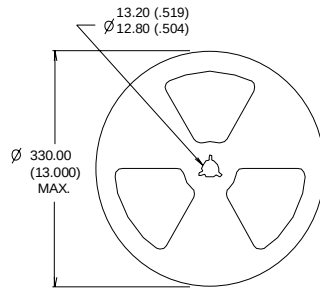
SOT-223 (TO-261AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



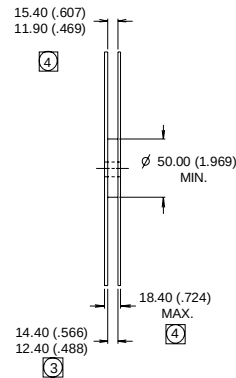
NOTES :

1. CONTROLLING DIMENSION: MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.
3. EACH Ø330.00 (13.00) REEL CONTAINS 2,500 DEVICES.



NOTES :

1. OUTLINE CONFORMS TO EIA-418-1.
2. CONTROLLING DIMENSION: MILLIMETER..
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 7.8\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 3.1\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ $I_{SD} \leq 1.6\text{A}$, $di/dt \leq 230\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$.

Data and specifications subject to change without notice.

This product has been designed and qualified for the Automotive [Q101] market.

Qualification Standards can be found on IR's Web site.

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