PI4ULS5V108

8-Bit Bi-directional Level Shifter for Open-Drain and Push-Pull Application

Features

➔ Provides Bidirectional Voltage Translation With No Direction Pin

➔ Supports Up to 100 MHz Up Translation and Greater Than 100 MHz Down Translation at≤ 30pF Cap Load and Up To 40 MHz Up/Down Translation at 50 pF Cap Load

➔ Supports Hot Insertion

➔ Allow Bidirectional Voltage Level Translation Between
  – 0.95 V ↔ 1.8/2.5/3.3/5 V
  – 1.2 V ↔ 1.8/2.5/3.3/5 V
  – 1.8 V ↔ 2.5/3.3/5 V
  – 2.5 V ↔ 3.3/5 V
  – 3.3 V ↔ 5 V

➔ Low Standby Current

➔ 5 V Tolerance I/O Port to Support TTL

➔ Low Ron Provides Less Signal Distortion

➔ High-Impedance I/O pins For EN = Low

➔ Flow-Through Pin out for Ease PCB Trace Routing

➔ ESD protection (8KV HBM and 1KV CDM)

➔ Latch-Up Performance Exceeds 100 mA Per JESD 17

➔ −40°C to 125°C Operating Temperature Range

➔ Package: TSSOP-20, VQFN2.5x4.5-20

Description

The PI4ULS5V108 supports up to 100 MHz up translation and greater than 100 MHz down translation at ≤ 30pF cap load and up to 40 MHz up/down translation at 50pF cap load which allows the LSF family to support more consumer or telecom interfaces (MDIO or SDIO). It has bidirectional voltage translation without the need for DIR pin which minimizes system effort (for PMBus, I2C, or SMbus).

The PI4ULS5V108 supports 5 V tolerance on IO port which makes it compatible with TTL levels in industrial and telecom applications. It is able to set up different voltage translation levels on each channel which makes it very flexible.

Pin configuration
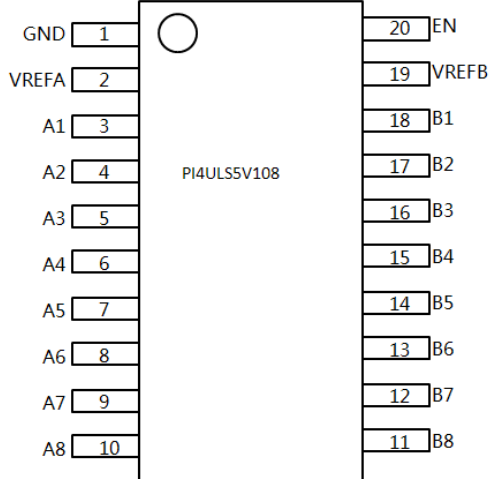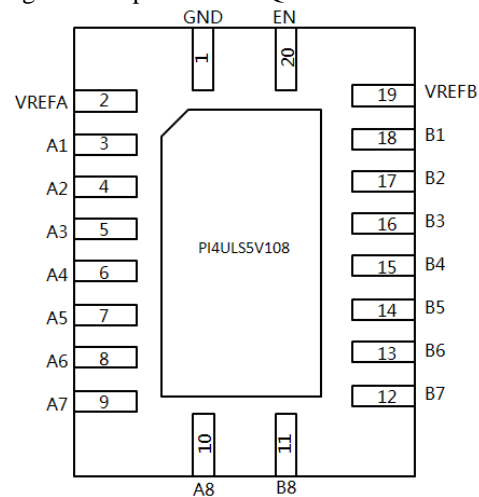
Figure 1. Top View of TSSOP-20

Figure 2. Top View of VQFN-20

Pin Description

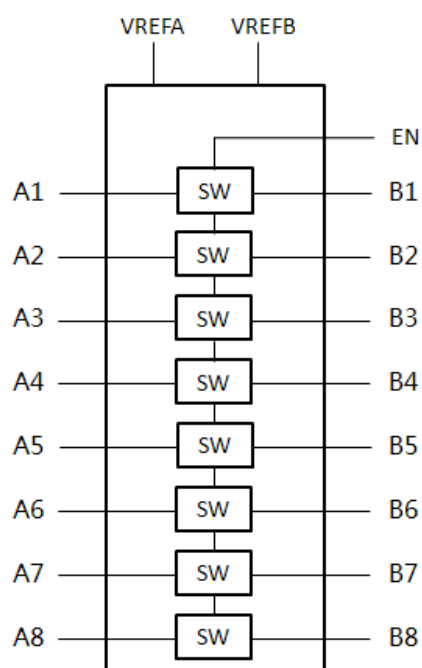| Pin Name	Pin No.	Description
GND	1	Ground.
VREFA	2	Reference supply voltage A
An	3-10	Data port A
Bn	18-11	Data port B
VREFB	19	Reference supply voltage B
EN	20	Enable. Connect to VREFB and pull-up through a 200k Ω resistor

Block Diagram

Figure 3: Block Diagram

Maximum Ratings

Storage Temperature	-65°C to +150°C
Tj, Junction temperature	125°C
Reference Voltage	-0.5V to +7.0V
I/O Input Voltage	-0.5V to +7.0V
channel current (DC)	128mA
Input clamping Current	-50Ma

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V$_{I/O}$	Voltage on an input/output pin	0	-	5	V
VREFA	Reference voltage	0	-	5	V
VREFB	Reference bias voltage	0	-	5	V
VEN	Input voltage on pin EN	0	-	5	V
I$_{(pass)}$	Pass switch current	-	-	64	mA
T$_A$	Ambient temperature	-40	-	85	$^\circ$C

DC Electrical Characteristics

(T$_A$ = –40°C to 85°C, unless otherwise noted. Typical values are at 3.3V Vdd and +25°C.)

Parameter	Description	Test Conditions[1]	Min	Typ.[2]	Max	Unit
Input and output SDAB and SCLB						
V$_{IK}$	input clamping voltage	I$_I$ = -18mA; VEN = 0 V	-	-	-1.2	V
I$_{IH}$	HIGH-level input current	V$_I$ = 5 V; VEN = 0 V	-	-	5	µA
ICC	Supply Current	VREFB = VEN = 5.5 V, VREFA = 4.5 V or 1 V, IO = 0, VI = VCC or GND		1		µA
C$_{i(refA/refB/EN)}$	input capacitance on pin VREFA, VREFB, EN	V$_I$ = 3 V or 0 V	-	11	-	pF
C$_{io(off)}$	off-state input/output capacitance	V$_O$ = 3 V or 0 V; VEN = 0 V	-	4	-	pF
C$_{io(on)}$	on-state input/output capacitance	V$_O$ = 3 V or 0 V; VEN = 3 V	-	10.5	-	pF

DC Electrical Characteristics Cont.

| Parameter	Description	Test Conditions[1]		Min	Typ.[2]	Max	Unit
Ron	ON-state resistance	$V_I = 0V$; $I_O = 64mA$; VREFB ,VEN connect to 5 V through 200k Ω	VREFA = 3.3 V;		8		Ω
			VREFA = 1.8 V;		9		Ω
			VREFA = 1.0 V;		10		Ω
		$V_I = 0V$; $I_O = 32mA$ VREFB ,VEN connect to 5 V through 200k Ω	VREFA = 1.8 V;		10		Ω
			VREFA = 2.5 V;		15		Ω
		$V_I = 1.8V$; $I_O = 15mA$ VREFB ,VEN connect to 5V through 200k Ω	VREFA = 3.3 V;		9		Ω
		$V_I = 1.0V$; $I_O = 10mA$ VREFB ,VEN connect to 3.3V through 200k Ω	VREFA = 1.8 V;		18		Ω
		$V_I = 0V$; $I_O = 10mA$ VREFB ,VEN connect to 3.3V through 200k Ω	VREFA = 1.0 V;		20		Ω
		$V_I = 0V$; $I_O = 10mA$ VREFB ,VEN connect to 1.8V through 200k Ω	VREFA = 1.0 V;		30		Ω

Notes:
1) All typical values are at $T_A = 25\ ℃$.
2) Measured by the voltage drop between the A and B pins at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.
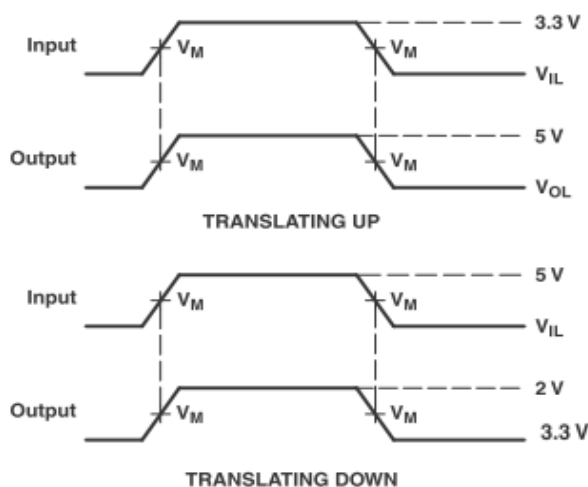
Dynamic characteristics

T_A = -40 °C to +85 °C; unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
Dynamic characteristics (translating down)									
VEN = 3.3 V; V_{IH} = 3.3 V; V_{IL} = 0 V; V_M = 1.15 V									
t_{PLH}	LOW-to-HIGH propagation delay	From A→B or B→A	1.9		1.4		0.78		ns
t_{PHL}	HIGH-to-LOW propagation delay		2		1.5		0.85		ns
VEN = 2.5 V; V_{IH} = 2.5 V; V_{IL} = 0 V; V_M = 0.75 V									
t_{PLH}	LOW-to-HIGH propagation delay	From A→B or B→A	2		1.45		0.8		ns
t_{PHL}	HIGH-to-LOW propagation delay		2.1		1.55		0.9		ns
Dynamic characteristics (translating up)									
VEN = 3.3 V; V_{IH} = 2.3 V; V_{IL} = 0 V; V_T = 3.3 V; V_M = 1.15 V; R_L = 300 Ω									
t_{PLH}	LOW-to-HIGH propagation delay		2.1		1.55		0.9		ns
t_{PHL}	HIGH-to-LOW propagation delay		2.2		1.65		1		ns
VEN = 2.5 V; V_{IH} = 1.5 V; V_{IL} = 0 V; V_T = 2.5 V; V_M = 0.75 V; R_L = 300 Ω									
t_{PLH}	LOW-to-HIGH propagation delay		1.8		1.35		0.8		ns
t_{PHL}	HIGH-to-LOW propagation delay		1.9		1.45		0.9		ns
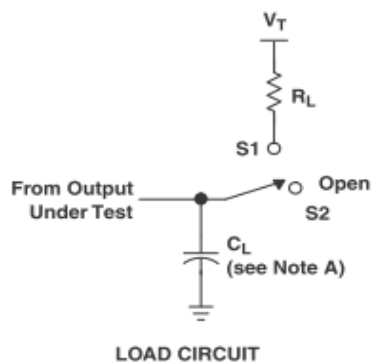
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 4 Test circuit

Function Description

The PI4ULS5V108 is bidirectional voltage level translators operational from 0.95 to 4.5 V (VREFA) and 1.8 to 5.5 V (VREFB). This allows bidirectional voltage translations between 1 V and 5 V without the need for a direction pin in open-drain or push-pull applications. It supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 30-pF capacitance and 250-Ω pull-up resistor.

When the A or B port is LOW, the switch is in the ON-state and a low resistance connection exists between the A and B ports. The low Ron of the switch allows connections to be made with minimal propagation delay and signal distortion. Assuming the higher voltage is on the B port when the B port is HIGH, the voltage on the A port is limited to the voltage set by VREFA When the A port is HIGH, the B port is pulled to the drain pull-up supply voltage by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

The supply voltage for each channel can be individually set up with a pull-up resistor. For example, channel 1 can be used in up-translation mode (1.2 V ↔ 3.3 V) and channel 2 in down-translation mode (2.5 V ↔ 1.8 V).When EN is HIGH, the translator switch is on, and the An is connected to the Bn , respectively, allowing bidirectional data flow between ports.

When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by VREFB To ensure the high-impedance state during power-up or power-down, EN must be LOW.

Application Information

The PI4ULS5V108 are able to perform voltage translation for open-drain or push-pull interface.
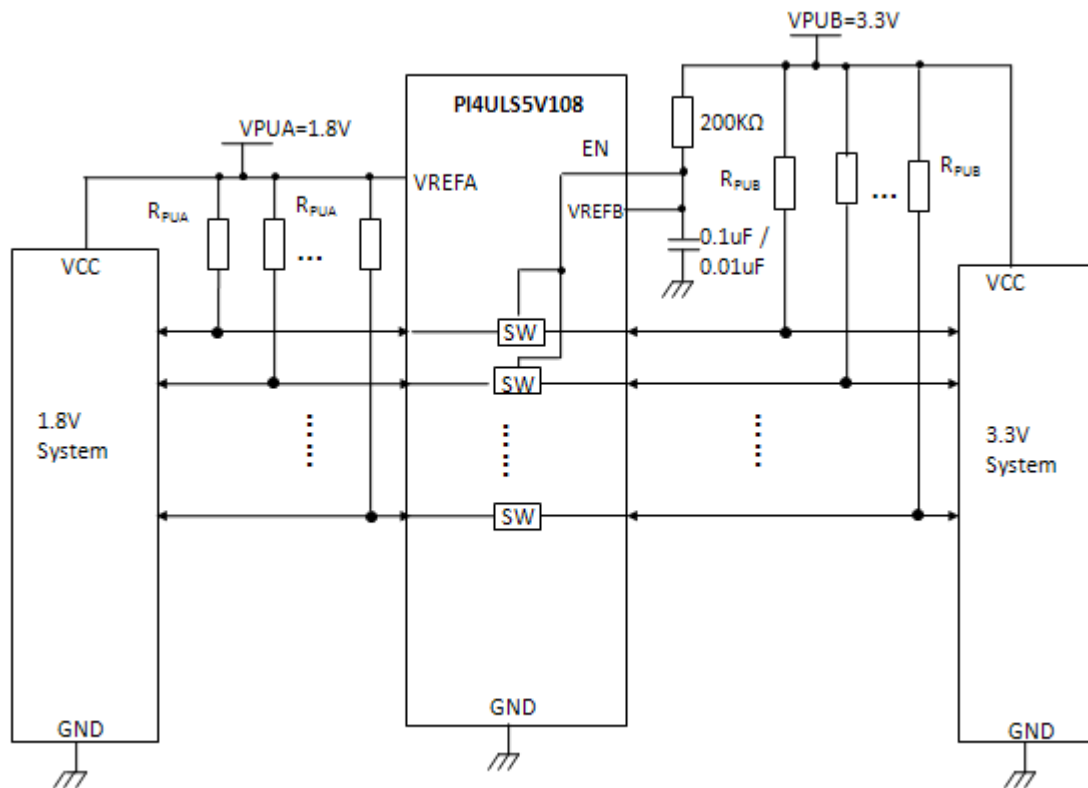

Figure 5 Typical Application

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREFB and both pins pulled to HIGH through a pull-up resistor (typically 200 k). This allows VREFB to regulate the EN input.

A filter capacitor on VREFB is recommended.

The master output driver can be totem pole or open-drain (pull-up resistors may be required) and the slave device output can be totem pole or open-drain (pull-up resistors are required to pull the Bn outputs to VPUB. However, if either output is totem-pole,

data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

When VREFB is connected through a 200k ohm resistor to a 3.3 V to 5.5 V power supply, and VREFA is set between 1.0 V and VPUB-1V, the output of each An has a maximum output voltage equal to VREFA, and the output of each Bn has a maximum output voltage equal to VPUB.

Pull-up resistors and minimum values

Sizing the pull-up resistor on an open-drain bus is specific to the individual application and is dependent on the following driver characteristics:

- The driver sink current
- The V_{OL} of driver
- The V_{OL} of the PI4ULS5V108
- The V_{IL} of the driver
- Frequency of operation

The following tables can be used to estimate the pull-up resistor value in different use cases so that the minimum resistance for the pull-up resistor can be found.

Tables in bellow contain suggested minimum values of pull-up resistors for the PI6UILS5V9306 with typical voltage translation levels and drive currents.

The calculated values assume that both drive currents are the same.

$V_{OL} = V_{IL} = 0.1*VCC$ and accounts for a 5 % VCC tolerance of the supplies, 1 % resistor values. It should be noted that the resistor chosen in the final application should be equal to or larger than the values shown in the table to ensure that the pass voltage is less than 10 % of the VCC voltage, and the external driver should be able to sink the total current from both pull-up resistors.

Pull-up resistor minimum values, 3 mA driver sink current for PI4ULS5V108

A Side	B side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.9V	$R_{RPUA} = 859\Omega$ $R_{RPUB} = 859\Omega$	$R_{RPUA} = 970\Omega$ $R_{RPUB} = 970\Omega$	$R_{RPUA} = $ none $R_{RPUB} = 896\Omega$ Or both 1.23kΩ	$R_{RPUA} = $ none $R_{RPUB} = 1.19$kΩ Or both 1.53kΩ	$R_{RPUA} = $ none $R_{RPUB} = 1.82$kΩ Or both 2.16kΩ
1.2V		$R_{RPUA} = 1.07$kΩ $R_{RPUB} = 1.07$kΩ	$R_{RPUA} = $ none $R_{RPUB} = 886\Omega$ Or both 1.33kΩ	$R_{RPUA} = $ none $R_{RPUB} = 1.18$kΩ Or both 1.63kΩ	$R_{RPUA} = $ none $R_{RPUB} = 1.81$kΩ Or both 2.26kΩ
1.5V			$R_{RPUA} = $ none $R_{RPUB} = 875\Omega$ Or both 1.43kΩ	$R_{RPUA} = $ none $R_{RPUB} = 1.17$kΩ Or both 1.73kΩ	$R_{RPUA} = $ none $R_{RPUB} = 1.8$kΩ Or both 2.36kΩ
1.8V			$R_{RPUA} = 1.53$kΩ $R_{RPUB} = 1.53$kΩ	$R_{RPUA} = $ none $R_{RPUB} = 1.16$kΩ Or both 1.82kΩ	$R_{RPUA} = $ none $R_{RPUB} = 1.79$kΩ Or both 2.46kΩ
2.5V				$R_{RPUA} = 2.06$kΩ $R_{RPUB} = 2.06$kΩ	$R_{RPUA} = $ none $R_{RPUB} = 1.77$kΩ Or both 2.69kΩ
3.3V					$R_{RPUA} = $ none $R_{RPUB} = 1.74$kΩ Or both 2.96kΩ

Pull-up resistor minimum values, 10 mA driver sink current for PI4ULS5V108

A Side	B side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.9V	$R_{RPUA} = 258\Omega$ $R_{RPUB} = 258\Omega$	$R_{RPUA} = 291\Omega$ $R_{RPUB} = 291\Omega$	$R_{RPUA} = none$ $R_{RPUB} = 269\Omega$ Or both 369Ω	$R_{RPUA} = none$ $R_{RPUB} = 358\Omega$ Or both 458Ω	$R_{RPUA} = none$ $R_{RPUB} = 546\Omega$ Or both 646Ω
1.2V		$R_{RPUA} = 321\Omega$ $R_{RPUB} = 321\Omega$	$R_{RPUA} = none$ $R_{RPUB} = 266\Omega$ Or both 399Ω	$R_{RPUA} = none$ $R_{RPUB} = 355\Omega$ Or both 488Ω	$R_{RPUA} = none$ $R_{RPUB} = 543\Omega$ Or both 677Ω
1.5V			$R_{RPUA} = none$ $R_{RPUB} = 263\Omega$ Or both 429Ω	$R_{RPUA} = none$ $R_{RPUB} = 352\Omega$ Or both 518Ω	$R_{RPUA} = none$ $R_{RPUB} = 540\Omega$ Or both 707Ω
1.8V			$R_{RPUA} = 460\Omega$ $R_{RPUB} = 460\Omega$	$R_{RPUA} = none$ $R_{RPUB} = 348\Omega$ Or both 548Ω	$R_{RPUA} = none$ $R_{RPUB} = 537\Omega$ Or both 737Ω
2.5V				$R_{RPUA} = 619\Omega$ $R_{RPUB} = 619\Omega$	$R_{RPUA} = none$ $R_{RPUB} = 521\Omega$ Or both 808Ω
3.3V					$R_{RPUA} = none$ $R_{RPUB} = 522\Omega$ Or both 889Ω

Pull-up resistor minimum values, 15 mA driver sink current for PI4ULS5V108

A Side	B side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.9V	$R_{RPUA} = 172\Omega$ $R_{RPUB} = 172\Omega$	$R_{RPUA} = 194\Omega$ $R_{RPUB} = 194\Omega$	$R_{RPUA} = none$ $R_{RPUB} = 179\Omega$ Or both 246Ω	$R_{RPUA} = none$ $R_{RPUB} = 238\Omega$ Or both 305Ω	$R_{RPUA} = none$ $R_{RPUB} = 364\Omega$ Or both 431Ω
1.2V		$R_{RPUA} = 214\Omega$ $R_{RPUB} = 214\Omega$	$R_{RPUA} = none$ $R_{RPUB} = 177\Omega$ Or both 266Ω	$R_{RPUA} = none$ $R_{RPUB} = 236\Omega$ Or both 325Ω	$R_{RPUA} = none$ $R_{RPUB} = 362\Omega$ Or both 451Ω
1.5V			$R_{RPUA} = none$ $R_{RPUB} = 175\Omega$ Or both 286Ω	$R_{RPUA} = none$ $R_{RPUB} = 234\Omega$ Or both 345Ω	$R_{RPUA} = none$ $R_{RPUB} = 360\Omega$ Or both 471Ω
1.8V			$R_{RPUA} = 306\Omega$ $R_{RPUB} = 306\Omega$	$R_{RPUA} = none$ $R_{RPUB} = 232\Omega$ Or both 366Ω	$R_{RPUA} = none$ $R_{RPUB} = 358\Omega$ Or both 492Ω
2.5V				$R_{RPUA} = 413\Omega$ $R_{RPUB} = 413\Omega$	$R_{RPUA} = none$ $R_{RPUB} = 354\Omega$ Or both 539Ω
3.3V					$R_{RPUA} = none$ $R_{RPUB} = 348\Omega$ Or both 593Ω

Max Frequency Application

The maximum frequency is limited by the minimum pulse width LOW and HIGH as well as rise time and fall time.

$$f(\text{max}) = \frac{1}{\text{tLOW(min)} + \text{tHIGH(min)} + \text{tr(actual)} + \text{tf(actual)}}$$
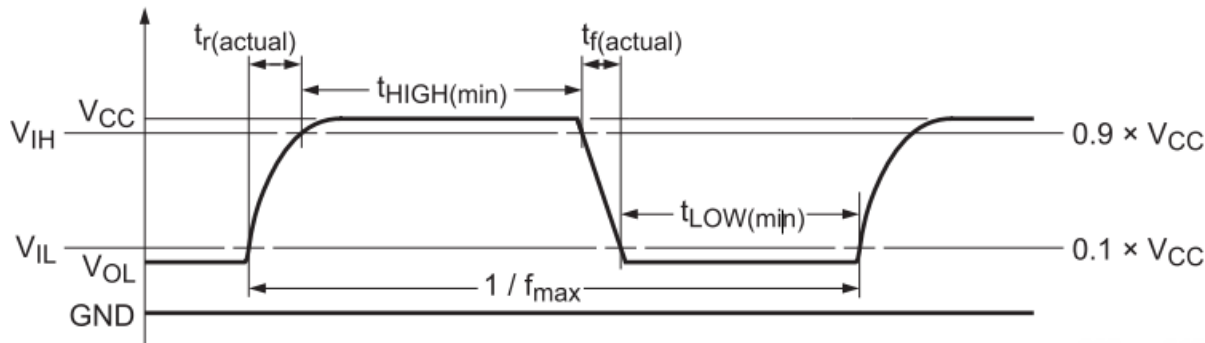
The rise and fall times are dependent upon translation voltages, the drive strength, the total node capacitance (CL) and the pull-up resistors (RPU) that are present on the bus. The node capacitance is the addition of the PCB trace capacitance and the device capacitance that exists on the bus.

Because of the dependency of the external components, PCB layout and the different device operating states the calculation of rise and fall times is complex and has several inflection points along the curve.

The main component of the rise and fall times is the RC time constant of the bus line when the device is in its two primary operating states: when device is in the ON state and it is low-impedance, the other is when the device is OFF isolating the A-side from the B-side.

There are some basic guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the PI4ULS5V108 close to the processor.
- The signal round trip time on trace should be shorter than the rise or fall time of signal to reduce reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher drive strength controlled by the pull-up resistor (up to 15 mA), the higher the frequency the device can use.

The system designer must design the pull-up resistor value based on external current drive strength and limit the node capacitance (minimize the wire, stub, connector and trace length) to get the desired operation frequency result.

Part Marking

L Package

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PI4ULS
5V108LE
YYWWXX̄
○
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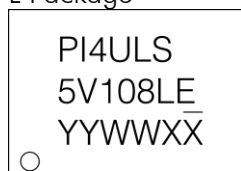
YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above fab code means Cu wire

ZBA Package

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PI4ULS5V
108ZBAE
YWXX̄
●
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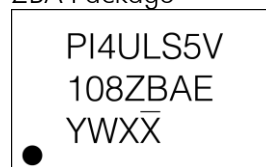
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above fab code means Cu wire

Packaging Mechanical:
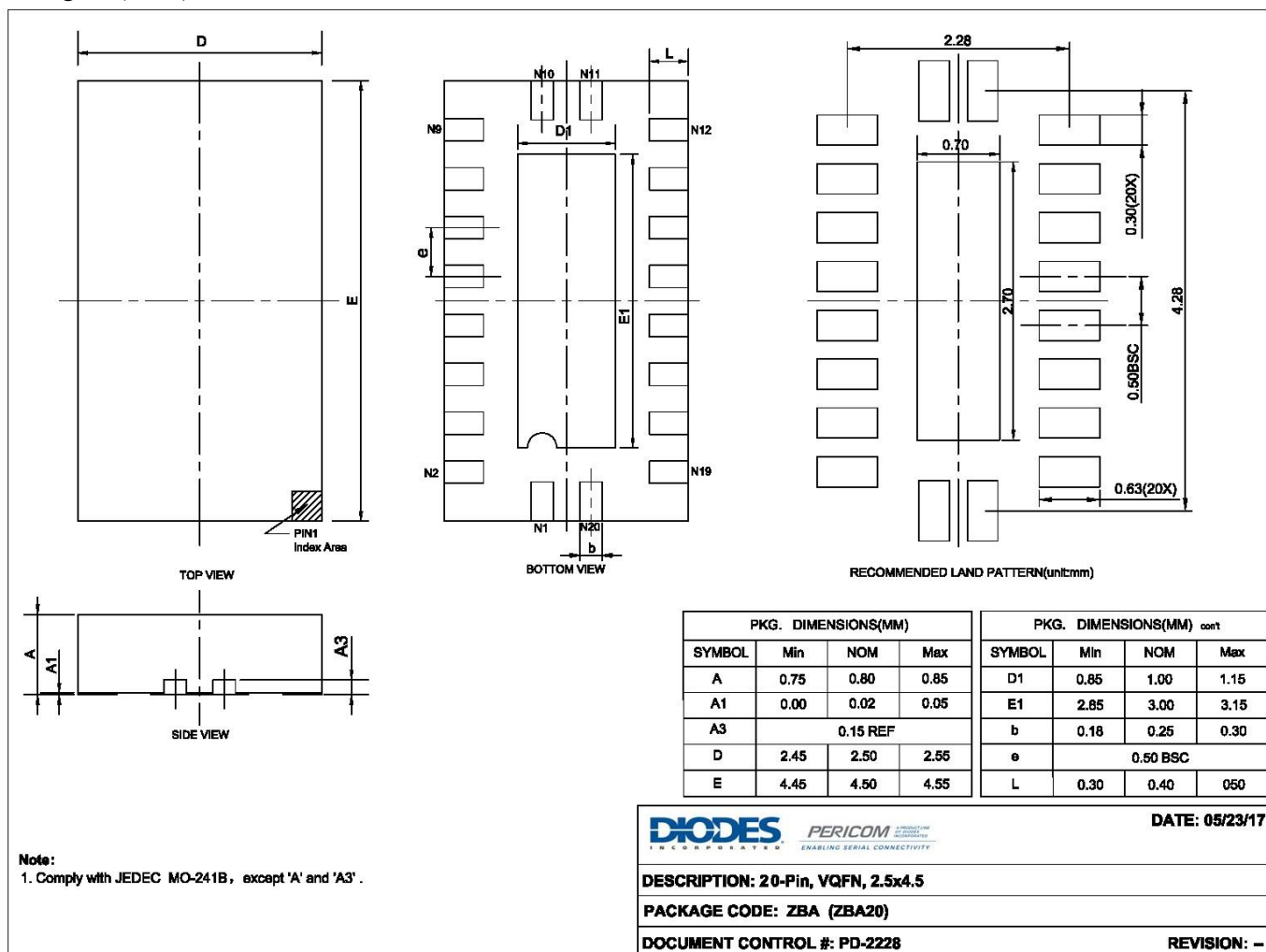**20-TSSOP (L)**

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO−153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

16-0074

PERICOM
Enabling Serial Connectivity

DATE: 03/31/16

DESCRIPTION: 20-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L20)

DOCUMENT CONTROL #: PD-1311

REVISION: G

20-VQFN (ZBA)

PKG. DIMENSIONS(MM)			
SYMBOL	Min	NOM	Max
A	0.75	0.80	0.85
A1	0.00	0.02	0.05
A3		0.15 REF	
D	2.45	2.50	2.55
E	4.45	4.50	4.55

PKG. DIMENSIONS(MM) con't			
SYMBOL	Min	NOM	Max
D1	0.85	1.00	1.15
E1	2.85	3.00	3.15
b	0.18	0.25	0.30
e		0.50 BSC	
L	0.30	0.40	050

DATE: 05/23/17

DESCRIPTION: 20-Pin, VQFN, 2.5x4.5

PACKAGE CODE: ZBA (ZBA20)

DOCUMENT CONTROL #: PD-2228   **REVISION: —**

Note:
1. Comply with JEDEC MO-241B，except 'A' and 'A3' .

17-0064

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part No.	Package Code	Package
PI4ULS5V108LEX	L	20-pin, 173 mil Wide TSSOP
PI4ULS5V108ZBAEX	ZBA	20-pin, 2.5x4.5(VQFN)

Notes:
- EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
- See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel