Improved Industry Standard Single-Ended Current Mode PWM Controller

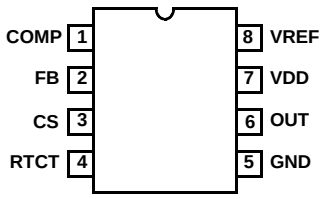
The ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845 family of adjustable frequency, low power, pulse width modulating (PWM) current mode controllers is designed for a wide range of power conversion applications including boost, flyback, and isolated output configurations. Peak current mode control effectively handles power transients and provides inherent overcurrent protection.

This advanced BiCMOS design is pin compatible with the industry standard 384x family of controllers and offers significantly improved performance. Features include low operating current, 60µA start-up current, adjustable operating frequency to 2MHz, and high peak current drive capability with 20ns rise and fall times.

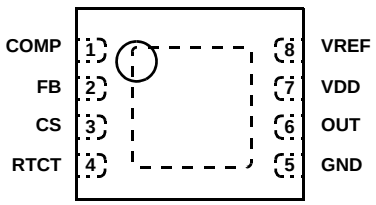
PART NUMBER	RISING UVLO (V)	MAX. DUTY CYCLE (%)
ISL6840	7.0	100
ISL6841	7.0	50
ISL6842	14.4	100
ISL6843	8.4	100
ISL6844	14.4	50
ISL6845	8.4	50

Pinouts

ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845
(8 LD SOIC, MSOP)
TOP VIEW



ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845
(8 LD DFN)
TOP VIEW



Features

- 1A MOSFET Gate Driver
- 60µA Start-up Current, 100µA Maximum
- 25ns Propagation Delay Current Sense to Output
- Fast Transient Response with Peak Current Mode Control
- Adjustable Switching Frequency to 2MHz
- 20ns Rise and Fall Times with 1nF Output Load
- Trimmed Timing Capacitor Discharge Current for Accurate Deadtime/Maximum Duty Cycle Control
- High Bandwidth Error Amplifier
- Tight Tolerance Voltage Reference Over Line, Load, and Temperature
- Tight Tolerance Current Limit Threshold
- Pb-Free Available (RoHS Compliant)

Applications

- Telecom and Datacom Power
- Wireless Base Station Power
- File Server Power
- Industrial Power Systems
- PC Power Supplies
- Isolated Buck and Flyback Regulators
- Boost Regulators

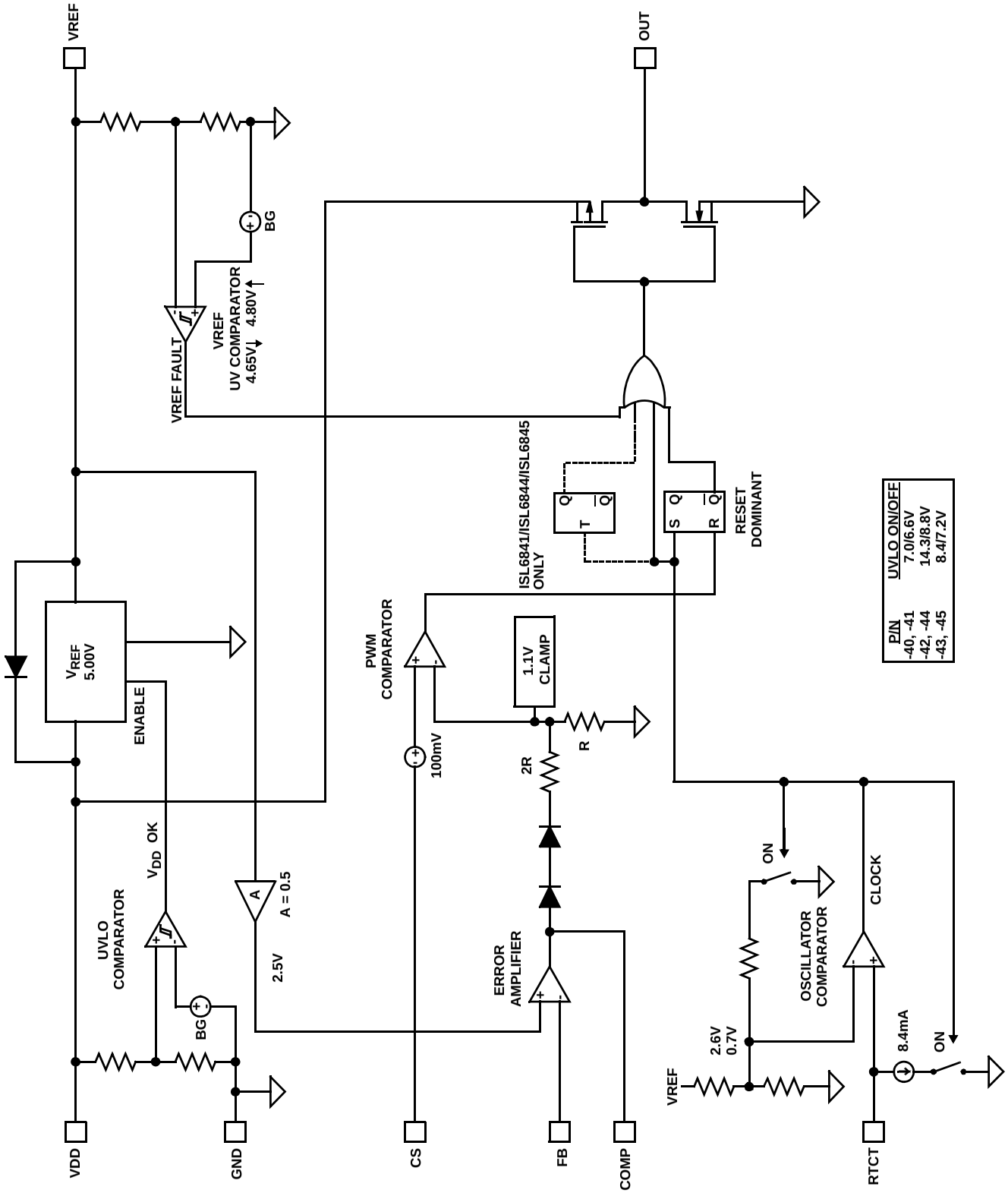
Ordering Information

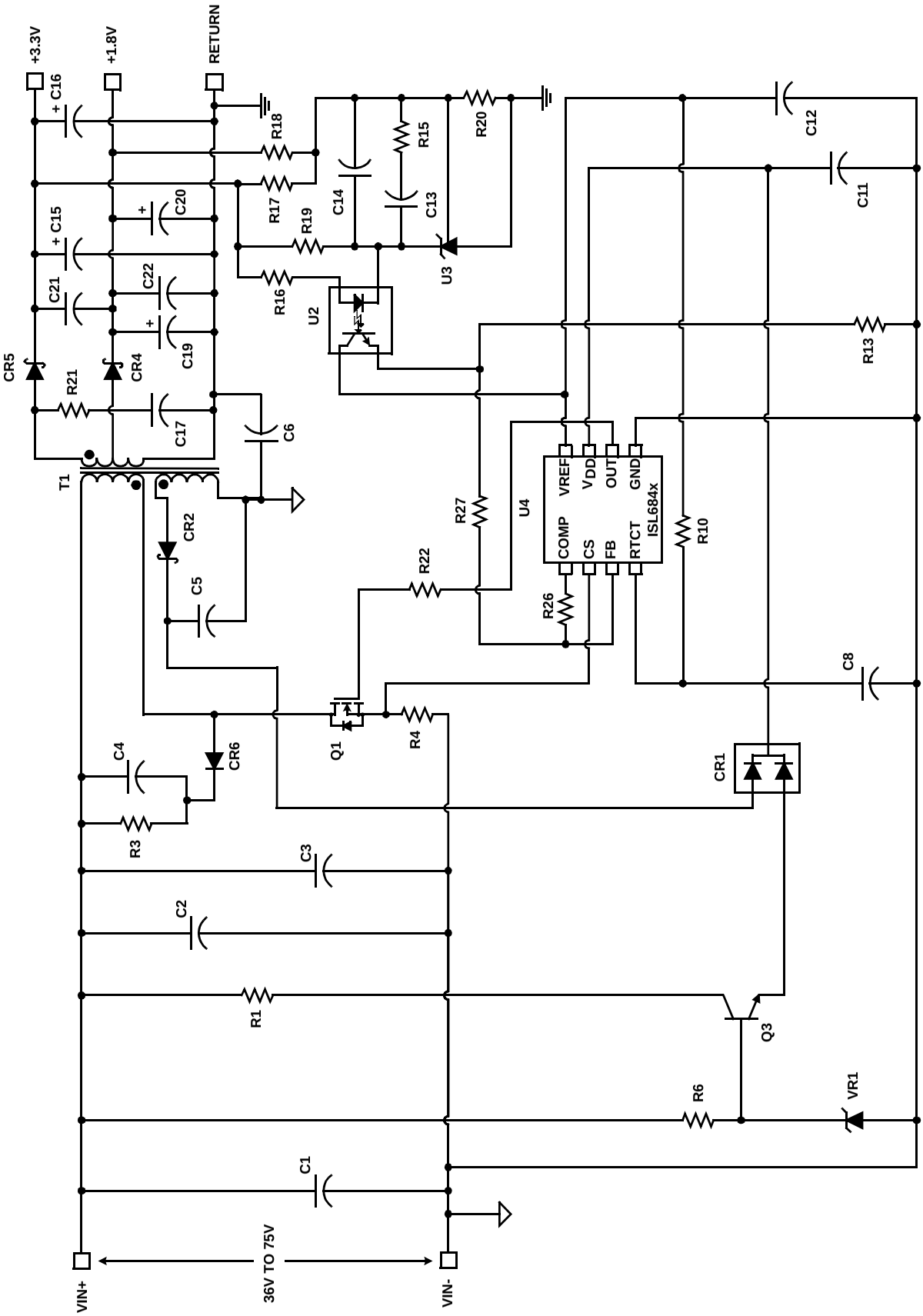
PART NUMBER (Note 4)	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6840IBZ (Notes 1, 3)	6840 IBZ	-40 to +105	8 Ld SOIC (Pb-free)	M8.15
ISL6840IRZ-T (Notes 2, 3)	40Z	-40 to +105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6840IUZ (Notes 1, 3)	6840Z	-40 to +105	8 Ld MSOP (Pb-free)	M8.118
ISL6841IB-T	ISL 6841IB	-40 to +105	8 Ld SOIC	M8.15
ISL6841IBZ (Notes 1, 3)	6841 IBZ	-40 to +105	8 Ld SOIC (Pb-free)	M8.15
ISL6841IRZ-T (Notes 2, 3)	41Z	-40 to +105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6841IUZ (Notes 1, 3)	6841Z	-40 to +105	8 Ld MSOP (Pb-free)	M8.118
ISL6842IBZ (Notes 1, 3)	6842 IBZ	-40 to +105	8 Ld SOIC (Pb-free)	M8.15
ISL6842IRZ-T (Notes 2, 3)	42Z	-40 to +105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6842IUZ (Notes 1, 3)	6842Z	-40 to +105	8 Ld MSOP (Pb-free)	M8.118
ISL6843CBZ (Notes 1, 3)	6843 CBZ	0 to +70	8 Ld SOIC (Pb-free)	M8.15
ISL6843IBZ (Notes 1, 3)	6843 IBZ	-40 to +105	8 Ld SOIC (Pb-free)	M8.15
ISL6843IRZ-T (Notes 2, 3)	43Z	-40 to +105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6843IU-T	6843	-40 to +105	8 Ld MSOP	M8.118
ISL6843IUZ (Notes 1, 3)	6843Z	-40 to +105	8 Ld MSOP (Pb-free)	M8.118
ISL6844IBZ (Notes 1, 3)	6844 IBZ	-40 to +105	8 Ld SOIC (Pb-free)	M8.15
ISL6844IRZ-T (Notes 2, 3)	44Z	-40 to +105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6844IUZ (Notes 1, 3)	6844Z	-40 to +105	8 Ld MSOP (Pb-free)	M8.118
ISL6845IBZ (Notes 1, 3)	6845 IBZ	-40 to +105	8 Ld SOIC (Pb-free)	M8.15
ISL6845IRZ-T (Notes 2, 3)	45Z	-40 to +105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6845IUZ (Notes 1, 3)	6845Z	-40 to +105	8 Ld MSOP (Pb-free)	M8.118
ISL6841EVAL3Z	Evaluation Board			
ISL6844EVAL1Z	Evaluation Board			
ISL6844EVAL2Z	Evaluation Board			
ISL6844EVAL3Z	Evaluation Board			

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Contact Factory for Availability.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845.For more information on MSL please see tech brief TB363.

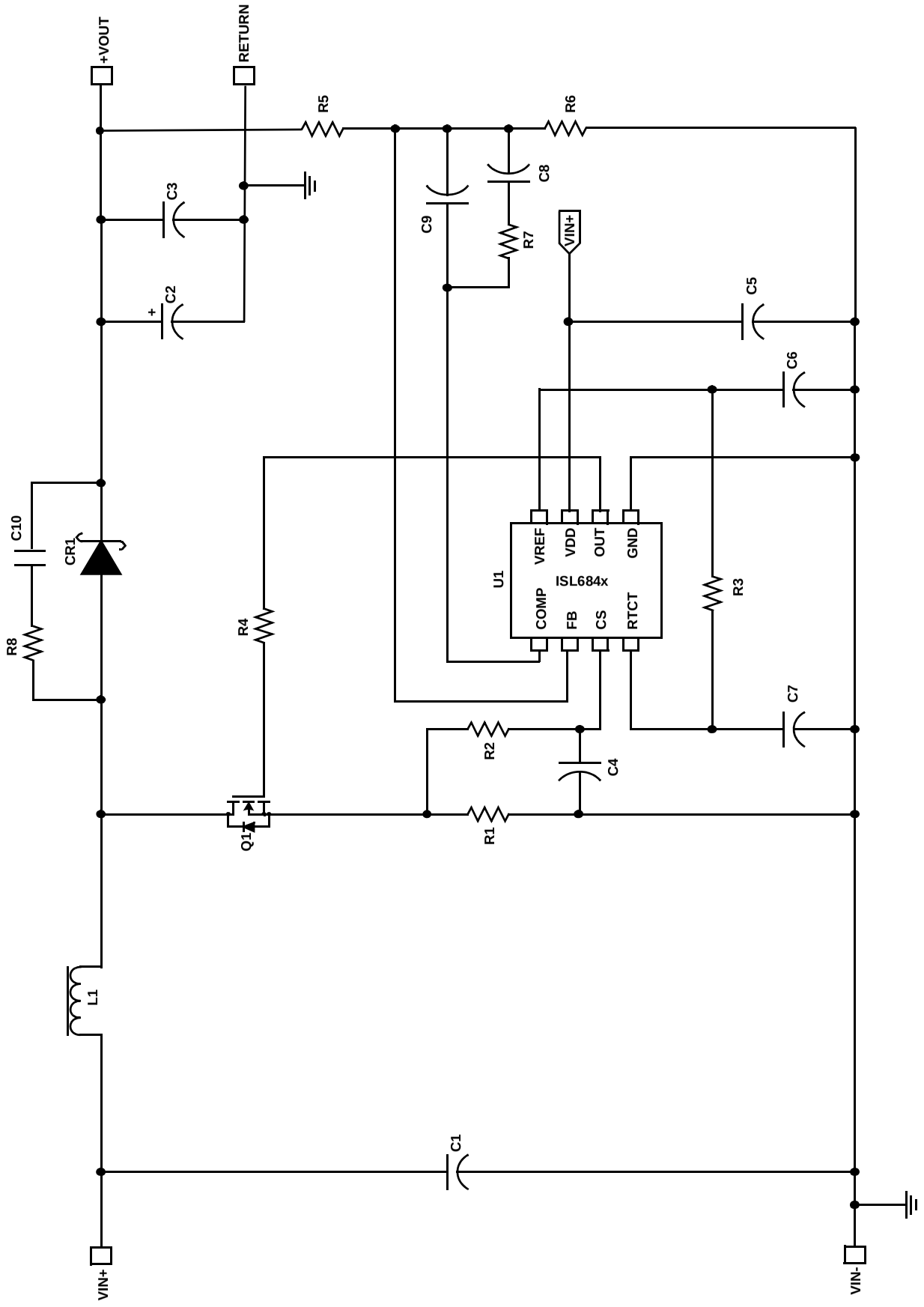
Functional Block Diagram





Typical Application - 48V Input Dual Output Flyback

Typical Application - Boost Converter



Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . GND - 0.3V to +20.0V
OUT . . . . . GND - 0.3V to V_{DD} + 0.3V
Signal Pins . . . . . GND - 0.3V to 6.0V
Peak GATE Current 1A

Operating Conditions

Temperature Range
ISL684xIx . . . . . -40°C to +105°C
ISL684xCx . . . . . 0°C to +70°C
Supply Voltage Range (Typical, Note 8)
ISL6840, ISL6841. . . . . 7.5V to 14V
ISL6843, ISL6845. . . . . 9V to 16V
ISL6842, ISL6844. . . . . 15V to 18V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Notes 5, 6).	77	6
SOIC Package (Note 5)	100	N/A
MSOP Package (Notes 5, 7)	165	62

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the “case temp” location is taken at the package top center.
8. All voltages are with respect to GND.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to “Functional Block Diagram” and “Typical Application” schematic on pages 3 and 4. V_{DD} = 15V (Note 12), R_t = 10kΩ, C_t = 3.3nF, T_A = -40°C to +105°C (Industrial) or T_A = 0°C to +70°C (Commercial), Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C or 0°C to +70°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
UNDERVOLTAGE LOCKOUT					
START Threshold (ISL6840, ISL6841)		**6.5**	7.0	**7.5**	V
START Threshold (ISL6843, ISL6845)		**7.8**	8.4	**9.0**	V
START Threshold (ISL6842, ISL6844)		**13.3**	14.3	**15.3**	V
STOP Threshold (ISL6840, ISL6841)		**6.1**	6.6	**6.9**	V
STOP Threshold (ISL6843, ISL6845)		**6.7**	7.2	**7.7**	V
STOP Threshold **(ISL6843C Only)**		**6.6**	7.2	**7.8**	V
STOP Threshold (ISL6842, ISL6844)		**8.0**	8.8	**9.6**	V
Hysteresis (ISL6840, ISL6841)		-	0.4	-	V
Hysteresis (ISL6843, ISL6845)		-	0.8	-	V
Hysteresis (ISL6842, ISL6844)		-	5.4	-	V
Start-up Current, I_{DD}	V_{DD} < START Threshold	-	60	**100**	µA
Operating Current, I_{DD}	(Note 10)	-	3.3	**4.0**	mA
Operating Supply Current, I_D	Includes 1nF GATE loading	-	4.1	**5.5**	mA
REFERENCE VOLTAGE					
Overall Accuracy	Over line (V_{DD} = 12V to 18V), load, temperature	**4.925**	5.000	**5.050**	V
Overall Accuracy **(ISL6843C Only)**		**4.82**	5.000	**5.18**	V
Long Term Stability	T_A = +125°C, 1000 hours (Note 11)	-	5	-	mV
Fault Voltage		**4.40**	4.65	**4.85**	V
VREF Good Voltage		**4.60**	4.80	**VREF - 0.05**	V
Hysteresis		**50**	165	**250**	mV

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" and "Typical Application" schematic on pages 3 and 4. V_{DD} = 15V (Note 12), R_t = 10kΩ, C_t = 3.3nF, T_A = -40°C to +105°C (Industrial) or T_A = 0°C to +70°C (Commercial), Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C or 0°C to +70°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Current Limit, Sourcing		**-20**	-	-	mA
Current Limit, Sinking		**5**	-	-	mA
CURRENT SENSE					
Input Bias Current	V_{CS} = 1V	**-1.0**	-	**1.0**	µA
CS Offset Voltage	V_{CS} = 0V (Note 11)	**95**	100	**105**	mV
COMP to PWM Comparator Offset Voltage	V_{CS} = 0V (Note 11)	**0.80**	1.15	**1.30**	V
Input Signal, Maximum		**0.91**	0.97	**1.03**	V
Input Signal, Maximum **(ISL6843C Only)**		***0.9***	***0.97***	***1.07***	V
Gain, $A_{CS} = \Delta V_{COMP}/\Delta V_{CS}$	0 < V_{CS} < 910mV, V_{FB} = 0V (Note 11)	**2.5**	3.0	**3.5**	V/V
CS to OUT Delay	(Note 11)	-	25	**40**	ns
CS to OUT Delay **(ISL6843C Only)**	(Note 11)			***70***	ns
ERROR AMPLIFIER					
Open Loop Voltage Gain	(Note 11)	**60**	90	-	dB
Open Loop Voltage Gain **(ISL6843C Only)**	(Note 11)	**55**			dB
Unity Gain Bandwidth	(Note 11)	**3.5**	5	-	MHz
Reference Voltage	$V_{FB} = V_{COMP}$	**2.475**	2.514	**2.55**	V
FB Input Bias Current	V_{FB} = 0V	**-1.0**	-0.2	**1.0**	µA
COMP Sink Current	V_{COMP} = 1.5V, V_{FB} = 2.7V	**1.0**	-	-	mA
COMP Source Current	V_{COMP} = 1.5V, V_{FB} = 2.3V	**-0.4**	-	-	mA
COMP VOH	V_{FB} = 2.3V	**4.80**	-	**VREF**	V
COMP VOL	V_{FB} = 2.7V	**0.4**	-	**1.0**	V
PSRR	Frequency = 120Hz, V_{DD} = 12V to 18V (Note 11)	**60**	80	-	dB
OSCILLATOR					
Frequency Accuracy	Initial, T_J = +25°C	49	52	55	kHz
Frequency Variation with V_{DD}	T = +25°C ($f_{18V} - f_{12V})/f_{12V}$	-	0.2	1.0	%
Temperature Stability	(Note 11)	-	-	**5**	%
Amplitude, Peak-to-Peak		-	1.9	-	V
RTCT Discharge Voltage		-	0.7	-	V
Discharge Current	RTCT = 2.0V	**7.2**	8.4	**9.5**	mA
OUTPUT					
Gate VOH	V_{DD} to OUT, I_{OUT} = -200mA	-	1.0	**2.0**	V
Gate VOL	OUT to GND, I_{OUT} = 200mA	-	1.0	**2.0**	V
Peak Output Current	C_{OUT} = 1nF (Note 11)	-	1.0	-	A
Rise Time	C_{OUT} = 1nF (Note 11)	-	20	**40**	ns
Fall Time	C_{OUT} = 1nF (Note 11)	-	20	**40**	ns
PWM					

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" and "Typical Application" schematic on pages 3 and 4. V_{DD} = 15V (Note 12), R_t = 10kΩ, C_t = 3.3nF, T_A = -40°C to +105°C (Industrial) or T_A = 0°C to +70°C (Commercial), Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C or 0°C to +70°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Maximum Duty Cycle	ISL6840, ISL6842, ISL6843	**94**	96	-	%
	ISL6841, ISL6844, ISL6845	**47**	48	-	%
Minimum Duty Cycle	ISL6840, ISL6842, ISL6843	-	-	**0**	%
	ISL6841, ISL6844, ISL6845	-	-	**0**	%

NOTES:

9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.
11. Limits established by characterization and are not production tested.
12. Adjust V_{DD} above the start threshold and then lower to 15V.

Typical Performance Curves

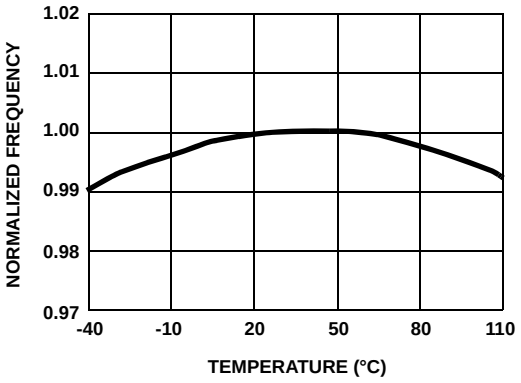


FIGURE 1. FREQUENCY vs TEMPERATURE

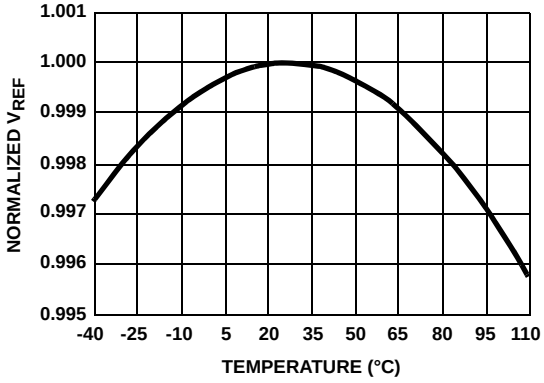


FIGURE 2. REFERENCE VOLTAGE vs TEMPERATURE

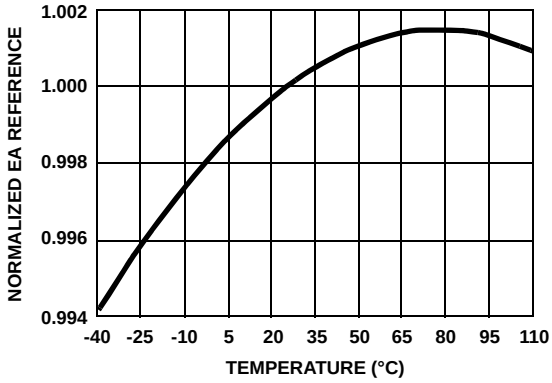


FIGURE 3. EA REFERENCE vs TEMPERATURE

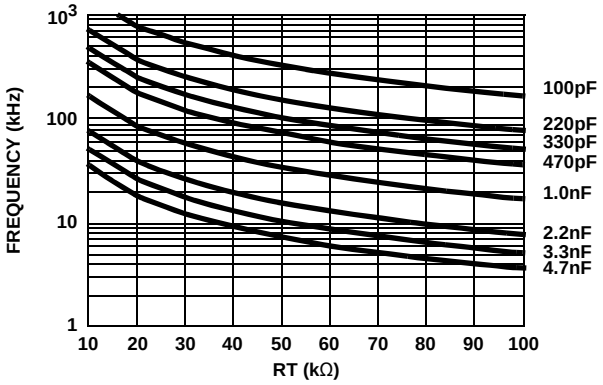


FIGURE 4. RESISTANCE FOR CT CAPACITOR VALUES GIVEN

Pin Descriptions

RTCT - This is the oscillator timing control pin. The operational frequency and maximum duty cycle are set by connecting a resistor, RT, between VREF and this pin and a timing capacitor, CT, from this pin to GND. The oscillator produces a sawtooth waveform with a programmable frequency range up to 2.0MHz. The charge time, t_C, the discharge time, t_D, the switching frequency, f, and the maximum duty cycle, Dmax, can be calculated from Equations 1, 2, 3 and 4:

$$t_C \approx 0.583 \bullet RT \bullet CT \quad \text{(EQ. 1)}$$

$$t_D \approx -RT \bullet CT \bullet \ln\left(\frac{0.0083 \bullet RT - 4.3}{0.0083 \bullet RT - 2.4}\right) \quad \text{(EQ. 2)}$$

$$f = 1/(t_C + t_D) \quad \text{(EQ. 3)}$$

$$D = t_C \bullet f \quad \text{(EQ. 4)}$$

Figure 4 may be used as a guideline in selecting the capacitor and resistor values required for a given frequency.

COMP - COMP is the output of the error amplifier and the input of the PWM comparator. The control loop frequency compensation network is connected between the COMP and FB pins.

FB - The output voltage feedback is connected to the inverting input of the error amplifier through this pin. The non-inverting input of the error amplifier is internally tied to a reference voltage.

CS - This is the current sense input to the PWM comparator. The range of the input signal is nominally 0V to 1.0V and has an internal offset of 100mV.

GND - GND is the power and small signal reference ground for all functions.

OUT - This is the drive output to the power switching device. It is a high current output capable of driving the gate of a power MOSFET with peak currents of 1.0A.

VDD - V_{DD} is the power connection for the device. The total supply current will depend on the load applied to OUT. Total I_{DD} current is the sum of the operating current and the average output current. Knowing the operating frequency, f, and the MOSFET gate charge, Qg, the average output current can be calculated in Equation 5:

$$I_{OUT} = Qg \times f \quad \text{(EQ. 5)}$$

To optimize noise immunity, bypass V_{DD} to GND with a ceramic capacitor as close to the VDD and GND pins as possible.

VREF - The 5.00V reference voltage output. +1.0/-1.5% tolerance over line, load and operating temperature. Bypass to GND with a 0.1µF to 3.3µF capacitor to filter this output as needed.

Functional Description

Features

The ISL684x current mode PWMs make an ideal choice for low-cost flyback and forward topology applications. With its greatly improved performance over industry standard parts, it is the obvious choice for new designs or existing designs which require updating.

Oscillator

The ISL684x family of controllers have a sawtooth oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor from VREF and a capacitor to GND on the RTCT pin. (Please refer to Figure 4 for the resistor and capacitance required for a given frequency.)

Soft-Start Operation

Soft-start must be implemented externally. One method, illustrated in Figure 5, clamps the voltage on COMP.

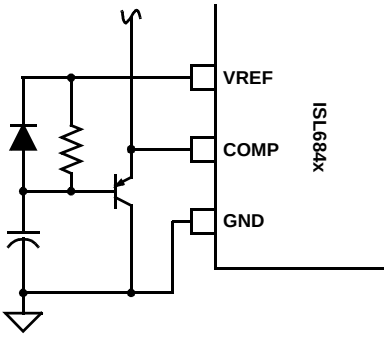


FIGURE 5. SOFT-START

Gate Drive

The ISL684x family are capable of sourcing and sinking 1A peak current. To limit the peak current through the IC, an optional external resistor may be placed between the totem-pole output of the IC (OUT pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation may be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability. The minimum amount of slope compensation required corresponds to 1/2 the inductor downslope. Adding excessive slope compensation, however, results in a control loop that behaves more as a voltage mode controller than as a current mode controller.

Slope compensation may be added to the CS signal shown in Figure 7.

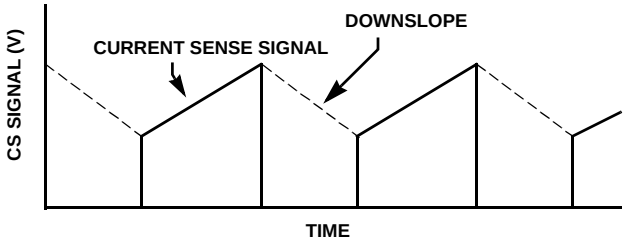


FIGURE 6. CURRENT SENSE DOWNSLOPE

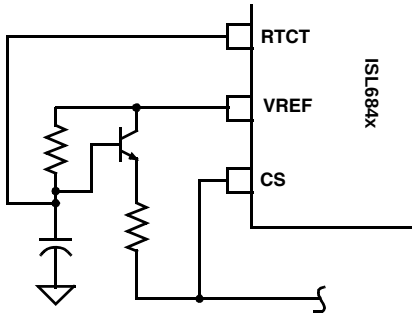


FIGURE 7. SLOPE COMPENSATION

Fault Conditions

A Fault condition occurs if VREF falls below 4.65V. When a Fault is detected, OUT is disabled. When VREF exceeds 4.80V, the Fault condition clears, and OUT is enabled.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. V_{DD} should be bypassed directly to GND with good high frequency capacitors.

Package Outline Drawing

M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

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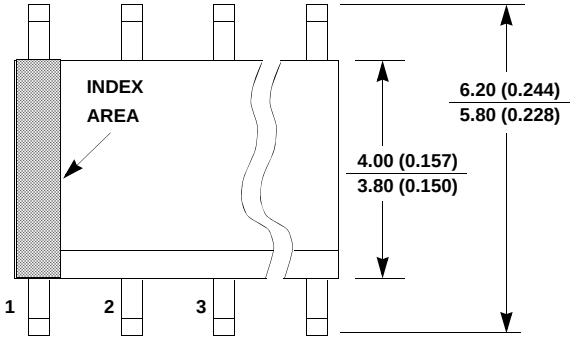
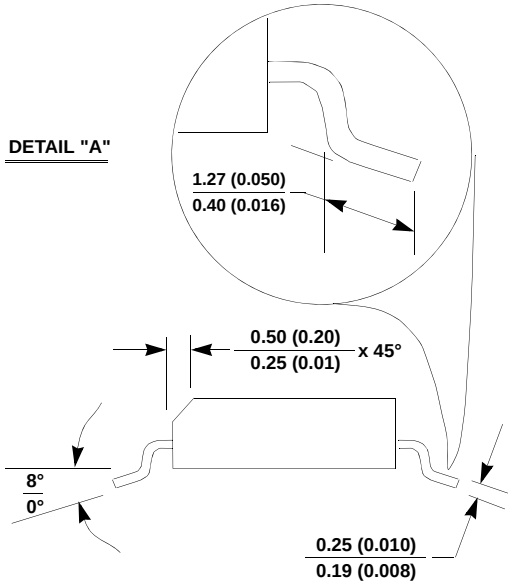
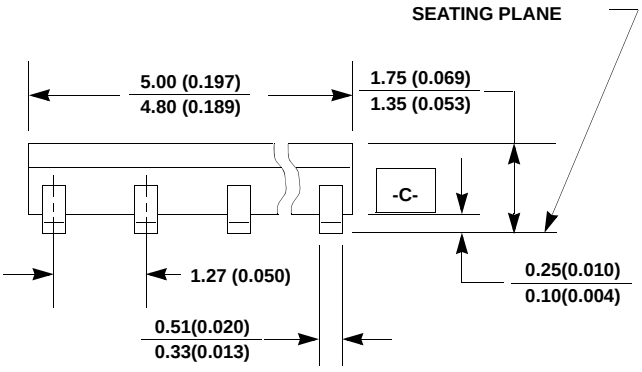


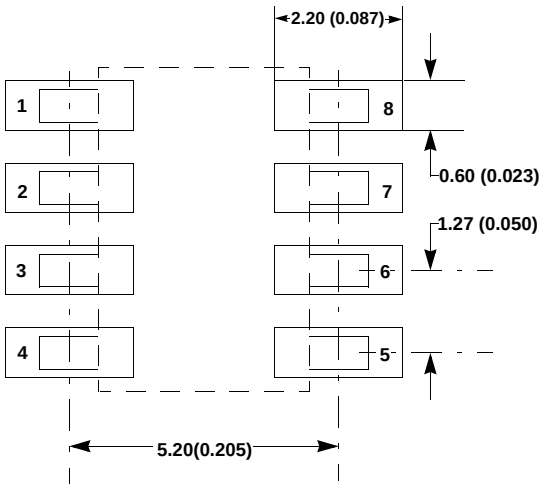
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

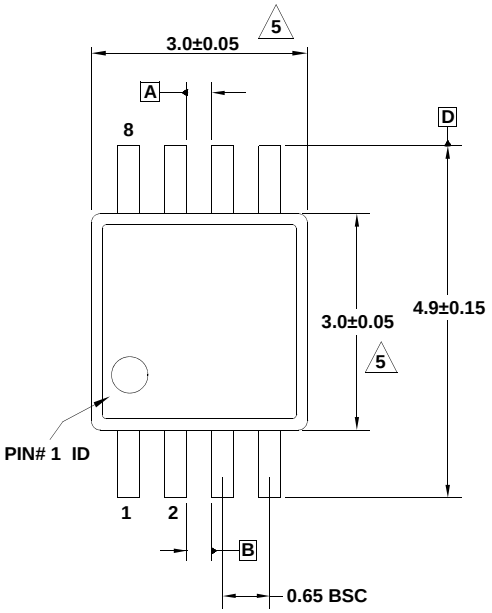
1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Package Outline Drawing

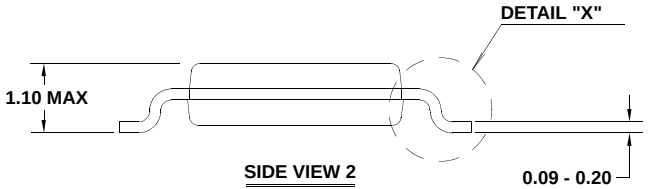
M8.118

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

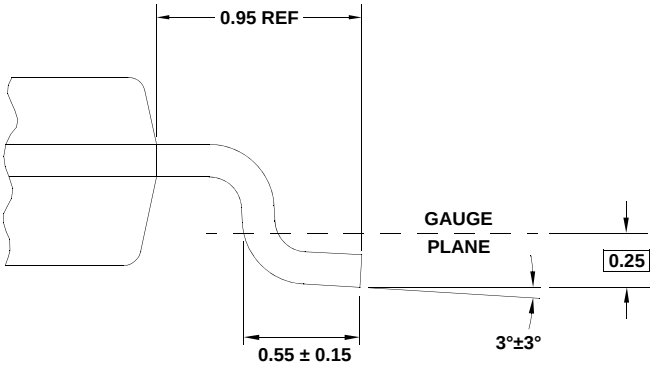
Rev 4, 7/11



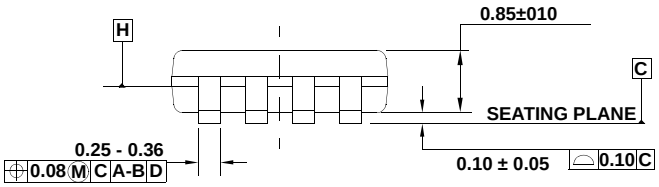
TOP VIEW



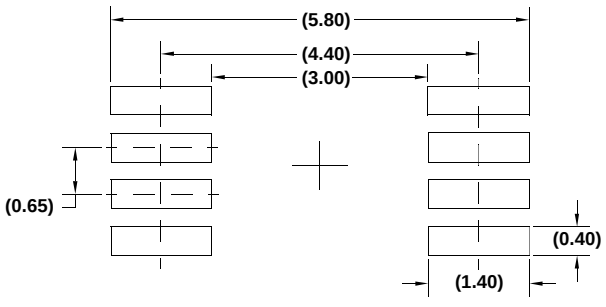
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

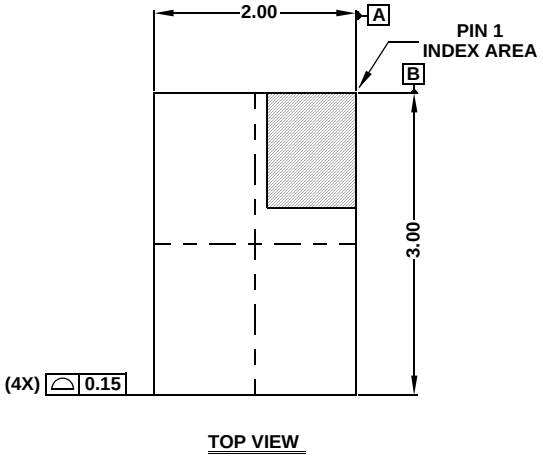
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

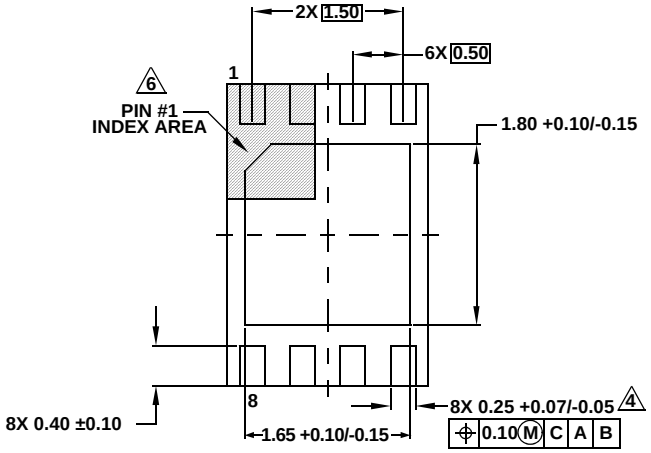
Package Outline Drawing

L8.2x3

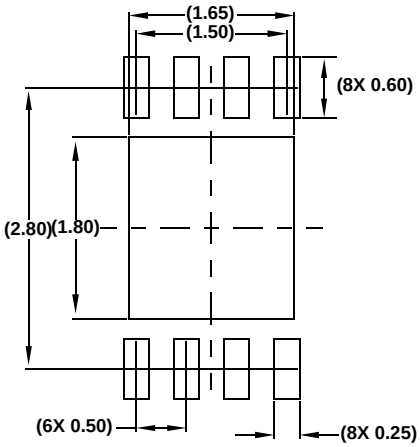
8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 3/10



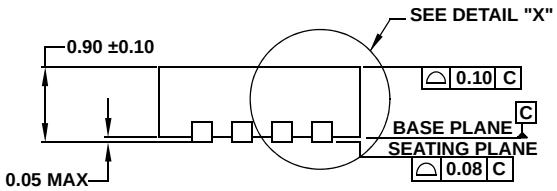
TOP VIEW



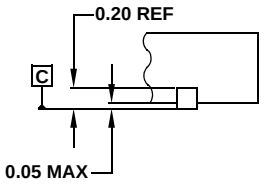
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compies to JEDEC MO-229 VCED-2.