

# 74HC123; 74HCT123

## Dual retriggerable monostable multivibrator with reset

Rev. 9 — 19 January 2015

Product data sheet

### 1. General description

The 74HC123; 74HCT123 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC123; 74HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods:

1. The basic pulse is programmed by selection of an external resistor ( $R_{EXT}$ ) and capacitor ( $C_{EXT}$ ).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ( $n\overline{A}$ ) or the active HIGH-going edge input ( $nB$ ). By repeating this process, the output pulse period ( $nQ = \text{HIGH}$ ,  $n\overline{Q} = \text{LOW}$ ) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input  $n\overline{RD}$ , which also inhibits the triggering.
3. An internal connection from  $n\overline{RD}$  to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input  $n\overline{RD}$  as shown in [Table 3](#).

Schmitt-trigger action in the  $n\overline{A}$  and  $nB$  inputs, makes the circuit highly tolerant to slower input rise and fall times.

The 74HC123; 74HCT123 are identical to the 74HC423; 74HCT423 but can be triggered via the reset input.

### 2. Features and benefits

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

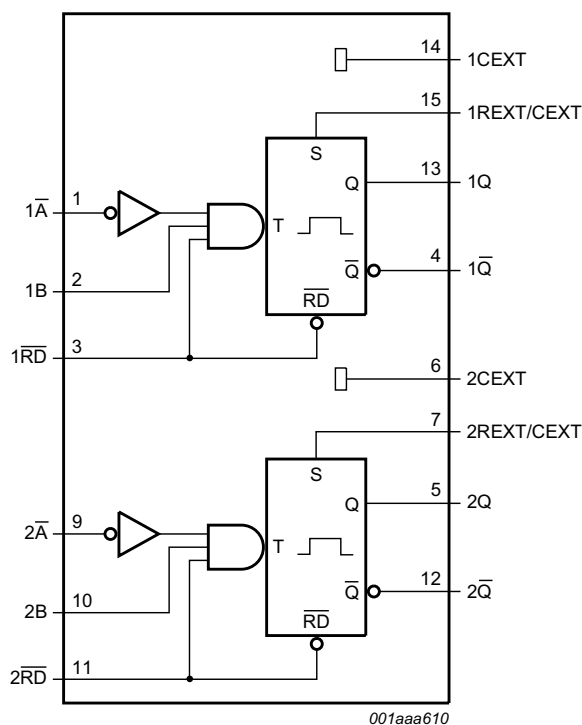


### 3. Ordering information

### Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC123N	−40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT123N				
74HC123D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT123D				
74HC123DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT123DB				
74HC123PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT123PW				
74HC123BQ	−40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

#### 4. Functional diagram



**Fig 1. Functional diagram**

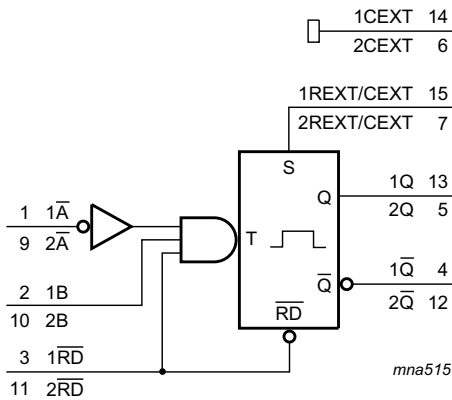


Fig 2. Logic symbol

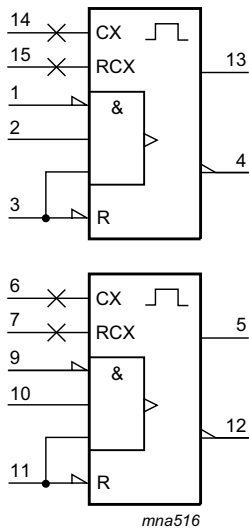


Fig 3. IEC logic symbol

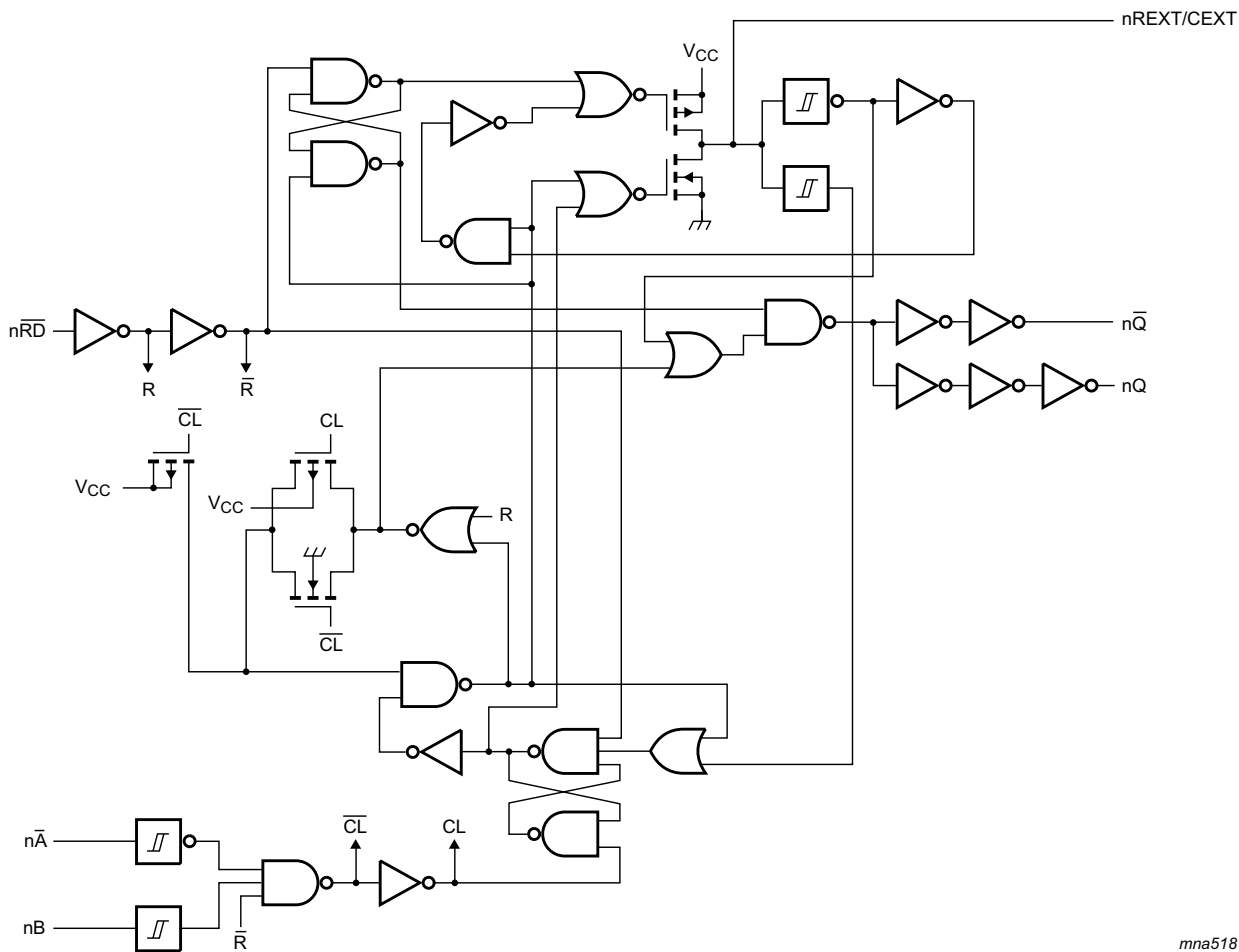
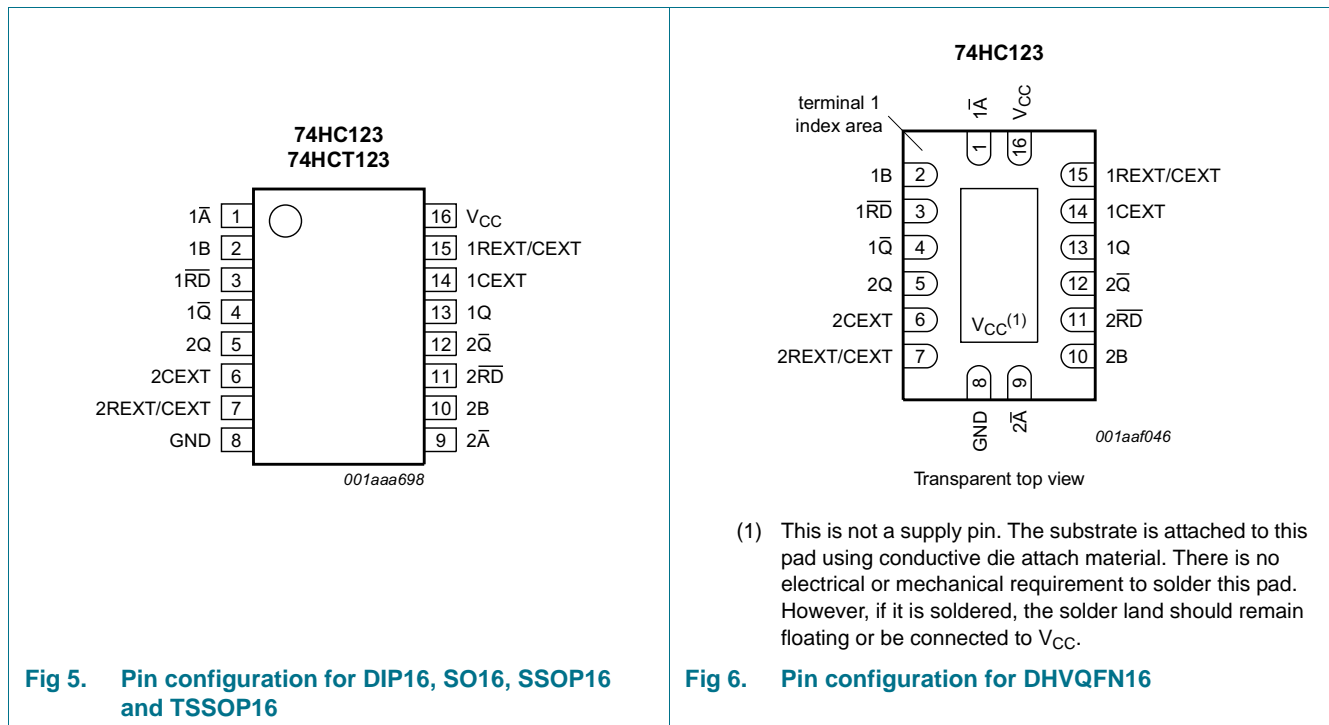


Fig 4. Logic diagram

## 5. Pinning information

### 5.1 Pinning









### 5.2 Pin description

**Table 2. Pin description**



Symbol	Pin	Description
1 $\bar{A}$	1	negative-edge triggered input 1
1B	2	positive-edge triggered input 1
1 $\overline{RD}$	3	direct reset LOW and positive-edge triggered input 1
1 $\bar{Q}$	4	active LOW output 1
2Q	5	active HIGH output 2
2CEXT	6	external capacitor connection 2
2REXT/CEXT	7	external resistor and capacitor connection 2
GND	8	ground (0 V)
2 $\bar{A}$	9	negative-edge triggered input 2
2B	10	positive-edge triggered input 2
2 $\overline{RD}$	11	direct reset LOW and positive-edge triggered input 2
2 $\bar{Q}$	12	active LOW output 2
1Q	13	active HIGH output 1
1CEXT	14	external capacitor connection 1
1REXT/CEXT	15	external resistor and capacitor connection 1
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input			Output	
nRD	nA	nB	nQ	nQ
L	X	X	L	H
X	H	X	L <sup>[2]</sup>	H <sup>[2]</sup>
X	X	L	L <sup>[2]</sup>	H <sup>[2]</sup>
H	L	↑		
H	↓	H		
↑	L	H		

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition;

 = one HIGH level output pulse;  = one LOW level output pulse.

[2] If the monostable was triggered before this condition was established, the pulse will continue as programmed.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>O</sub>	output current	except for pins nREXT/CEXT; V <sub>O</sub> = -0.5 V to (V <sub>CC</sub> + 0.5 V)	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-	-50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation				
	DIP16 package	<sup>[1]</sup>	-	750	mW
	SO16 package	<sup>[2]</sup>	-	500	mW
	SSOP16 package	<sup>[3]</sup>	-	500	mW
	TSSOP16 package	<sup>[3]</sup>	-	500	mW
	DHVQFN16 package	<sup>[4]</sup>	-	500	mW

[1] For DIP16 package: P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 packages: P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN16 package: P<sub>tot</sub> derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC123			74HCT123			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$\Delta t/\Delta V$	input transition rise and fall rate	nRD input							
		$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC123										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = −20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = −20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = −20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = −4 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = −5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	μA

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT123</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = –20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = –4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; I <sub>O</sub> = 0 A; V <sub>I</sub> = V <sub>CC</sub> – 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V								
		pins nA, nB	-	35	125	-	160	-	170	µA
		pin nRD	-	50	180	-	225	-	245	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC123										
t <sub>pd</sub>	propagation delay	nRD, nA, nB to nQ or nQ; <a href="#">[1]</a> C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 kΩ; see <a href="#">Figure 9</a>								
		V <sub>CC</sub> = 2.0 V	-	83	255	-	320	-	385	ns
		V <sub>CC</sub> = 4.5 V	-	30	51	-	64	-	77	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	26	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	24	43	-	54	-	65	ns
		nRD (reset) to nQ or nQ; C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 kΩ; see <a href="#">Figure 9</a>								
		V <sub>CC</sub> = 2.0 V	-	66	215	-	270	-	325	ns
		V <sub>CC</sub> = 4.5 V	-	24	43	-	54	-	65	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	20	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	19	37	-	46	-	55	ns
t <sub>t</sub>	transition time	see <a href="#">Figure 9</a> <a href="#">[1]</a>								
		V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns
t <sub>w</sub>	pulse width	nA LOW; see <a href="#">Figure 10</a>								
		V <sub>CC</sub> = 2.0 V	100	8	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	20	3	-	25	-	30	-	ns
		V <sub>CC</sub> = 6.0 V	17	2	-	21	-	26	-	ns
		nB HIGH; see <a href="#">Figure 10</a>								
		V <sub>CC</sub> = 2.0 V	100	17	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	20	6	-	25	-	30	-	ns
		V <sub>CC</sub> = 6.0 V	17	5	-	21	-	26	-	ns
		nRD LOW; see <a href="#">Figure 11</a>								
		V <sub>CC</sub> = 2.0 V	100	14	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	20	5	-	25	-	30	-	ns
		V <sub>CC</sub> = 6.0 V	17	4	-	21	-	26	-	ns
		nQ HIGH and nQ LOW; <a href="#">[2]</a> V <sub>CC</sub> = 5.0 V; see <a href="#">Figure 10</a> and <a href="#">11</a>								
		C <sub>EXT</sub> = 100 nF; R <sub>EXT</sub> = 10 kΩ	-	450	-	-	-	-	-	μs
		C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 kΩ	-	75	-	-	-	-	-	ns



**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_{\text{trig}}$	retrigger time	$\overline{nA}$ , nB; $C_{\text{EXT}} = 0$ pF; $R_{\text{EXT}} = 5$ k $\Omega$ ; $V_{\text{CC}} = 5.0$ V; see <a href="#">Figure 10</a> <a href="#">[3][4]</a>	-	110	-	-	-	-	-	ns
$R_{\text{EXT}}$	external timing resistor	see <a href="#">Figure 7</a>								
		$V_{\text{CC}} = 2.0$ V	10	-	1000	-	-	-	-	k $\Omega$
		$V_{\text{CC}} = 5.0$ V	2	-	1000	-	-	-	-	k $\Omega$
$C_{\text{EXT}}$	external timing capacitor	$V_{\text{CC}} = 5.0$ V; see <a href="#">Figure 7</a> <a href="#">[4]</a>	-	-	-	-	-	-	-	pF
$C_{\text{PD}}$	power dissipation capacitance	per monostable; $V_I = \text{GND to } V_{\text{CC}}$ <a href="#">[5]</a>	-	54	-	-	-	-	-	pF
<b>74HCT123</b>										
$t_{\text{PHL}}$	HIGH to LOW propagation delay	$\overline{nRD}$ , $\overline{nA}$ , nB to nQ or $\overline{nQ}$ ; $C_{\text{EXT}} = 0$ pF; $R_{\text{EXT}} = 5$ k $\Omega$ ; see <a href="#">Figure 9</a>								
		$V_{\text{CC}} = 4.5$ V	-	30	51	-	64	-	77	ns
		$V_{\text{CC}} = 5$ V; $C_L = 15$ pF	-	26	-	-	-	-	-	ns
		$\overline{nRD}$ (reset) to nQ or $\overline{nQ}$ ; $C_{\text{EXT}} = 0$ pF; $R_{\text{EXT}} = 5$ k $\Omega$ ; see <a href="#">Figure 9</a>								
		$V_{\text{CC}} = 4.5$ V	-	27	46	-	58	-	69	ns
		$V_{\text{CC}} = 5$ V; $C_L = 15$ pF	-	23	-	-	-	-	-	ns
$t_{\text{PLH}}$	LOW to HIGH propagation delay	$\overline{nRD}$ , $\overline{nA}$ , nB to nQ or $\overline{nQ}$ ; $C_{\text{EXT}} = 0$ pF; $R_{\text{EXT}} = 5$ k $\Omega$ ; see <a href="#">Figure 9</a>								
		$V_{\text{CC}} = 4.5$ V	-	28	51	-	64	-	77	ns
		$V_{\text{CC}} = 5$ V; $C_L = 15$ pF	-	26	-	-	-	-	-	ns
		$\overline{nRD}$ (reset) to nQ or $\overline{nQ}$ ; $C_{\text{EXT}} = 0$ pF; $R_{\text{EXT}} = 5$ k $\Omega$ ; see <a href="#">Figure 9</a>								
		$V_{\text{CC}} = 4.5$ V	-	23	46	-	58	-	69	ns
		$V_{\text{CC}} = 5$ V; $C_L = 15$ pF	-	23	-	-	-	-	-	ns
$t_t$	transition time	$V_{\text{CC}} = 4.5$ V; see <a href="#">Figure 9</a> <a href="#">[1]</a>	-	7	15	-	19	-	22	ns

**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_W$	pulse width	$V_{CC} = 4.5$ V								
		nA LOW; see <a href="#">Figure 10</a>	20	3	-	25	-	30	-	ns
		nB HIGH; see <a href="#">Figure 10</a>	20	5	-	25	-	30	-	ns
		nRD LOW; see <a href="#">Figure 11</a>	20	7	-	25	-	30	-	ns
		nQ HIGH and nQ LOW; <a href="#">[2]</a> $V_{CC} = 5.0$ V; see <a href="#">Figure 10</a> and <a href="#">11</a>								
		$C_{EXT} = 100$ nF; $R_{EXT} = 10$ kΩ	-	450	-	-	-	-	-	μs
$t_{trig}$	retrigger time	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ kΩ; $V_{CC} = 5.0$ V; see <a href="#">Figure 10</a>	-	110	-	-	-	-	-	ns
$R_{EXT}$	external timing resistor	$V_{CC} = 5.0$ V; see <a href="#">Figure 7</a>	2	-	1000	-	-	-	-	kΩ
$C_{EXT}$	external timing capacitor	$V_{CC} = 5.0$ V; see <a href="#">Figure 7</a> <a href="#">[4]</a>	-	-	-	-	-	-	-	pF
$C_{PD}$	power dissipation capacitance	per monostable; <a href="#">[5]</a> $V_I = GND$ to $V_{CC} - 1.5$ V	-	56	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ ;  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$

[2] For other  $R_{EXT}$  and  $C_{EXT}$  combinations see [Figure 7](#). If  $C_{EXT} > 10$  nF, the next formula is valid.

$t_W = K \times R_{EXT} \times C_{EXT}$ , where:

$t_W$  = typical output pulse width in ns;

$R_{EXT}$  = external resistor in kΩ;

$C_{EXT}$  = external capacitor in pF;

$K$  = constant = 0.45 for  $V_{CC} = 5.0$  V and 0.55 for  $V_{CC} = 2.0$  V.

The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7 pF.

[3] The time to retrigger the monostable multivibrator depends on the values of  $R_{EXT}$  and  $C_{EXT}$ . The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If  $C_{EXT} > 10$  pF, the next formula (at  $V_{CC} = 5.0$  V) for the setup time of a retrigger pulse is valid:

$t_{trig} = 30 + 0.19 \times R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$ , where:

$t_{trig}$  = retrigger time in ns;

$C_{EXT}$  = external capacitor in pF;  $R_{EXT}$  = external resistor in kΩ.

The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7 pF.

[4] When the device is powered-up, initiate the device via a reset pulse, when  $C_{EXT} < 50$  pF.

[5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

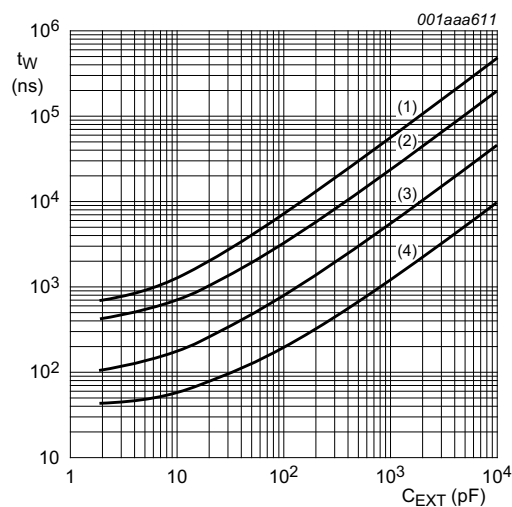
$D$  = duty factor in %;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

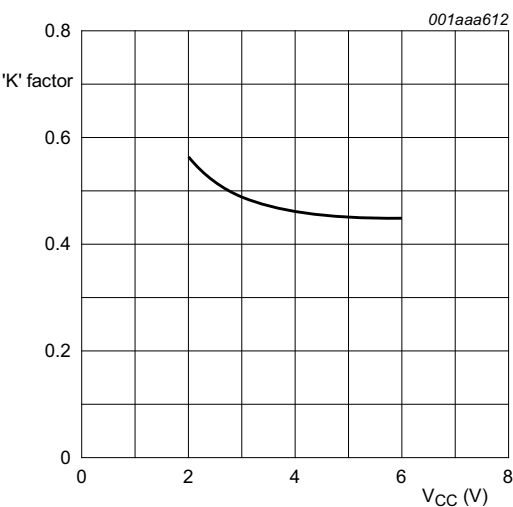
$C_{EXT}$  = timing capacitance in pF;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  sum of outputs.



$V_{CC} = 5.0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .  
(1)  $R_{EXT} = 100\text{ k}\Omega$   
(2)  $R_{EXT} = 50\text{ k}\Omega$   
(3)  $R_{EXT} = 10\text{ k}\Omega$   
(4)  $R_{EXT} = 2\text{ k}\Omega$

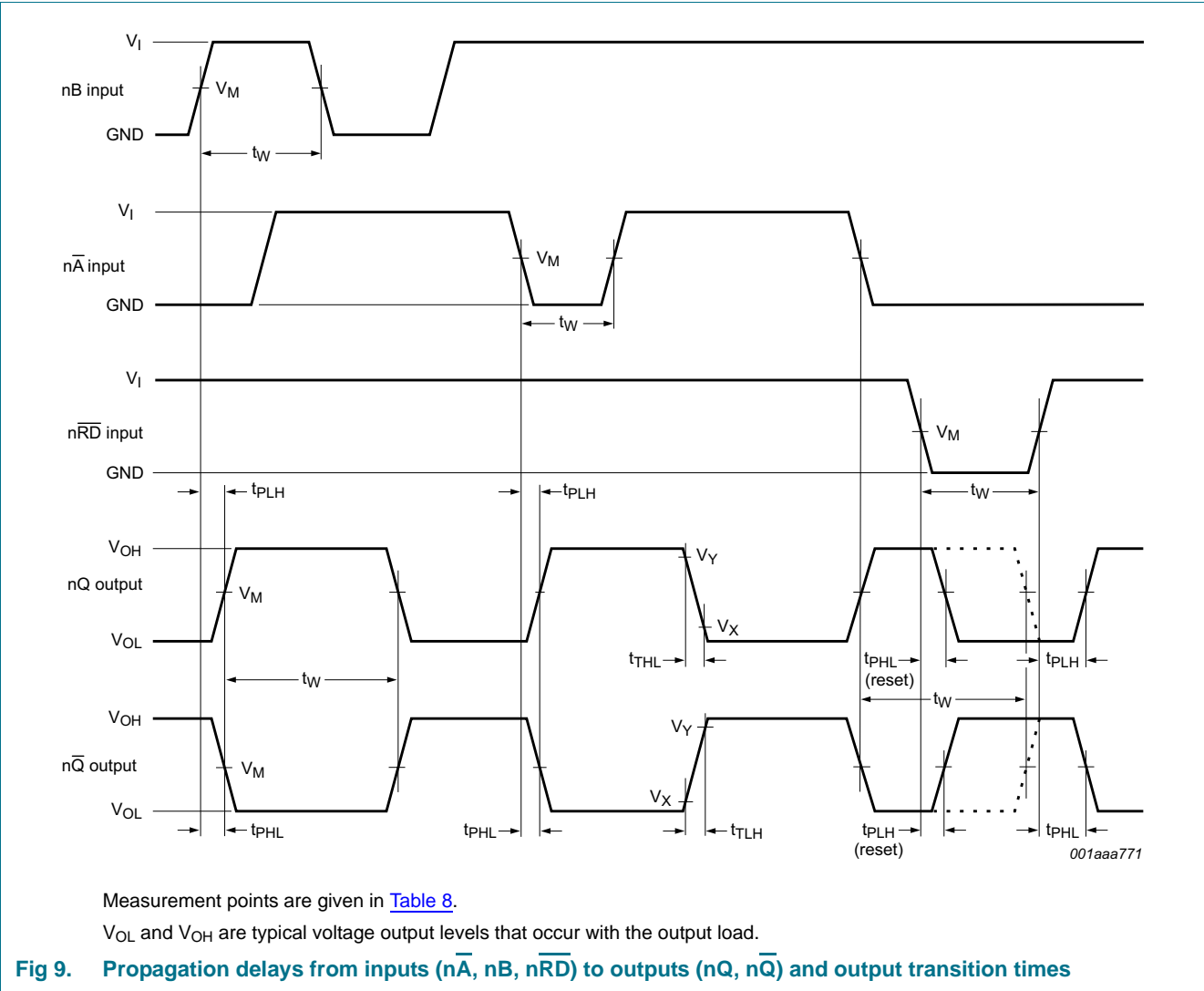
**Fig 7. Typical output pulse width as a function of the external capacitor value**

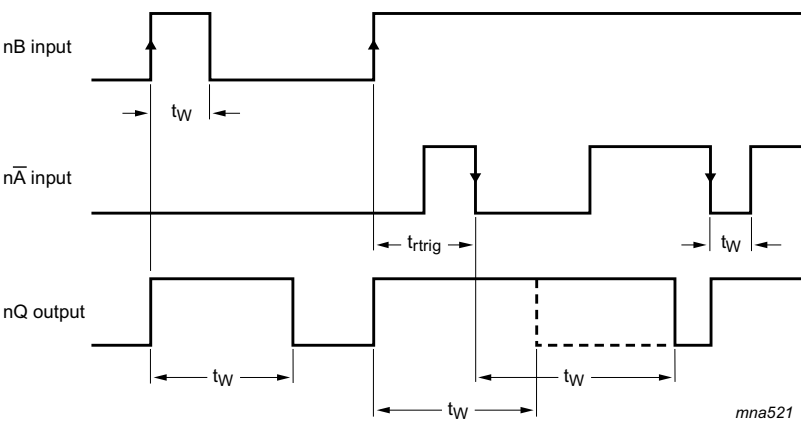


$C_{EXT} = 10\text{ nF}$ ;  $R_{EXT} = 10\text{ k}\Omega$  to  $100\text{ k}\Omega$ .  
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

**Fig 8. 74HC123 typical 'K' factor as function of  $V_{CC}$**

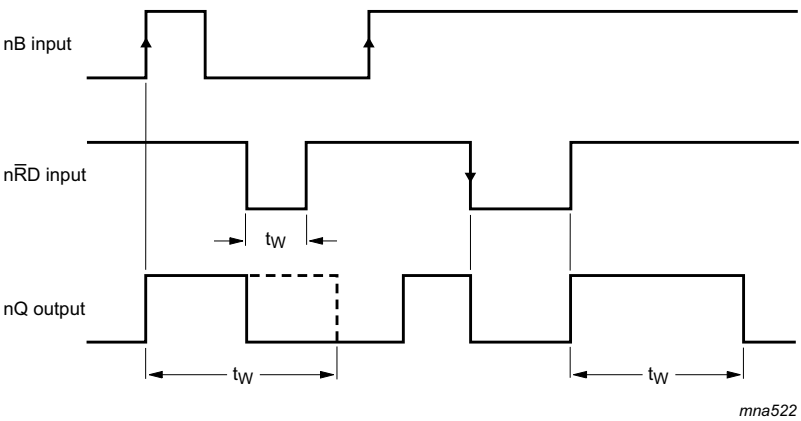
11. Waveforms





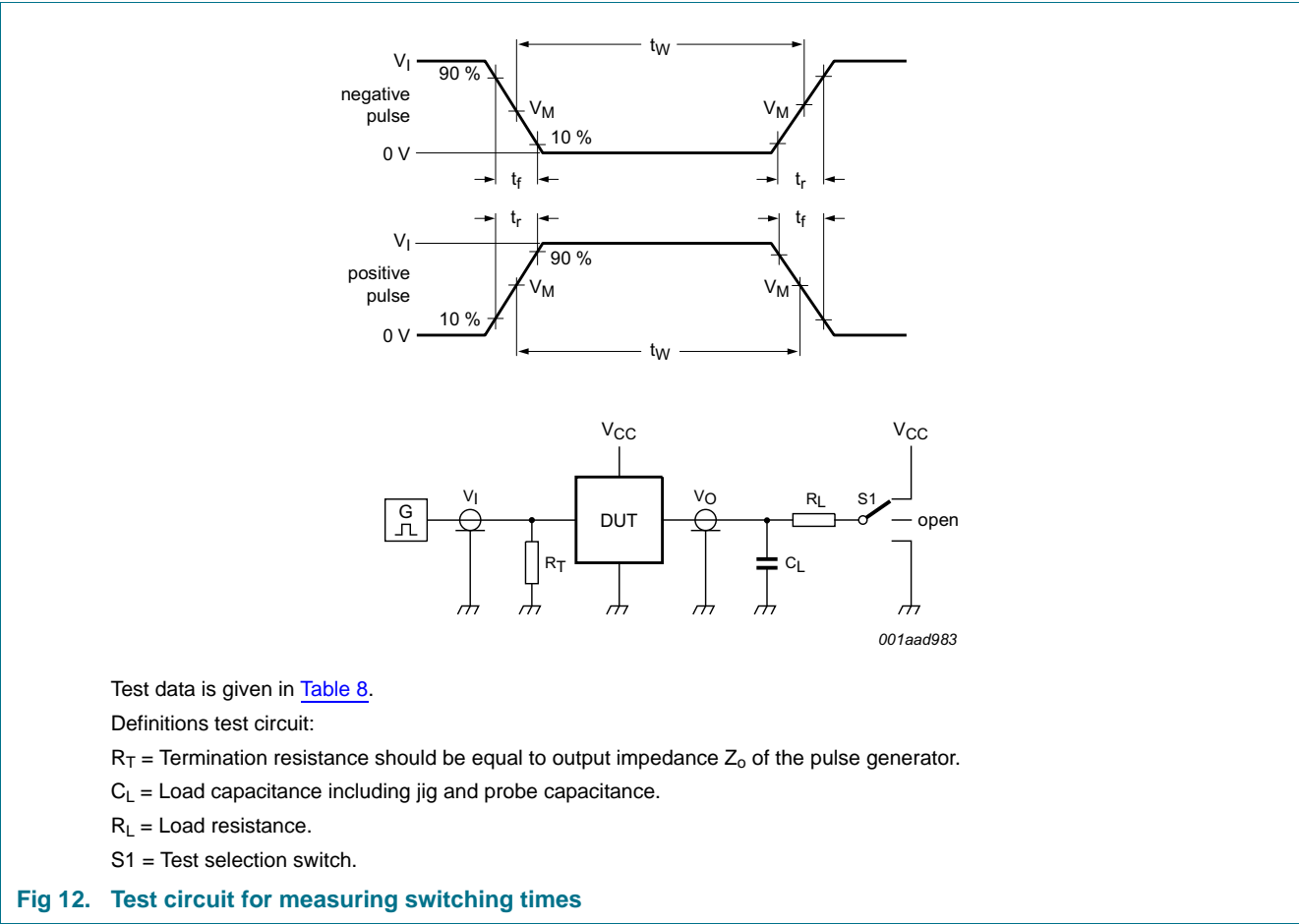
$\overline{nRD} = \text{HIGH}$

Fig 10. Output pulse control using retrigger pulse



$\overline{nA} = \text{LOW}$

Fig 11. Output pulse control using reset input  $\overline{nRD}$



Test data is given in [Table 8](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

$S1$  = Test selection switch.

Fig 12. Test circuit for measuring switching times

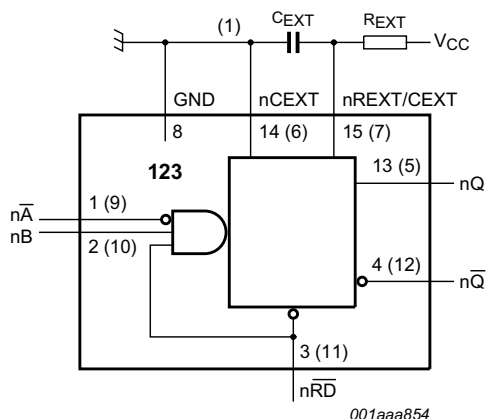
Table 8. Test data

Type	Input		Load		S1 position
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	
74HC123	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open
74HCT123	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open

## 12. Application information

### 12.1 Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components  $R_{EXT}$  and  $C_{EXT}$ .

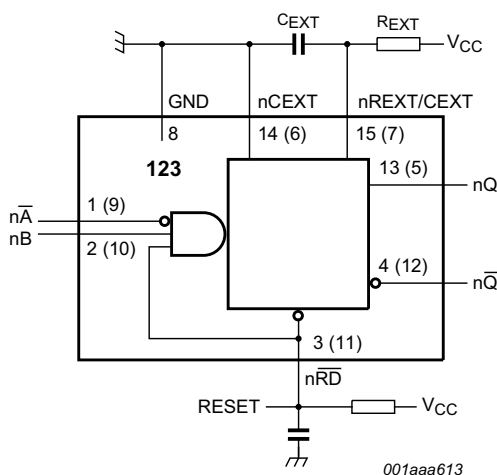


(1) For minimum noise generation it is recommended to ground pins 6 (2CEXT) and 14 (1CEXT) externally to pin 8 (GND).

**Fig 13. Timing component connections**

### 12.2 Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of  $R_{EXT}$  and  $C_{EXT}$ . This output pulse can be eliminated using the circuit shown in [Figure 14](#).



**Fig 14. Power-up output pulse elimination circuit**

### 12.3 Power-down considerations

A large capacitor  $C_{EXT}$  may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of  $V_{CC}$  to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode ( $D_{EXT}$ ) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in [Figure 15](#).

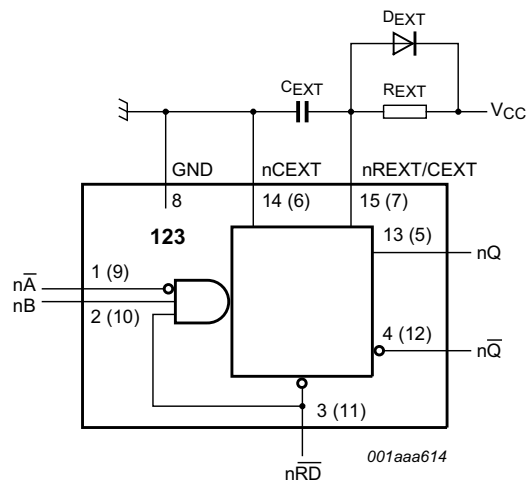


Fig 15. Power-down protection circuit



13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

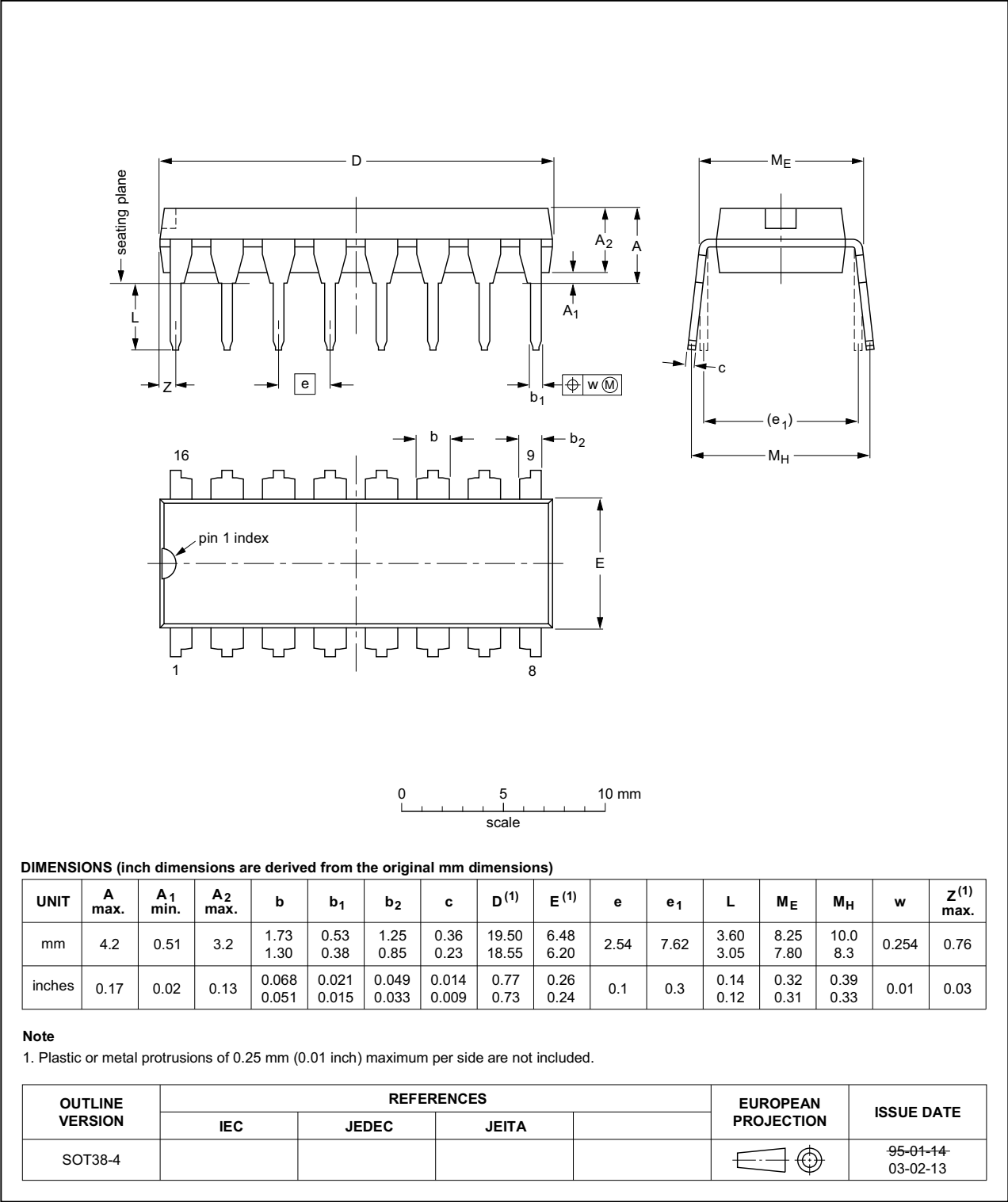


Fig 16. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

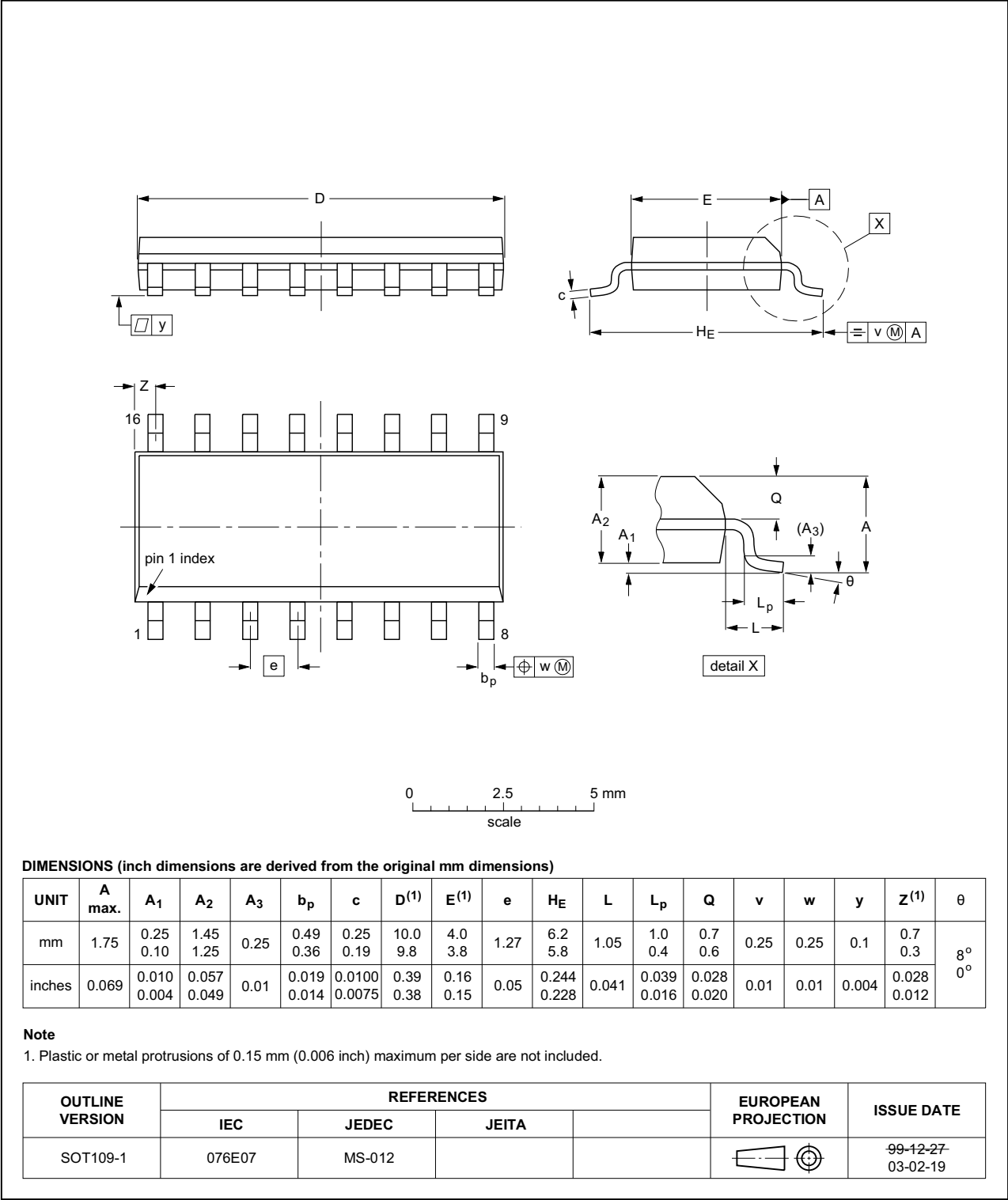


Fig 17. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

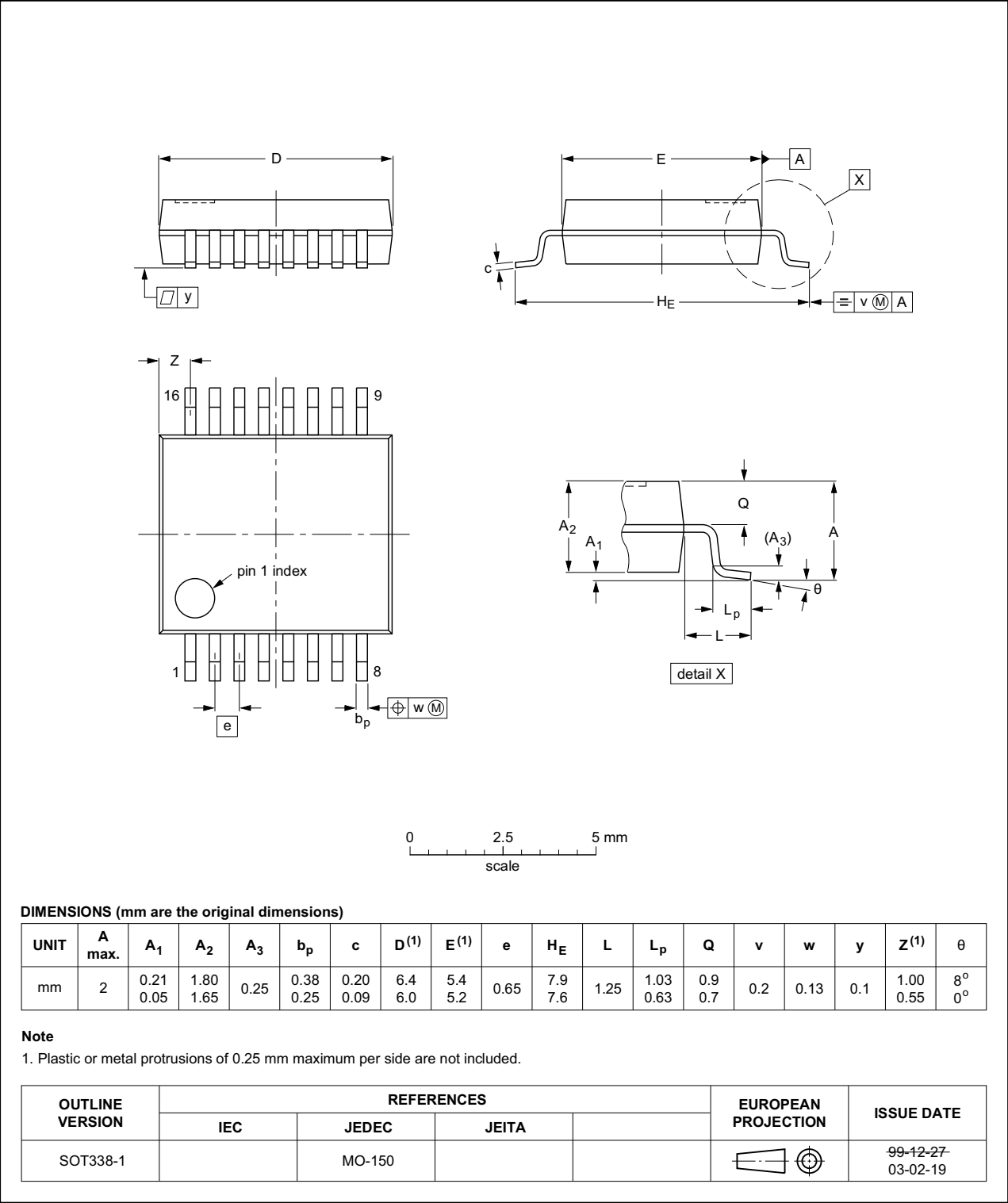


Fig 18. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

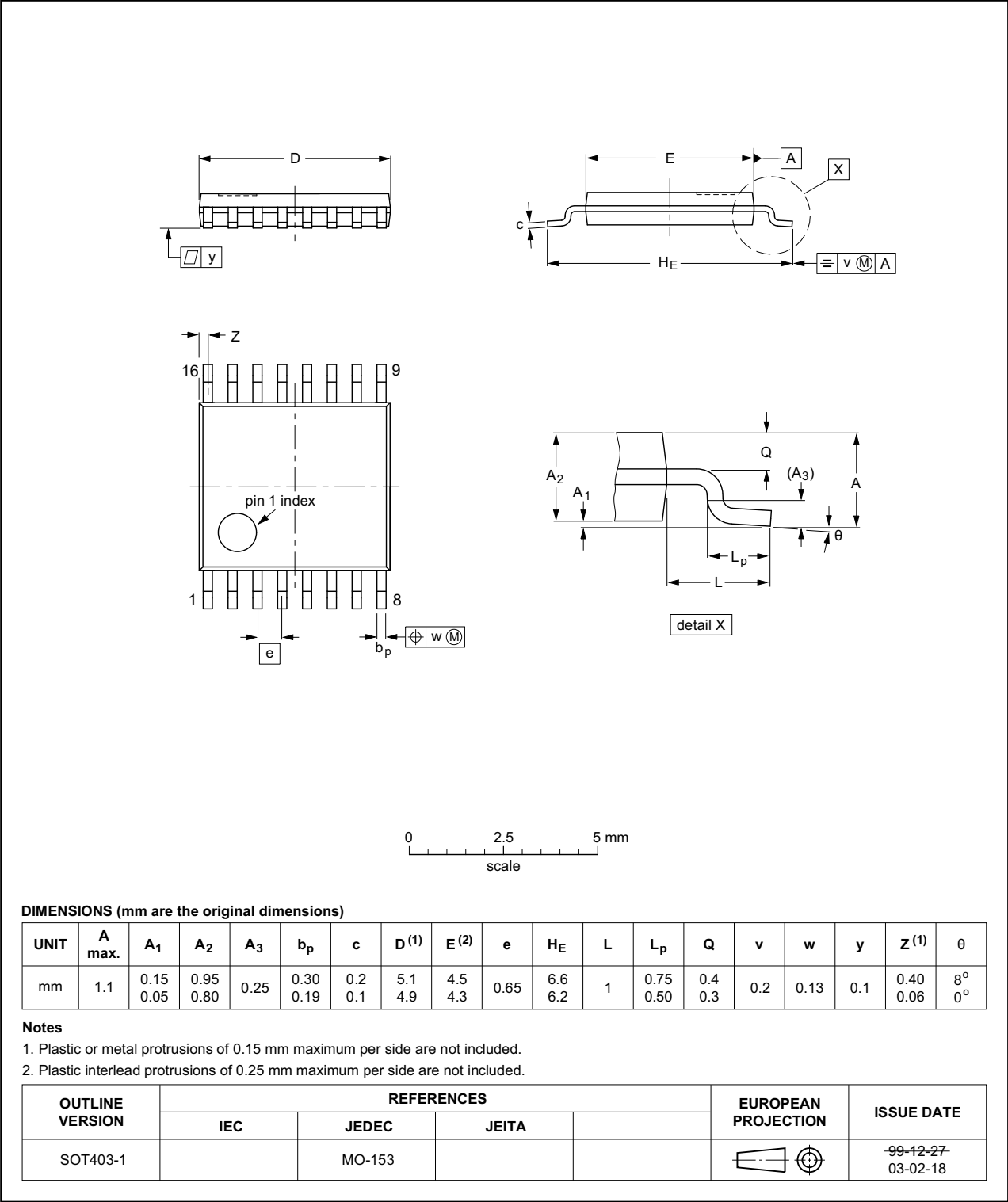


Fig 19. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

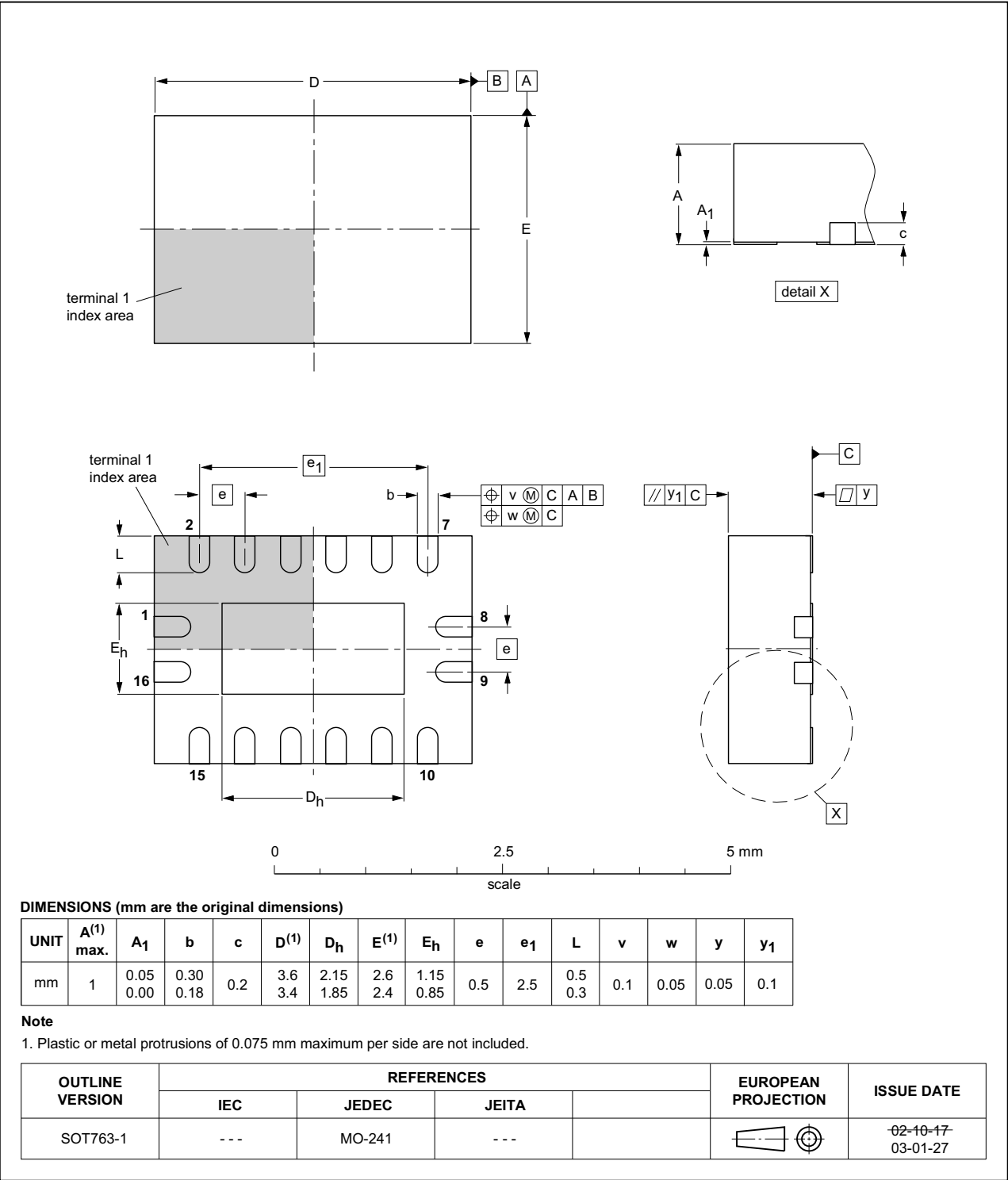


Fig 20. Package outline SOT763-1 (DHVQFN16)

## 14. Abbreviations

Table 9. Abbreviations

Acronym	Abbreviation
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

## 15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT123 v.9	20150119	Product data sheet	-	74HC_HCT123 v.8
Modifications:	• <a href="#">Table 7</a> : Power dissipation capacitance condition for 74HCT123 is corrected.			
74HC_HCT123 v.8	20111216	Product data sheet	-	74HC_HCT123 v.7
Modifications:	• Legal pages updated.			
74HC_HCT123 v.7	20110825	Product data sheet	-	74HC_HCT123 v.6
74HC_HCT123 v.6	20110314	Product data sheet	-	74HC_HCT123 v.5
74HC_HCT123 v.5	20090713	Product data sheet	-	74HC_HCT123 v.4
74HC_HCT123 v.4	20060616	Product data sheet	-	74HC_HCT123 v.3
74HC_HCT123 v.3	20040511	Product specification	-	74HC_HCT123_CNV v.2
74HC_HCT123_CNV v.2	19980708	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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## 18. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>4</b>
5.1	Pinning .....	4
5.2	Pin description .....	4
<b>6</b>	<b>Functional description</b> .....	<b>5</b>
<b>7</b>	<b>Limiting values</b> .....	<b>5</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>6</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>6</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>8</b>
<b>11</b>	<b>Waveforms</b> .....	<b>12</b>
<b>12</b>	<b>Application information</b> .....	<b>15</b>
12.1	Timing component connections .....	15
12.2	Power-up considerations .....	15
12.3	Power-down considerations .....	16
<b>13</b>	<b>Package outline</b> .....	<b>17</b>
<b>14</b>	<b>Abbreviations</b> .....	<b>22</b>
<b>15</b>	<b>Revision history</b> .....	<b>22</b>
<b>16</b>	<b>Legal information</b> .....	<b>23</b>
16.1	Data sheet status .....	23
16.2	Definitions .....	23
16.3	Disclaimers .....	23
16.4	Trademarks .....	24
<b>17</b>	<b>Contact information</b> .....	<b>24</b>
<b>18</b>	<b>Contents</b> .....	<b>25</b>

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