FAIRCHILD SEMICONDUCTOR™

June 2003
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FIN3385 • FIN3386, FIN3383 • FIN3384, FIN3365 • FIN3366, FIN3363 • FIN3364

Low Voltage 24/18 Bit Flat Panel Display Link Serializers/De-Serializers

General Description

The FIN3385/FIN3383/FIN3365/FIN3363 transforms 28/21 bit wide parallel LVTTL (Low Voltage TTL) data into 4/3 serial LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data steam over a separate LVDS link. Every cycle of transmit clock 28/21 bits of input LVTTL data are sampled and transmitted.

The FIN3386/FIN3384/FIN3366/FIN3364 receives and converts the 4/3 serial LVDS data streams back into 28/21 bits of LVTTL data. Refer to Table 1 for a matrix summary of the Serializers and De-serializers available. For the FIN3385, at a transmit clock frequency of 85 MHz, 28 bits of LVTTL data are transmitted at a rate of 595 Mbps per LVDS channel.

These chipsets are an ideal solution to solve EMI and cable size problems associated with wide and high-speed TTL interfaces.

Features

- Low power consumption
- 20 MHz to 85 MHz shift clock support
- 50% duty cycle on the clock output of receiver
- ±1V common-mode range around 1.2V
- Narrow bus reduces cable size and cost
- High throughput (up to 2.38 Gbps throughput)
- Internal PLL with no external component
- Compatible with TIA/EIA-644 specification
- Devices are offered in 48- and 56-lead TSSOP packages

Ordering Code:

Order Number	Package Number	Package Description
FIN3363MTD (Preliminary)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
FIN3364MTD (Preliminary)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
FIN3365MTD (Preliminary)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
FIN3366MTD (Preliminary)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
FIN3383MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
FIN3384MTD (Preliminary)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
FIN3385MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
FIN3386MTD (Preliminary)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

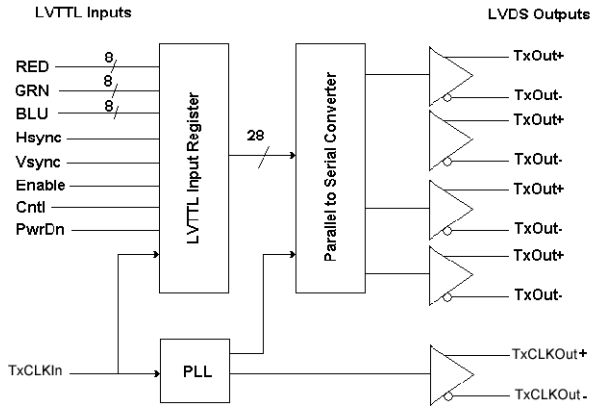
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

TABLE 1. Display Panel Link Serializers/De-Serializers Chip Matrix

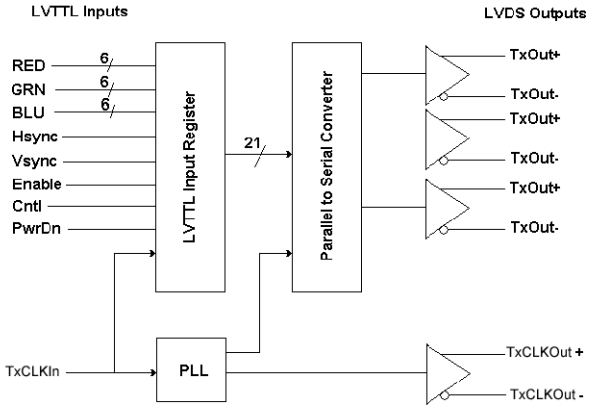
Part	CLK Frequency	LVTTL IN	LVDS OUT	LVDS IN	LVTTL OUT	Package
FIN3385	85	28	4			56 TSSOP
FIN3386	85			4	28	56 TSSOP
FIN3383	66	28	4			56 TSSOP
FIN3384	66			4	28	56 TSSOP
FIN3365	85	21	3			48 TSSOP
FIN3366	85			3	21	48 TSSOP
FIN3363	66	21	3			48 TSSOP
FIN3364	66			3	21	48 TSSOP

Block Diagrams

Transmitter Functional Diagram for FIN3385 and FIN3383

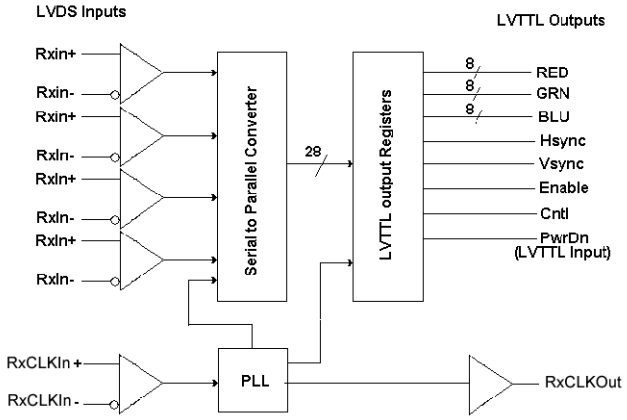


Transmitter Functional Diagram for FIN3365 and FIN3363

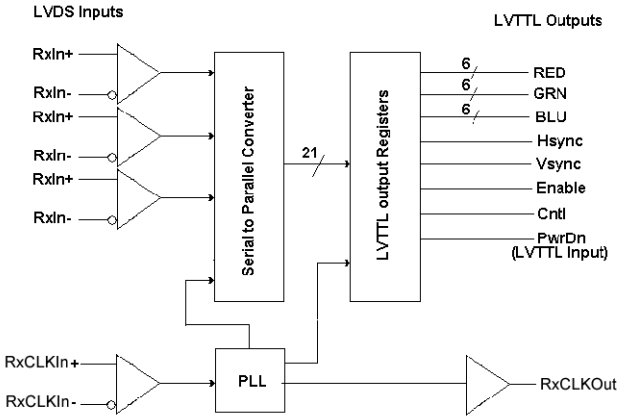


Block Diagrams (Continued)

Receiver Functional Diagram for FIN3386 and FIN3384



Receiver Functional Diagram for FIN3366 and FIN3364



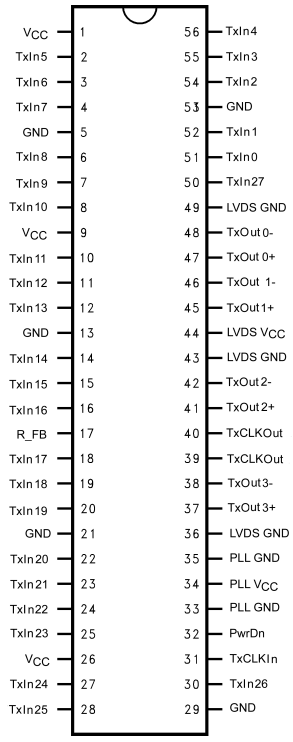
Transmitters

Pin Descriptions

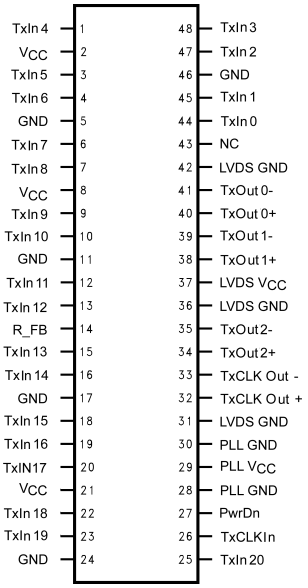
Pin Names	I/O Type	Number of Pins	Description of Signals
TxIn	I	28/21	LVTTL Level Inputs
TxCLKIn	I	1	LVTTL Level Clock Input The rising edge is for data strobe.
TxOut+	O	4/3	Positive LVDS Differential Data Output
TxOut–	O	4/3	Negative LVDS Differential Data Output
TxCLKOut+	O	1	Positive LVDS Differential Clock Output
TxCLKOut–	O	1	Negative LVDS Differential Clock Output
R_FB	I	1	Rising Edge Clock (HIGH), Falling Edge Clock (LOW)
PwrDn	I	1	LVTTL Level Power-Down Input Assertion (LOW) puts the outputs in high-impedance state.
PLL V_{CC}	I	1	Power Supply Pin for PLL
PLL GND	I	2	Ground Pins for PLL
LVDS V_{CC}	I	1	Power Supply Pin for LVDS Outputs
LVDS GND	I	3	Ground Pins for LVDS Outputs
V_{CC}	I	3	Power Supply Pins for LVTTL Inputs
GND	I	5	Ground pins for LVTTL Inputs
NC			No Connect

Connection Diagrams

FIN3385 and FIN3383 (28:4 Transmitter)
Pin Assignment for TSSOP



FIN3365 and FIN3363 (21:3 Transmitter)
Pin Assignment for TSSOP



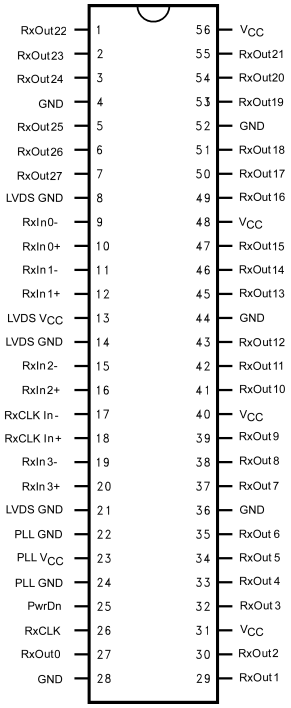
Receivers

Pin Descriptions

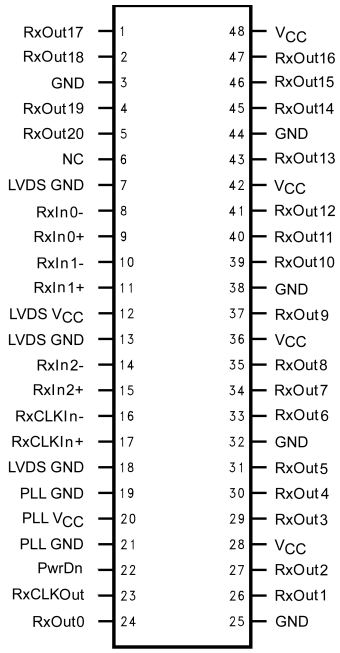
Pin Names	I/O Type	Number of Pins	Description of Signals
RxIn	I	4/3	Negative LVDS Differential Data Inputs
RxIn+	I	4/3	Positive LVDS Differential Data Inputs
RxCLKIn–	I	1	Negative LVDS Differential Clock Input
RxCLKIn+	I	1	Positive LVDS Differential Clock Input
RxOut	O	28/21	LVTTL Level Data Outputs Goes HIGH for PwrDn LOW
RxCLKOut	O	1	LVTTL Clock Output
$\overline{\text{PwrDn}}$	I	1	LVTTL Level Input Refer to Transmitter and Receiver Power-Up and Power-Down Operation Truth Table
PLL V_{CC}	I	1	Power Supply Pin for PLL
PLL GND	I	2	Ground Pins for PLL
LVDS V_{CC}	I	1	Power Supply Pin for LVDS Inputs
LVDS GND	I	3	Ground Pins for LVDS Inputs
V_{CC}	I	4	Power Supply for LVTTL Outputs
GND	I	5	Ground Pins for LVTTL Outputs
NC			No Connect

Connection Diagrams

FIN3386 and FIN3384 (4:28 Receiver)
Pin Assignment for TSSOP



FIN3366 and FIN3364 (3:21 Receiver)
Pin Assignment for TSSOP



Transmitter and Receiver Power-Up/Power-Down Operation Truth Table

The outputs of the transmitter remain in the High-Impedance state until the power supply reaches 2V. The following table shows the operation of the transmitter during power-up and power-down and operation of the PwrDn pin.

Transmitter			**PwrDn**	**Normal**			
	V_{CC}	<2V	>2V	>2V	>2V	>2V	>2V
	TxIn	X	X	Active	Active		
	TxOut±	Z	Z	Active	X		
	TxCLKIn	X	X	Active	H/L/Z		
	TxCLKOut±	Z	Z	Active	(Note 1)		
	PwrDn	L	L	H	H	H	H
Receiver			**PwrDn**				
	RxIn±	X	X	Active	Active	(Note 2)	(Note 2)
	RxOut	Z	L	L/H	P	H	P
	RxCLKIn±	X	X	Active	(Note 2)	Active	(Note 2)
	RxCLKOut	Z	(Note 3)	Active	(Note 3)	(Note 3)	(Note 3)
	PwrDn	L	L	H	H	H	H
	V_{CC}	<2V	>2V	>2V	>2V	>2V	>2V

H = HIGH Logic Level
L = LOW Logic Level
P = Last Valid State
X = Don't Care
Z = High-Impedance

Note 1: If the transmitter is powered up and PwrDn is inactive HIGH and the clock input goes to any state LOW, HIGH or Z then the internal PLL will go to a known low frequency and stay until the clock starts normal operation again.

Note 2: If the input is terminated and un-driven (Z) or shorted or open. (fail safe condition)

Note 3: For PwrDn or fail safe condition the RxCLKOut pin will go LOW for Panel Link devices and HIGH for Channel Link devices.

Note 4: Shorted here means (± inputs are shorted to each other, or ± inputs are shorted to each other and Ground or V_{CC}, or either ± inputs are shorted to Ground or V_{CC}) with no other Current/Voltage sources (noise) applied. If the V_{ID} is still in the valid range (greater than 100mV) and VCM is in the valid range (0V to 2.4V) then the input signal is still recognized and the part will respond normally.

Absolute Maximum Ratings(Note 5)

Power Supply Voltage (V_{CC})	-0.3V to +4.6V
TTL/CMOS Input/Output Voltage	–0.5V to +4.6V
LVDS Input/Output Voltage	-0.3V to +4.6V
LVDS Output Short Circuit Current (I_{OSD})	Continuous
Storage Temperature Range (T_{STG})	–65°C to +150°C
Maximum Junction Temperature (T_J)	150°C
Lead Temperature (T_L)	
(Soldering, 4 seconds)	260°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	
I/O to GND	>10.0 kV
All Pins	>6.5 kV
ESD Rating (MM, 0Ω, 200 pF)	>400V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Operating Temperature (T_A)(Note 5)	–10°C to +70°C
Maximum Supply Noise Voltage	
(V_{CCNPP})	100 mV_{P-P} (Note 6)

Note 5: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 6: 100mV V_{CC} noise should be tested for frequency at least up to 2 MHz. All the specification below should be met under such a noise.

Transmitter DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (Note 7)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Transmitter LVTTL Input Characteristics							
V_{IH}	Input High Voltage			2.0		V_{CC}	V
V_{IL}	Input Low Voltage			GND		0.8	V
V_{IK}	Input Clamp Voltage	I_{IK} = –18 mA			–0.79	–1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V to 4.6V			1.8	10.0	µA
		V_{IN} = GND		–10.0	0		
Transmitter LVDS Output Characteristics (Note 8)							
V_{OD}	Output Differential Voltage	R_L = 100 Ω, See Figure 1		250	TBD	450	mV
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW-to-HIGH					35.0	mV
V_{OS}	Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH						mV
I_{OS}	Short Circuit Output Current	V_{OUT} = 0V			–3.5	–5.0	mA
I_{OZ}	Disabled Output Leakage Current	DO = 0V to 4.6V, $\overline{PwrDn}$ = 0V			±1.0	±10.0	µA
Transmitter Supply Current							
I_{CCWT}	28:4 Transmitter Power Supply Current for Worst Case Pattern (With Load) (Note 9)	R_L = 100 Ω, See Figures 3, 4	32.5 MHz		31.0	49.5	mA
			40.0 MHz		32.0	55.0	
			66.0 MHz		37.0	60.5	
			85.0 MHz		42.0	66.0	
I_{CCWT}	21:3 Transmitter Power Supply Current for Worst Case Pattern (With Load) (Note 9)	R_L = 100 Ω, See Figures 3, 4	32.5 MHz		28.0	46.2	mA
			40.0 MHz		29.0	51.7	
			66.0 MHz		34.0	57.2	
			85.0 MHz		39.0	62.7	
I_{CCPDT}	Powered Down Supply Current	$\overline{PwrDn}$ = 0.8V			10.0	55.0	µA
I_{CCGT}	28:4 Transmitter Supply Current for 16 Grayscale (Note 9)	See Figure 22 (Note 10)	32.5 MHz		29.0	41.8	mA
			40.0 MHz		30.0	44.0	
			65.0 MHz		35.0	49.5	
			85.0 MHz		39.0	55.0	
I_{CCGT}	21:3 Transmitter Supply Current for 16 Grayscale (Note 9)	See Figure 22 (Note 10)	32.5 MHz		26.0	38.5	mA
			40.0 MHz		27.0	40.7	
			65.0 MHz		32.0	46.2	
			85.0 MHz		36.0	51.7	

Note 7: All Typical values are at T_A = 25°C and with V_{CC} = 3.3V.

Note 8: Positive current values refer to the current flowing into device and negative values means current flowing out of pins. Voltage are referenced to ground unless otherwise specified (except ΔV_{OD} and V_{OD}).

Note 9: The power supply current for both transmitter and receiver can be different with the number of active I/O channels.

Note 10: The 16-grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical strips across the display.

Transmitter AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period	See Figure 4	11.76	T	50.0	ns
t_{TCH}	Transmit Clock (TxCLKIn) HIGH Time		0.35	0.5	0.65	T
t_{TCL}	Transmit Clock Low Time		0.35	0.5	0.65	T
t_{CLKT}	TxCLKIn Transition Time (Rising and Failing)	(10% to 90%)	1.0		6.0	ns
t_{JIT}	TxCLKIn Cycle-to-Cycle Jitter	See Figure 12			3.0	ns
t_{XIT}	TxIn Transition Time		1.5		6.0	ns
LVDS Transmitter Timing Characteristics						
t_{TLH}	Differential Output Rise Time (20% to 80%)	See Figure 3		0.75	1.5	ns
t_{THL}	Differential Output Fall Time (80% to 20%)			0.75	1.5	ns
t_{STC}	TxIn Setup to TxCLNIn	See Figure 4 (f = 85 MHz)	2.5			ns
t_{HTC}	TxIn Holds to TCLKIn		0			ns
t_{TPDD}	Transmitter Power-Down Delay	See Figure 8, (Note 11)			100	ns
t_{TCCD}	Transmitter Clock Input to Clock Output Delay	See Figure 5			5.5	ns
	Transmitter Clock Input to Clock Output Delay	(T_A = 25°C and with V_{CC} = 3.3V)	2.8		6.8	
Transmitter Output Data Jitter (f = 40 MHz) (Note 12)						
t_{TPPB0}	Transmitter Output Pulse Position of Bit 0	See Figure 10 $a = \frac{1}{f \times 7}$	–0.25	0	0.25	ns
t_{TPPB1}	Transmitter Output Pulse Position of Bit 1		a–0.25	a	a+0.25	ns
t_{TPPB2}	Transmitter Output Pulse Position of Bit 2		2a–0.25	2a	2a+0.25	ns
t_{TPPB3}	Transmitter Output Pulse Position of Bit 3		3a–0.25	3a	3a+0.25	ns
t_{TPPB4}	Transmitter Output Pulse Position of Bit 4		4a–0.25	4a	4a+0.25	ns
t_{TPPB5}	Transmitter Output Pulse Position of Bit 5		5a–0.25	5a	5a+0.25	ns
t_{TPPB6}	Transmitter Output Pulse Position of Bit 6		6a–0.25	6a	6a+0.25	ns
Transmitter Output Data Jitter (f = 65 MHz) (Note 12)						
t_{TPPB0}	Transmitter Output Pulse Position of Bit 0	See Figure 10 $a = \frac{1}{f \times 7}$	–0.2	0	0.2	ns
t_{TPPB1}	Transmitter Output Pulse Position of Bit 1		a–0.2	a	a+0.2	ns
t_{TPPB2}	Transmitter Output Pulse Position of Bit 2		2a–0.2	2a	2a+0.2	ns
t_{TPPB3}	Transmitter Output Pulse Position of Bit 3		3a–0.2	3a	3a+0.2	ns
t_{TPPB4}	Transmitter Output Pulse Position of Bit 4		4a–0.2	4a	4a+0.2	ns
t_{TPPB5}	Transmitter Output Pulse Position of Bit 5		5a–0.2	5a	5a+0.2	ns
t_{TPPB6}	Transmitter Output Pulse Position of Bit 6		6a–0.2	6a	6a+0.2	ns
Transmitter Output Data Jitter (f = 85 MHz) (Note 12)						
t_{TPPB0}	Transmitter Output Pulse Position of Bit 0	See Figure 10 $a = \frac{1}{f \times 7}$	–0.2	0	0.2	ns
t_{TPPB1}	Transmitter Output Pulse Position of Bit 1		a–0.2	a	a+0.2	ns
t_{TPPB2}	Transmitter Output Pulse Position of Bit 2		2a–0.2	2a	2a+0.2	ns
t_{TPPB3}	Transmitter Output Pulse Position of Bit 3		3a–0.2	3a	3a+0.2	ns
t_{TPPB4}	Transmitter Output Pulse Position of Bit 4		4a–0.2	4a	4a+0.2	ns
t_{TPPB5}	Transmitter Output Pulse Position of Bit 5		5a–0.2	5a	5a+0.2	ns
t_{TPPB6}	Transmitter Output Pulse Position of Bit 6		6a–0.2	6a	6a+0.2	ns
t_{JCC}	FIN3385/3365 Transmitter Clock Out Jitter	f = 40 MHz		350	370	ps
	(Cycle-to-Cycle)	f = 65 MHz		210	230	
	See Figure 12	f = 85 MHz		110	150	
t_{TPLLS}	Transmitter Phase Lock Loop Set Time (Note 13)	See Figure 6, (Note 12)			10.0	ms

Note 11: Outputs of all transmitters stay in 3-STATE until power reaches 2V. Both clock and data output begins to toggle 10ms after V_{CC} reaches 3V and Power-Down pin is above 1.5V.

Note 12: This output data pulse position works for both transmitter with 28 or 21 TTL inputs except the LVDS output bit mapping difference (see Figures 15, 16). Figure 17 shows the skew between the first data bit and clock output. Also 2-bit cycle delay is guaranteed when the MSB is output from transmitter.

Note 13: This jitter specification is based on the assumption that PLL has a ref clock with cycle-to-cycle input jitter less than 2ns.

Receiver DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (Note 14)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
LVTTL/CMOS DC Characteristics							
V_{IH}	Input High Voltage			2.0		V_{CC}	V
V_{IL}	Input Low Voltage			GND		0.8	V
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA		2.7	3.3		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA			0.06	0.3	V
V_{IK}	Input Clamp Voltage	I_{IK} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0V to 4.6V		−10.0		10.0	µA
I_{OFF}	Input/Output Power Off Leakage Current	V_{CC} = 0V, All LVTTL Inputs/Outputs 0V to 4.6V				±10.0	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			−60.0	−120	mA
Receiver LVDS Input Characteristics							
V_{TH}	Differential Input Threshold HIGH	Figure 2, Table 2				100	mV
V_{TL}	Differential Input Threshold LOW	Figure 2, Table 2		−100			mV
V_{ICM}	Input Common Mode Range	Figure 2, Table 2		0.05		2.35	V
I_{IN}	Input Current	V_{IN} = 2.4V, V_{CC} = 3.6V or 0V				±10.0	µA
		V_{IN} = 0V, V_{CC} = 3.6V or 0V				±10.0	µA
Receiver Supply Current							
I_{CCWR}	4:28 Receiver Power Supply Current for Worst Case Pattern (With Load) (Note 15)	C_L = 8 pF, See Figures 2, 3	32.5 MHz			70.0	mA
			40.0 MHz			75.0	
			66.0 MHz			114	
			85.0 MHz			135	
I_{CCWR}	3:21 Receiver Power Supply Current for Worst Case Pattern (With Load) (Note 15)	C_L = 8 pF, See Figures 2, 3	32.5 MHz		49.0	60.0	mA
			40.0 MHz		53.0	65.0	
			66.0 MHz		78.0	100	
			85.0 MHz		90.0	115	
I_{CCPDR}	Powered Down Supply Current	$\overline{PwrDn}$ = 0.8V (RxOut stays LOW)			NA	55.0	µA
t_{RCOP}	Receiver Clock Output (RxCLKOut) Period	See Figure 9 (f = 85 MHz) (Rising Edge Strobe)		11.76	T	50.0	
t_{RCOL}	RxCLKOut LOW Time			4.0	5.0	6.0	ns
t_{RCOH}	RxCLKOut HIGH Time			4.5	5.0	6.5	ns
t_{RSRC}	RxOut Valid Prior to RxCLKOut			3.5			ns
t_{RHRC}	RxOut Valid After RxCLKOut			3.5			ns
t_{ROLH}	Output Rise Time (20% to 80%)	C_L = 8 pF, See Figure 5			2.0	3.5	ns
t_{ROHL}	Output Fall Time (80% to 20%)				1.8	3.5	ns
t_{RCCD}	Receiver Clock Input to Clock Output Delay	See Figure 11, (Note 16) T_A = 25°C and V_{CC} = 3.3V		3.5	5.0	7.5	ns
t_{RPDD}	Receiver Power-Down Delay	See Figure 14				1.0	µs
t_{RSPB0}	Receiver Input Strobe Position of Bit 0	See Figure 8 (f = 85 MHz)		0.49	0.84	1.19	ns
t_{RSPB1}	Receiver Input Strobe Position of Bit 1			2.17	2.52	2.87	ns
t_{RSPB2}	Receiver Input Strobe Position of Bit 2			3.85	4.20	4.55	ns
t_{RSPB3}	Receiver Input Strobe Position of Bit 3			5.53	5.88	6.23	ns
t_{RSPB4}	Receiver Input Strobe Position of Bit 4			7.21	7.56	7.91	ns
t_{RSPB5}	Receiver Input Strobe Position of Bit 5			8.89	9.24	9.59	ns
t_{RSPB6}	Receiver Input Strobe Position of Bit 6			10.57	10.92	11.27	ns
t_{RSKM}	RxIN Skew Margin	See Figure 9, (Note 17)		290			ps
t_{RPLLS}	Receiver Phase Lock Loop Set Time	See Figure 12				10.0	ms

Note 14: All Typical Values are at T_A = 25°C and with V_{CC} = 3.3V. Positive current values refer to the current flowing into device and negative values means current flowing out of pins. Voltage are referenced to ground unless otherwise specified (except ΔV_{OD} and V_{OD}).

Note 15: The power supply current for the receiver can be different with the number of active I/O channels.

Note 16: Total channel latency from Sewrializer to deserializer is (T + t_{TCCD}) + (2*T + t_{RCCD}). T here is the clock period.

Note 17: Receiver skew margin is defined as the valid sampling window after considering potential setup/hold time and minimum/maximum bit position.

Receiver AC Electrical Characteristics (66 MHz)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{RCOP}	Receiver Clock Output (RxCLKOut) Period	See Figure 9	15.0	T	50.0	ns
t_{RCOL}	RxCLKOut LOW Time		10.0	11.0		ns
t_{RCOH}	RxCLKOut HIGH Time	See Figure 9	10.0	12.2		ns
t_{RSRC}	RxOut Valid Prior to RxCLKOut	(Rising Edge Strobe)	6.5	11.6		ns
t_{RHRC}	RxOut Valid After RxCLKOut	(f = 40 MHz)	6.0	11.6		ns
t_{RCOL}	RxCLKOut LOW Time		5.0	6.3	9.0	ns
t_{RCOH}	RxCLKOut HIGH Time	See Figure 9, (Note 18)	5.0	7.6	9.0	ns
t_{RSRC}	RxOut Valid Prior to RxCLKOut	(Rising Edge Strobe)	4.5	7.3		ns
t_{RHRC}	RxOut Valid After RxCLKOut	(f = 66 MHz)	4.0	6.3		ns
t_{ROLH}	Output Rise Time (20% to 80%)	C_L = 8 pF, (Note 17)		2.0	5.0	ns
t_{ROHL}	Output Fall Time (80% to 20%)	See Figure 5		1.8	5.0	ns
t_{RCCD}	Receiver Clock Input to Clock Output Delay	See Figure 11, (Note 19) T_A = 25°C and V_{CC} = 3.3V	3.5	5.0	7.5	ns
t_{RPDD}	Receiver Power-Down Delay	See Figure 14			1.0	µs
t_{RSPB0}	Receiver Input Strobe Position of Bit 0		1.0	1.4	2.15	ns
t_{RSPB1}	Receiver Input Strobe Position of Bit 1		4.5	5.0	5.8	ns
t_{RSPB2}	Receiver Input Strobe Position of Bit 2	See Figure 17	8.1	8.5	9.15	ns
t_{RSPB3}	Receiver Input Strobe Position of Bit 3	(f = 40 MHz)	11.6	11.9	12.6	ns
t_{RSPB4}	Receiver Input Strobe Position of Bit 4		15.1	15.6	16.3	ns
t_{RSPB5}	Receiver Input Strobe Position of Bit 5		18.8	19.2	19.9	ns
t_{RSPB6}	Receiver Input Strobe Position of Bit 6		22.5	22.9	23.6	ns
t_{RSPB0}	Receiver Input Strobe Position of Bit 0		0.7	1.1	1.4	ns
t_{RSPB1}	Receiver Input Strobe Position of Bit 1		2.9	3.3	3.6	ns
t_{RSPB2}	Receiver Input Strobe Position of Bit 2	See Figure 17	5.1	5.5	5.8	ns
t_{RSPB3}	Receiver Input Strobe Position of Bit 3	(f = 65 MHz)	7.3	7.7	8.0	ns
t_{RSPB4}	Receiver Input Strobe Position of Bit 4		9.5	9.9	10.2	ns
t_{RSPB5}	Receiver Input Strobe Position of Bit 5		11.7	12.1	12.4	ns
t_{RSPB6}	Receiver Input Strobe Position of Bit 6		13.9	14.3	14.6	ns
t_{RSKM}	RxIn Skew Margin	f = 40 MHz	490			ps
	See Figure 19, (Note 20)	f = 66 MHz	400			
t_{RPLLS}	Receiver Phase Lock Loop Set Time	See Figure 17			10.0	ms

Note 18: For the receiver with falling-edge strobe, the definition of setup/hold time will be slightly different from the one with rising-edge strobe. The clock reference point is the time when the clock falling edge passes through 2V. For hold time t_{RHRC}, the clock reference point is the time when falling edge passes through +0.8V.

Note 19: Total channel latency from Sewrializer to deserializer is $(T + t_{TCCD}) + (2*T + t_{RCCD})$. There is the clock period.

Note 20: Receiver skew margin is defined as the valid sampling window after considering potential setup/hold time and minimum/maximum bit position.

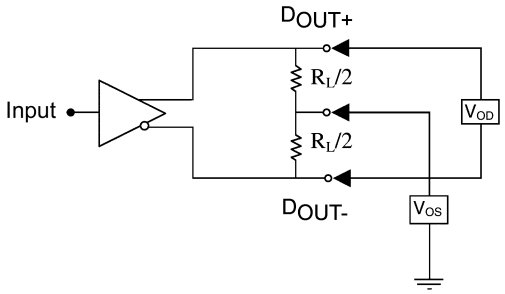
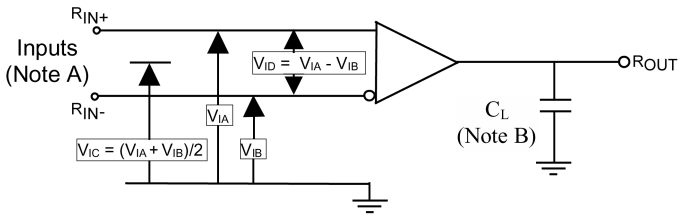


FIGURE 1. Differential LVDS Output DC Test Circuit

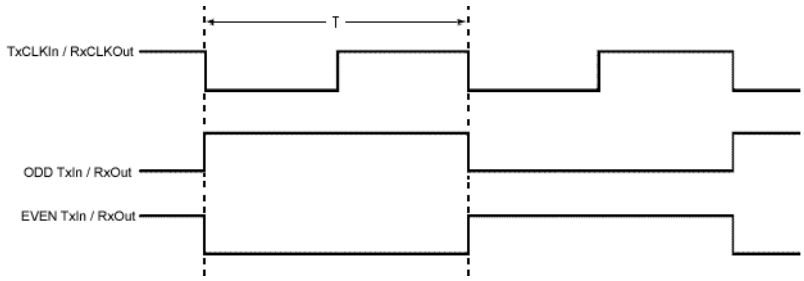


Note A: For all input pulses, t_R or t_F < = 1 ns.
Note B: C_L includes all probe and jig capacitance.

FIGURE 2. Differential Receiver Voltage Definitions and Propagation Delay and Transition Time Test Circuit

TABLE 2. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common Mode Input Voltage (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	–100	1.2
2.4	2.3	100	2.35
2.3	2.4	–100	2.35
0.1	0	100	0.05
0	0.1	–100	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3



Note: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVTTL/CMOS I/O. Depending on the valid strobe edge of transmitter, the TxCLKIn can be either rising or falling edge data strobe.

FIGURE 3. "Worst Case" Test Pattern

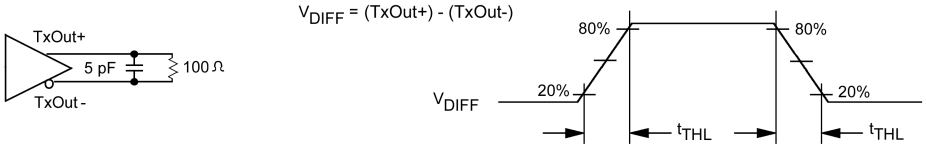


FIGURE 4. Transmitter LVDS Output Load and Transition Times

FIGURE 5. Receiver LVTTL/CMOS Output Load and Transition Times

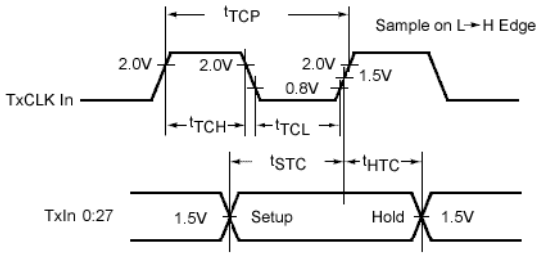


FIGURE 6. Transmitter Setup/Hold and HIGH/LOW Times (Rising Edge Strobe)

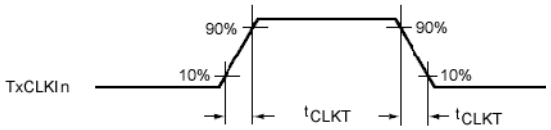


FIGURE 7. Transmitter Input Clock Transition Time

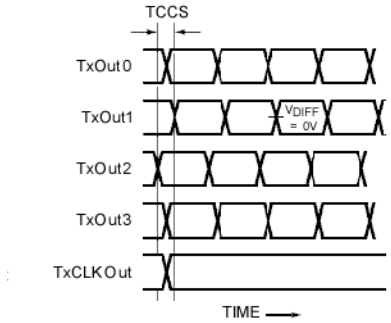
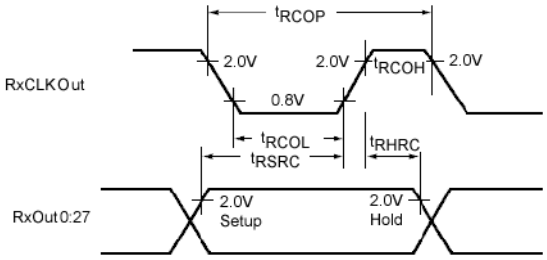


FIGURE 8. Transmitter Outputs Channel-to-Channel Skew



Note: For the receiver with falling-edge strobe, the definition of setup/hold time will be slightly different from the one with rising-edge strobe. The clock reference point is the time when the clock falling edge passes through 2V. For hold time t_{RHRC}, the clock reference point is the time when falling edge passes through +0.8V.

FIGURE 9. (Receiver) Setup/Hold and HIGH/LOW Times

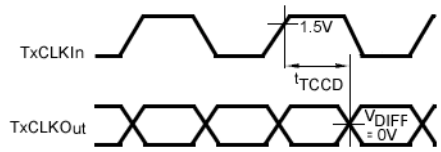


FIGURE 10. Transmitter Clock In to Clock Out Delay (Rising Edge Strobe)

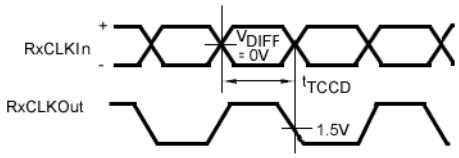


FIGURE 11. Receiver Clock In to Clock Out Delay (Falling Edge Strobe)

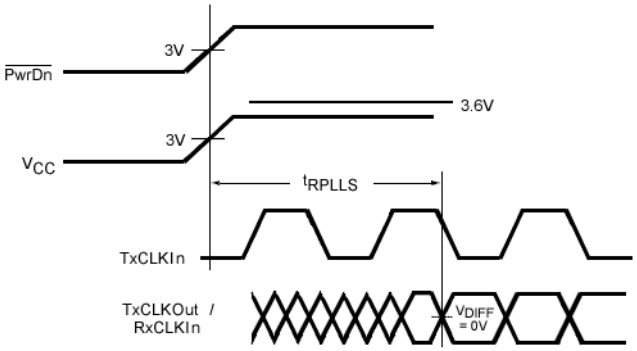


FIGURE 12. Receiver Phase Lock Loop Set Time

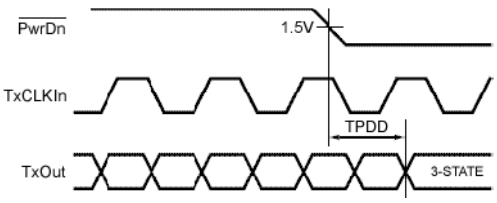


FIGURE 13. Transmitter Power-Down Delay

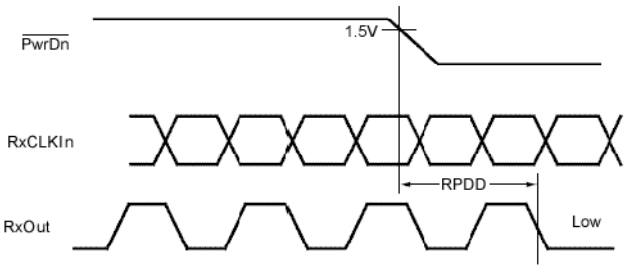
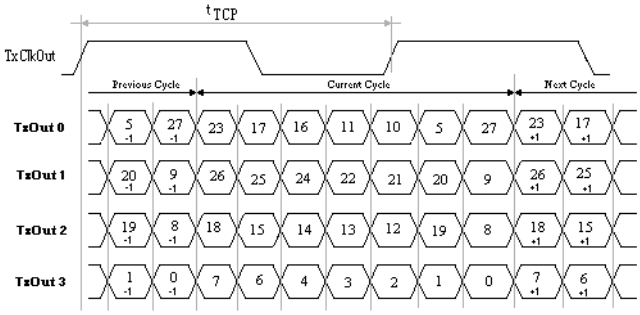
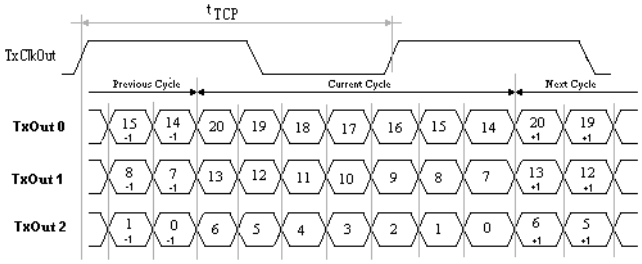


FIGURE 14. Receiver Power-Down Delay



Note: This output data pulse position works for both transmitter with 28 or 21 TTL inputs except the LVDS output bit mapping difference. All the information in this diagram tells that the skew between the first data bit and clock output. Also 2-bit cycle delay is guaranteed when the MSB is output from transmitter.

FIGURE 15. 28 Parallel LVTTL Inputs Mapped to 4 Serial LVDS Outputs



Note: This output data pulse position works for both transmitter with 28 or 21 TTL inputs except the LVDS output bit mapping difference. All the information in this diagram tells that the skew between the first data bit and clock output. Also 2-bit cycle delay is guaranteed when the MSB is output from transmitter.

FIGURE 16. 21 Parallel LVTTL Inputs Mapped to 3 Serial LVDS Outputs

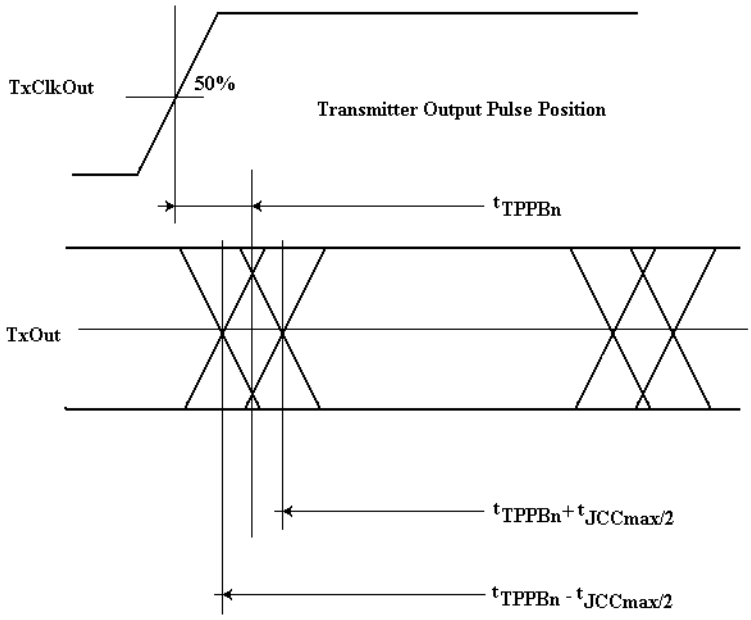


FIGURE 17.

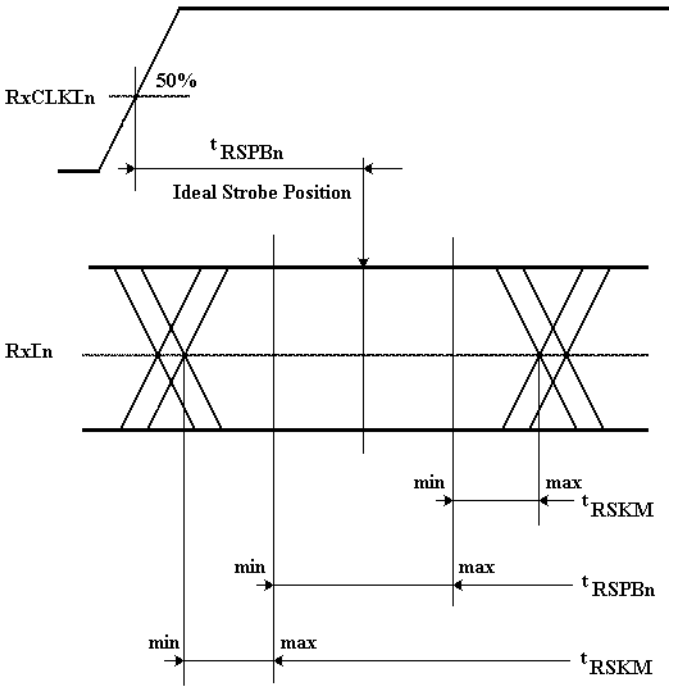
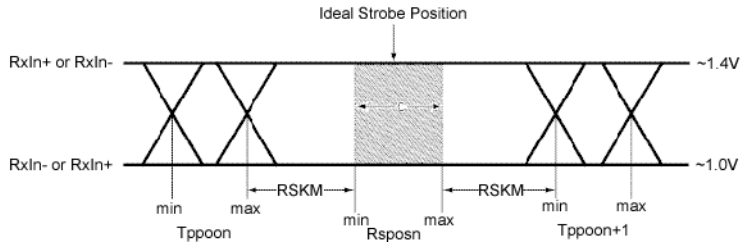


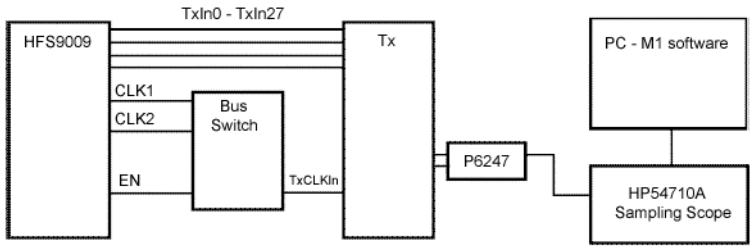
FIGURE 18.



Note: t_{RSKM} is the budget for the cable skew and source clock skew plus ISI (Inter-Symbol Interference).

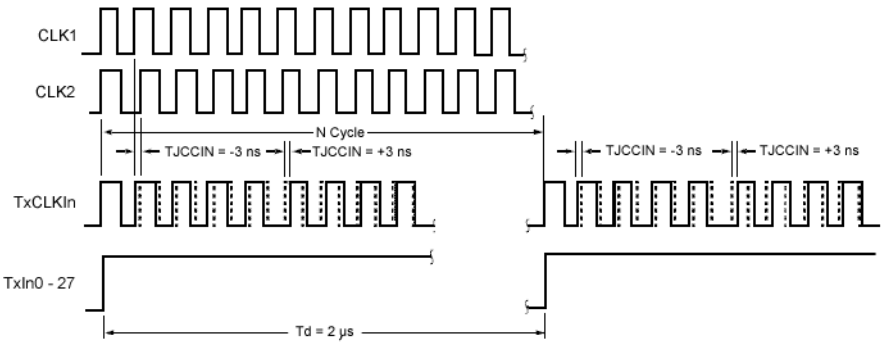
Note: The minimum and maximum pulse position values are based on the bit position of each of the 7 bits within the LVDS data stream across PVT (Process, Voltage Supply, and Temperature).

FIGURE 19. Receiver LVDS Input Skew Margin



Note: Test setup used considers no requirement for separation of RMS and deterministic jitter. Other hardware setup such as Wavecrest boxes can be used if no M1 software is available, but the test methodology in Figure 21 should be followed.

FIGURE 20. Transmitter Clock Out Jitter Measurement Setup

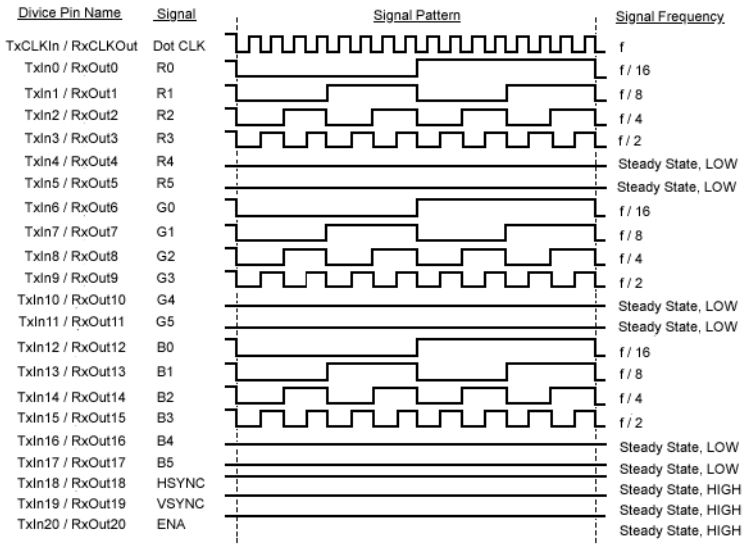


32.5 MHz - N Cycle = 66
40 MHz - N Cycle = 80
65 MHz - N Cycle = 132
85 MHz - N Cycle = 170

Note: This jitter pattern is used to test the jitter response (Clock Out) of the device over the power supply range with worst jitter ±3ns (cycle-to-cycle) clock input. The specific test methodology is as follows:

- Switching input data TxIn0 to TxIn20 at 0.5 MHz, and the input clock is shifted to left –3ns and to the right +3ns when data is HIGH (by switching between CLK1 and CLK2 in Figure 20).
- The ±3 ns cycle-to-cycle input jitter is the static phase error between the two clock sources. Jumping between two clock sources to simulate the worst case of clock edge jump (3 ns) from graphical controllers. Cycle-to-cycle jitter at TxCLK out pin should be measured cross V_{CC} range with 100mV noise (V_{CC} noise frequency <2 MHz).

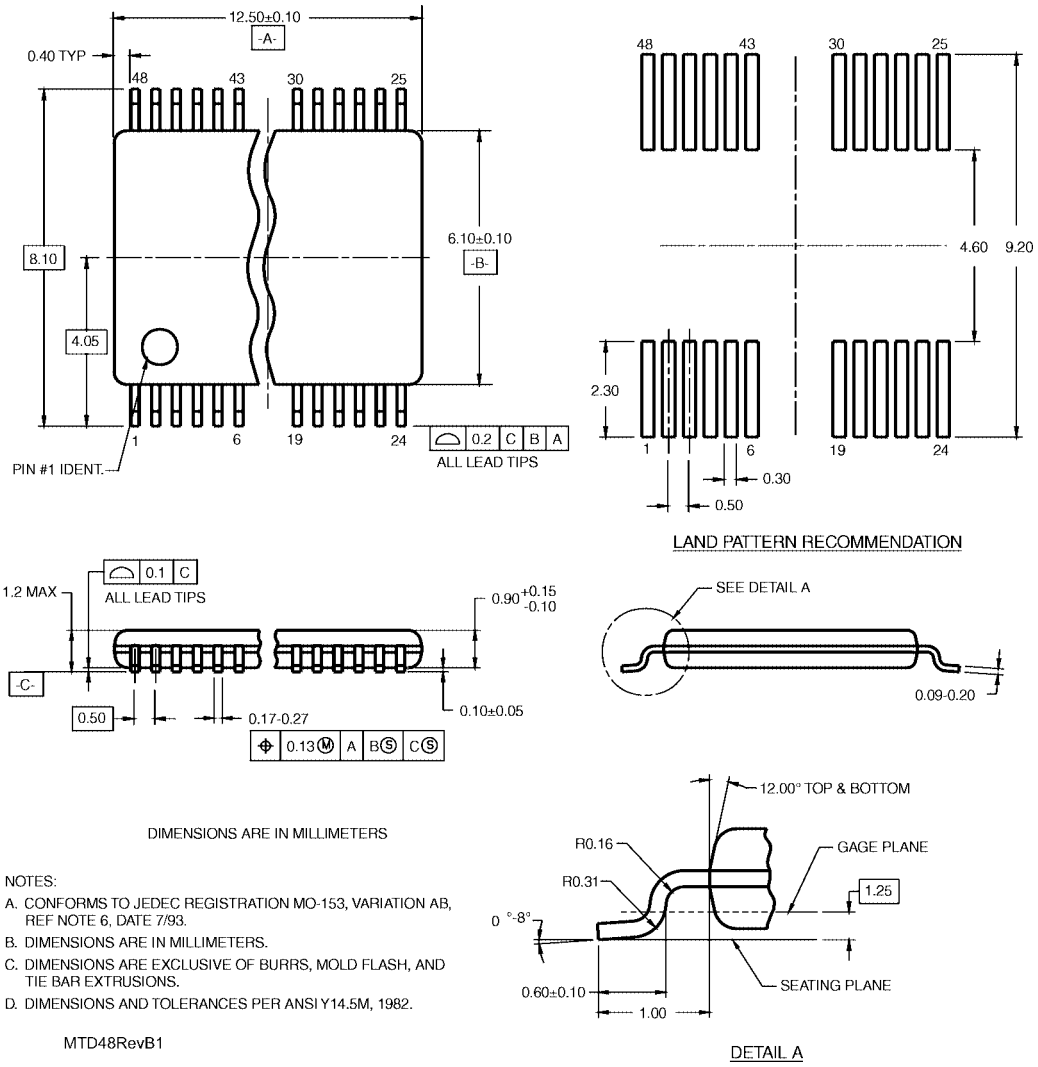
FIGURE 21. Timing Diagram of Transmitter Clock Input with Jitter



Note: The 16-grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical strips across the display.

FIGURE 22. “16 Grayscale” Test Pattern

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

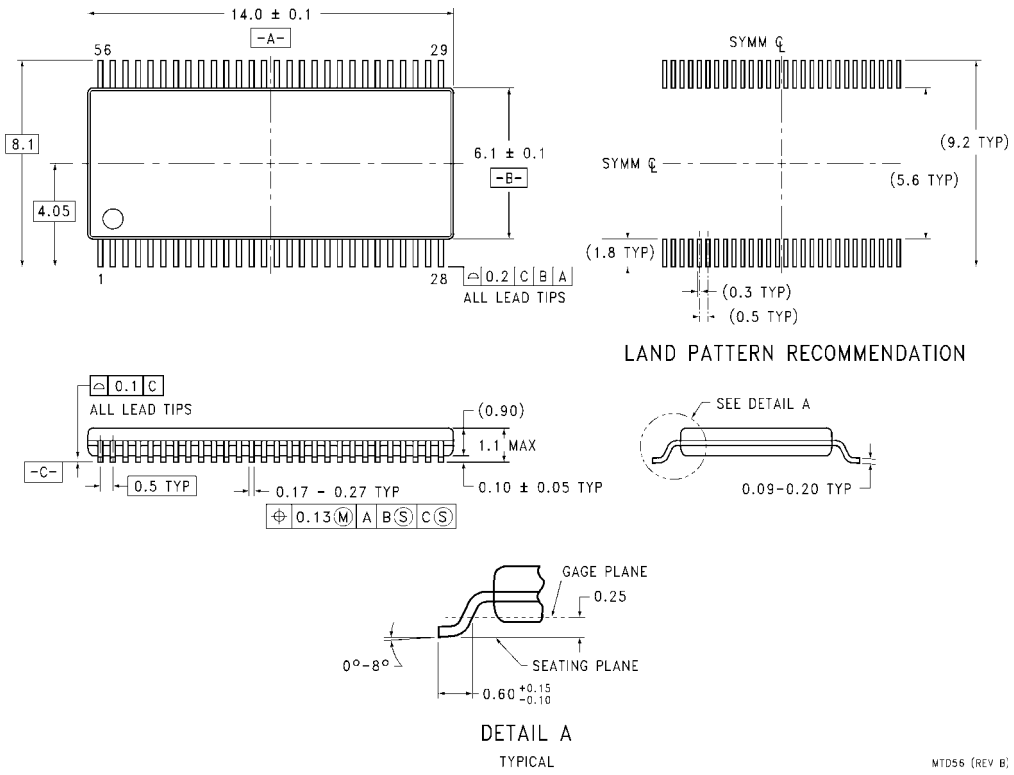
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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