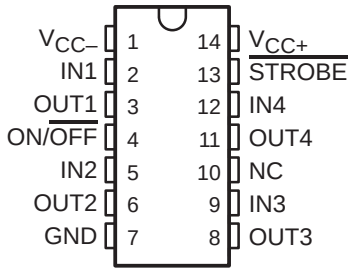
SLLS048F – APRIL 1989 – REVISED APRIL 1998

- **Low Supply Voltage . . . ±5 V to ±15 V**
- **Supply Current . . . 500 μA Typical**
- **Zero Supply Current When Shut Down**
- **Outputs Can Be Driven ±30 V**
- **Output Open When Off (3-State)**
- **10-mA Output Drive**
- **Outputs of Several Devices Can Be Connected in Parallel**
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-F Specifications**
- **Designed to Be Interchangeable With Linear Technology LT1030**

D OR N PACKAGE
(TOP VIEW)



NC – No internal connection

description

The LT1030C is an EIA/TIA-232-F line driver that operates over a ±5-V to ±15-V supply-voltage range on low supply current. The device can be shut down to zero supply current. Current limiting fully protects the outputs from externally applied voltages of ±30 V. Since the output swings to within 200 mV of the positive supply and to within 1 V of the negative supply, supply-voltage requirements are minimized.

A major advantage of the LT1030C is the high-impedance output state when the device is off or powered down. This feature allows several different drivers on the same bus.

The device can be used as an EIA/TIA-232-F driver, micropower interface, or level translator, among others.

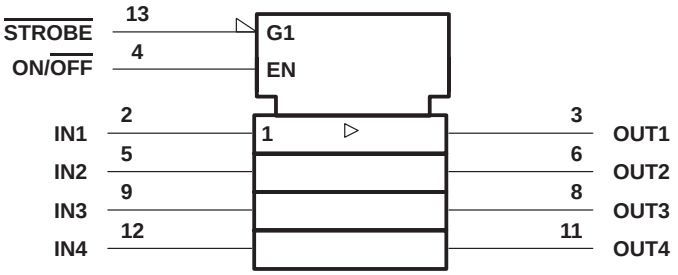
The LT1030C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

PACKAGE	
SMALL OUTLINE (D)	**PLASTIC DIP (N)**
LT1030CD	LT1030CN

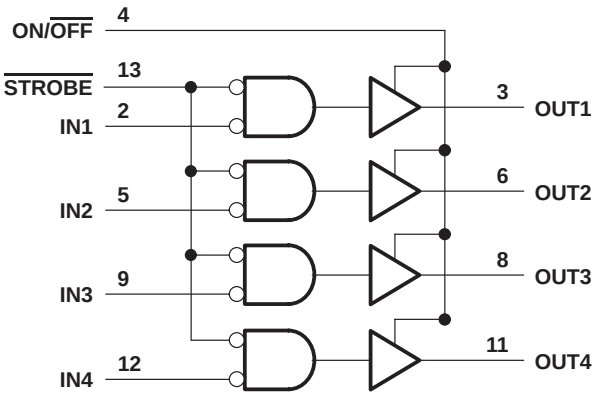
The D package is available taped and reeled. Add the suffix R to the device type (i.e., LT1030CDR).

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
GND	7	Ground terminal
IN1 IN2 IN3 IN4	2 5 9 12	Logic inputs. INx operate properly on TTL or CMOS levels. Output valid from $V_I = V_{CC-} + 2$ V to 15 V. Connect to 5 V when not used.
ON/$\overline{\text{OFF}}$	4	ON/$\overline{\text{OFF}}$ shuts down the entire circuit. It cannot be left open. For normally on operation, connect between 5 V and 10 V. If V_{IL} is at or near 0.8 V, significant settling time may be required.
OUT1 OUT2 OUT3 OUT4	3 6 8 11	Line driver outputs
$\overline{\text{STROBE}}$	13	$\overline{\text{STROBE}}$ forces all outputs low. Drive with 3 V. Strobe terminal input impedance is approximately 2 kΩ to GND. Leave $\overline{\text{STROBE}}$ open when not used.
V_{CC+}	14	Positive supply
V_{CC-}	1	Negative supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC+} (see Note 1) . . . . . 0 V to 15 V
Supply voltage range, V_{CC-} . . . . . 0 V to –15 V
Input voltage range, logic inputs, V_I . . . . . V_{CC-} to 25 V
Input voltage range at ON/$\overline{OFF}$, V_I . . . . . 0 V to 12 V
Output voltage range, V_O (any output) . . . . . V_{CC+} – 30 V to V_{CC-} + 30 V
Duration of output short circuit to ±30 V at (or below) 25°C (see Note 2) . . . . . Unlimited
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 127°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to GND.
2. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	5	15	V
Supply voltage, V_{CC-}	–5	–15	V
High-level input voltage, V_{IH} (see Note 4)	2	15	V
Low-level input voltage, V_{IL} (see Note 4)		0.8	V
Operating free-air temperature, T_A	0	70	°C

NOTE 4: These V_{IH} and V_{IL} specifications apply only for inputs IN1–IN4. For operating levels for ON/$\overline{OFF}$, see Figure 2.

electrical characteristics over operating free-air temperature range, $V_{CC\pm}$ = ±5 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OM+}	Maximum positive peak output voltage swing	I_O = –2 mA, T_A = 25°C	V_{CC+}–0.3	V_{CC+}–0.1		V
V_{OM-}	Maximum negative peak output voltage swing	I_O = 2 mA, T_A = 25°C		V_{CC-}+0.9	V_{CC-}+1.4	V
I_{IH}	High-level input current	$V_I \geq$ 2 V, T_A = 25°C		2	20	µA
I_{IL}	Low-level input current	$V_I \leq$ 0.8 V, T_A = 25°C		–10	–20	µA
I_I	Input current, ON/$\overline{OFF}$	V_I = 0		–0.1	–10	µA
		V_I = 5 V		30	65	
I_O	Output current	T_A = 25°C	5	12		mA
I_{OZ}	Off-state output current	V_O = ±15 V, T_A = 25°C, ON/$\overline{OFF}$ at 0.4 V		±2	±100	µA
I_{CC}	Supply current (all outputs low)	$V_I \geq$ at 2.4 V, I_O = 0		500	1000	µA
$I_{CC(off)}$	Off-state supply current	ON/$\overline{OFF}$ at 0.4 V			10	µA
		ON/$\overline{OFF}$ at 0.1 V		10	150	

‡ All typical values are at $V_{CC\pm}$ = ±12 V, T_A = 25°C.

operating characteristics, $V_{CC\pm}$ = ±5 V to ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ, C_L = 51 pF	4	15	30	V/μs

† All typical values are at $V_{CC\pm}$ = ±12 V, T_A = 25°C.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

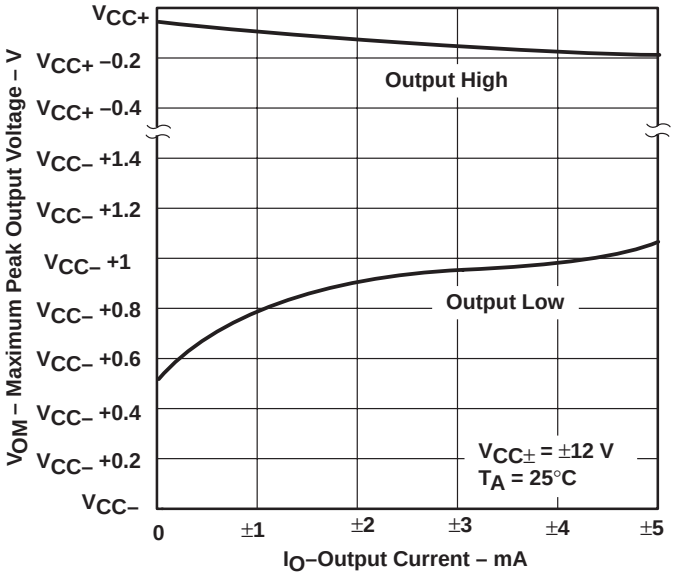


Figure 1

ON/$\overline{\text{OFF}}$ TERMINAL VOLTAGE vs FREE-AIR TEMPERATURE

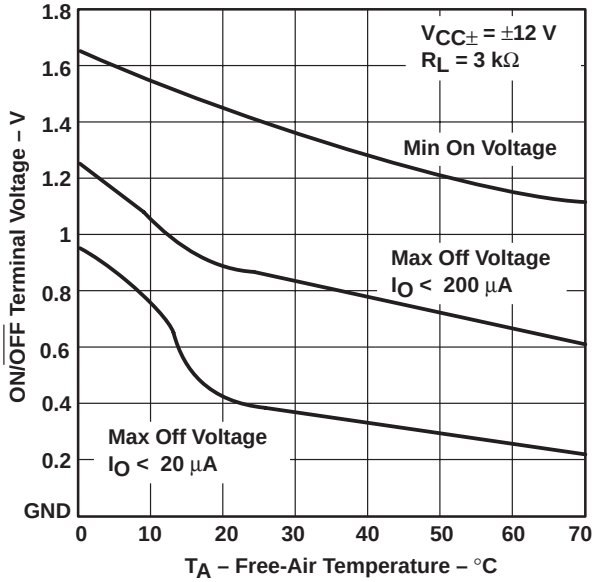


Figure 2

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

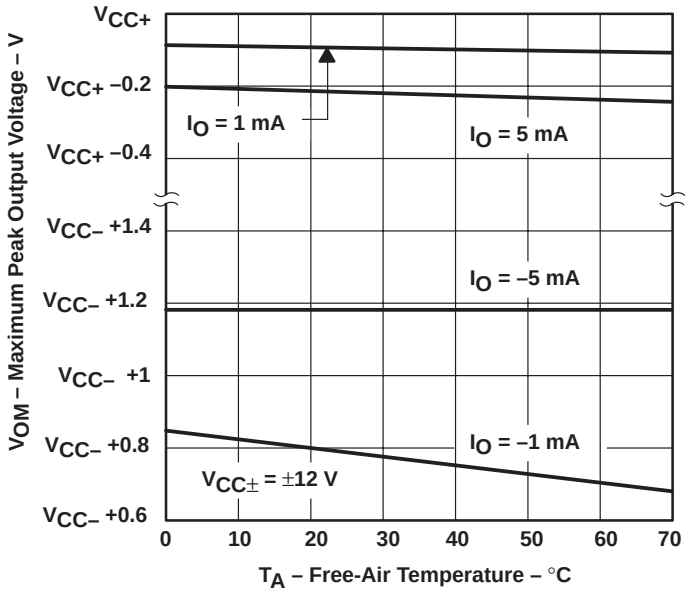


Figure 3

ON/$\overline{\text{OFF}}$ TERMINAL CURRENT vs ON/$\overline{\text{OFF}}$ TERMINAL VOLTAGE

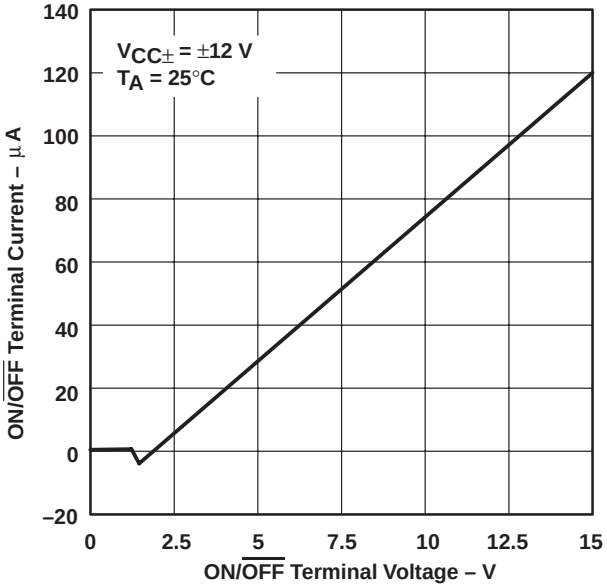


Figure 4

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs FREE-AIR TEMPERATURE

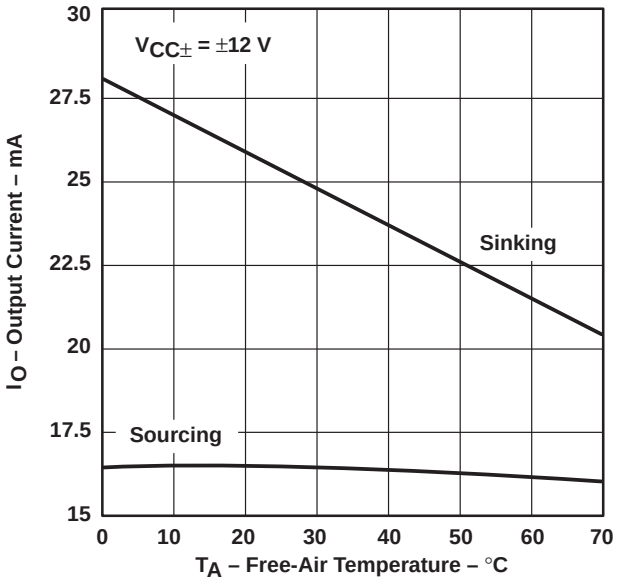


Figure 5

OFF-STATE OUTPUT CURRENT vs FREE-AIR TEMPERATURE

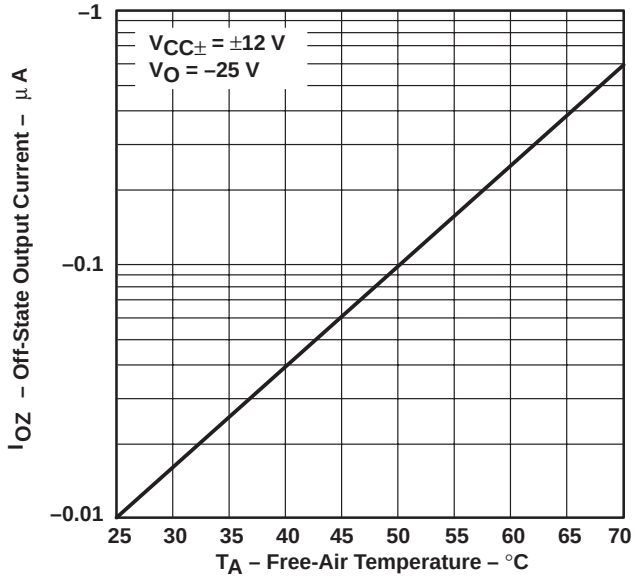


Figure 6

TYPICAL CHARACTERISTICS

OFF-STATE SUPPLY CURRENT vs FREE-AIR TEMPERATURE

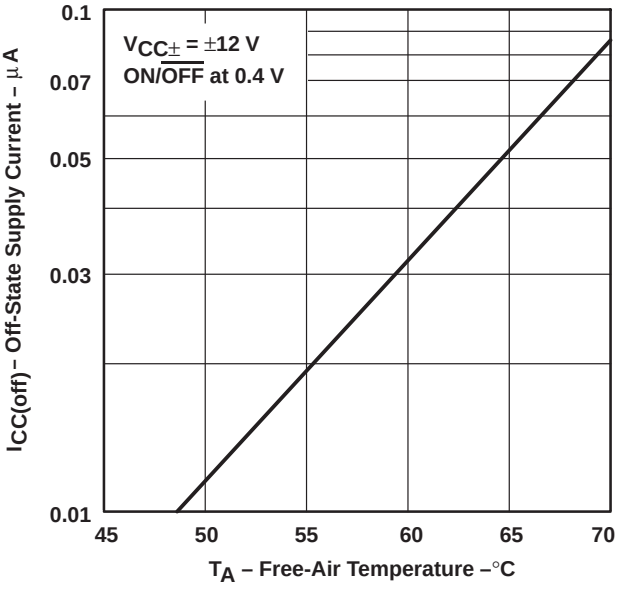


Figure 7

SUPPLY CURRENT vs TOTAL SUPPLY VOLTAGE

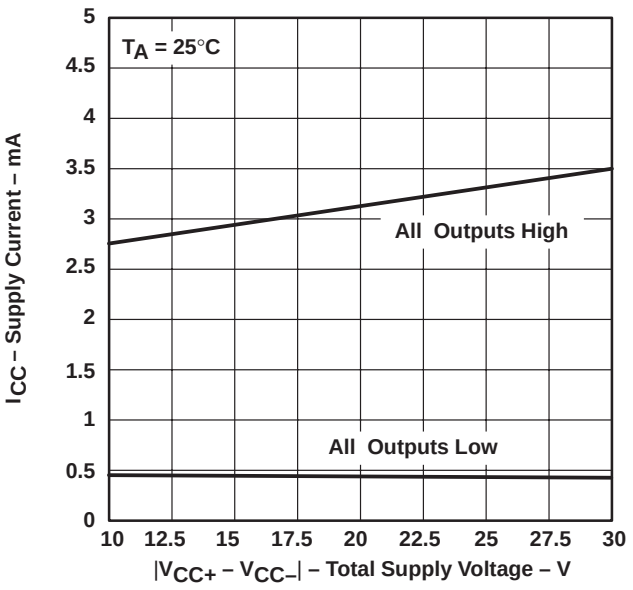


Figure 8

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

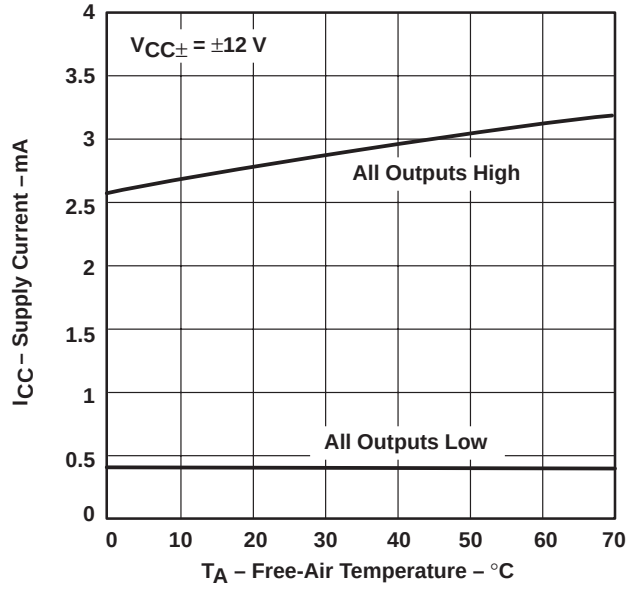


Figure 9

SLEW RATE vs FREE-AIR TEMPERATURE

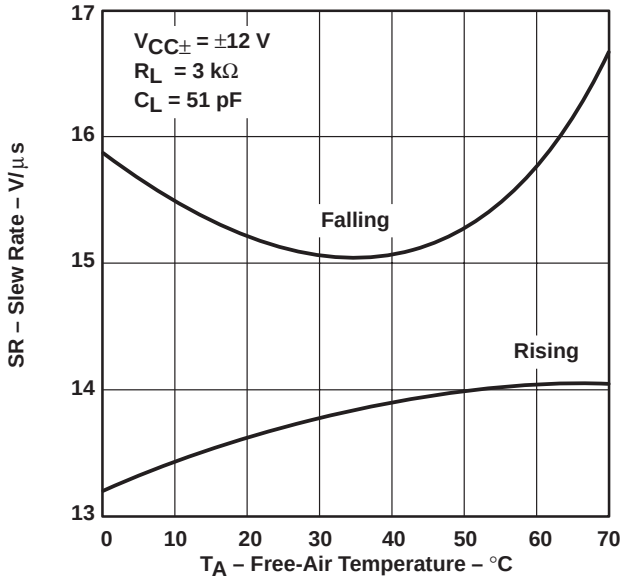


Figure 10

APPLICATION INFORMATION

forward biasing the substrate

As with other bipolar integrated circuits, forward biasing the substrate diode can cause problems. The LT1030C draws high current from V_{CC+} to GND when V_{CC-} is open circuited or pulled above ground. Connecting a diode from V_{CC-} to GND (if possible) prevents the high-current state. Any low-cost diode can be used (see Figure 11).

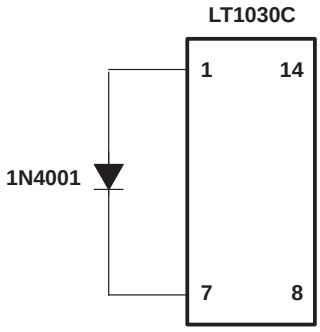


Figure 11. Connecting a Diode From V_{CC-} to GND

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LT1030CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	LT1030C	Samples
LT1030CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	LT1030C	Samples
LT1030CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	LT1030C	Samples
LT1030CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1030CN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

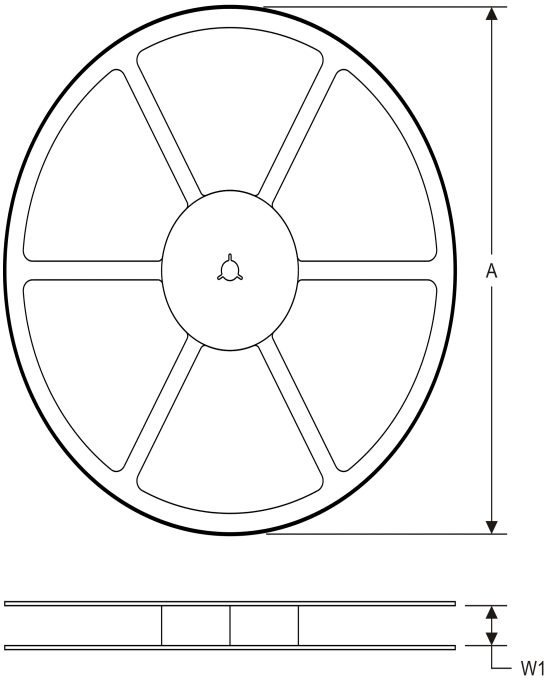
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

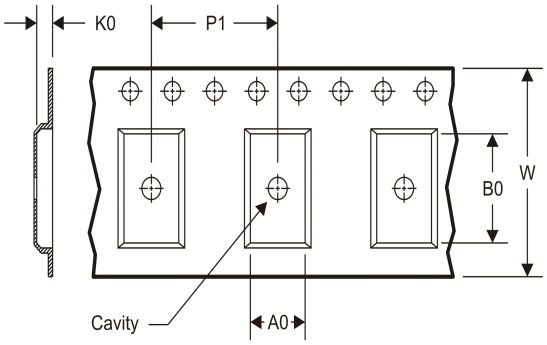
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



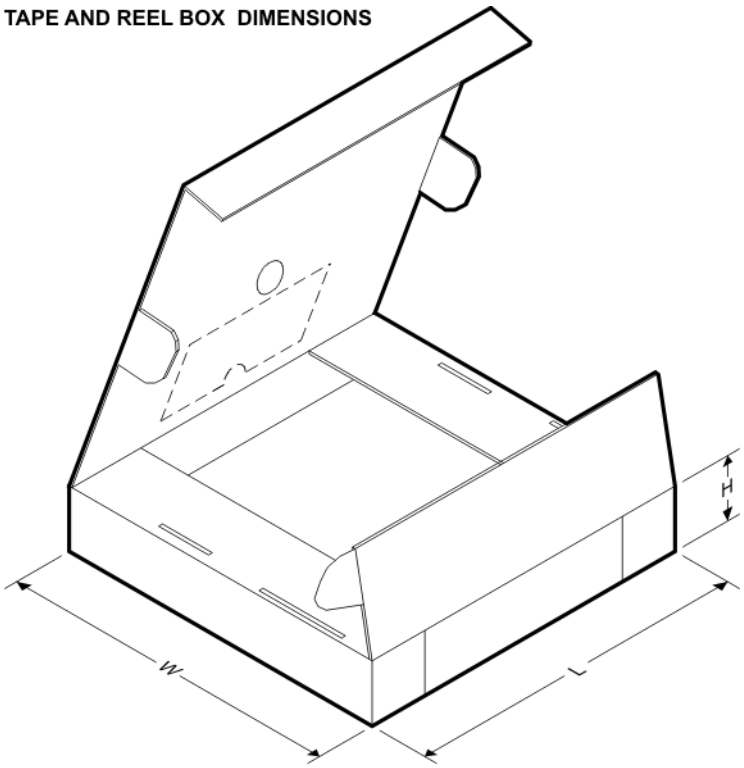
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1030CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



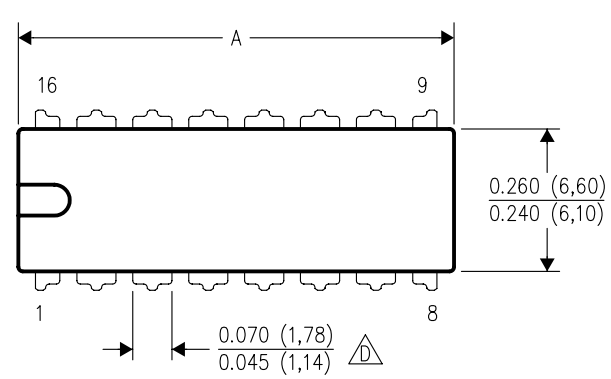
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1030CDR	SOIC	D	14	2500	367.0	367.0	38.0

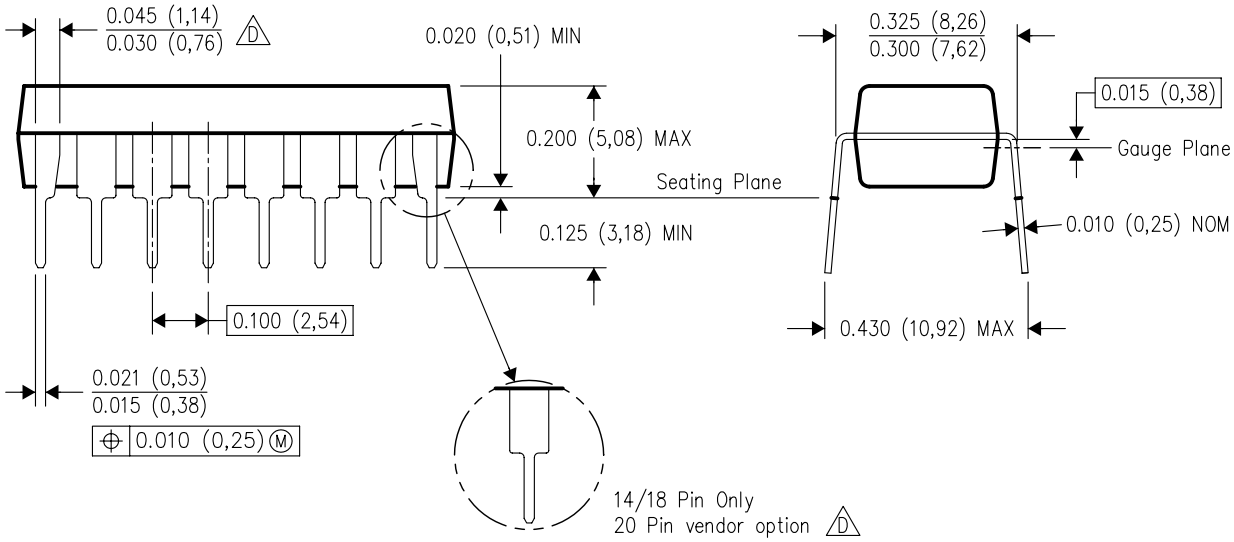
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



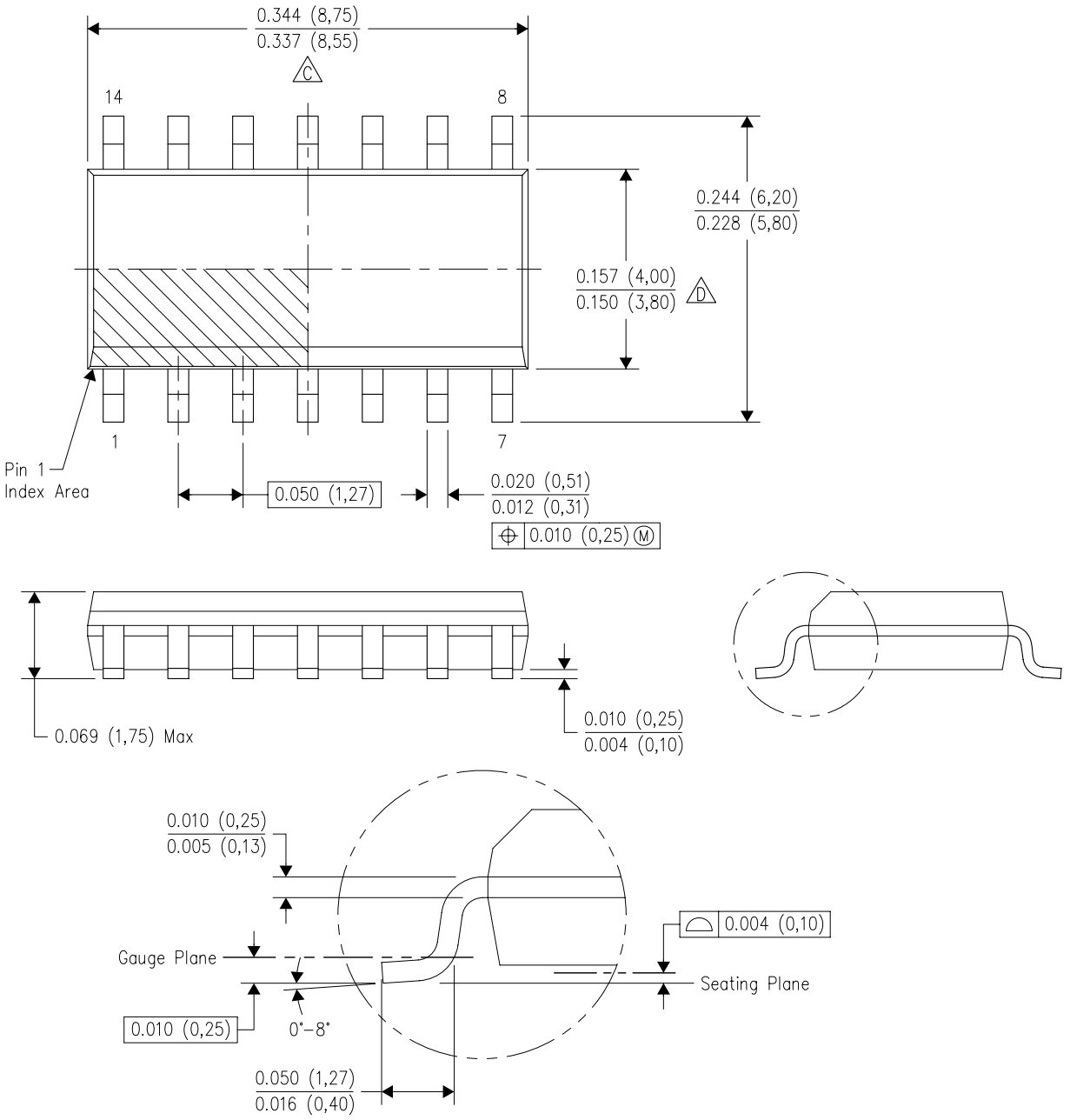
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

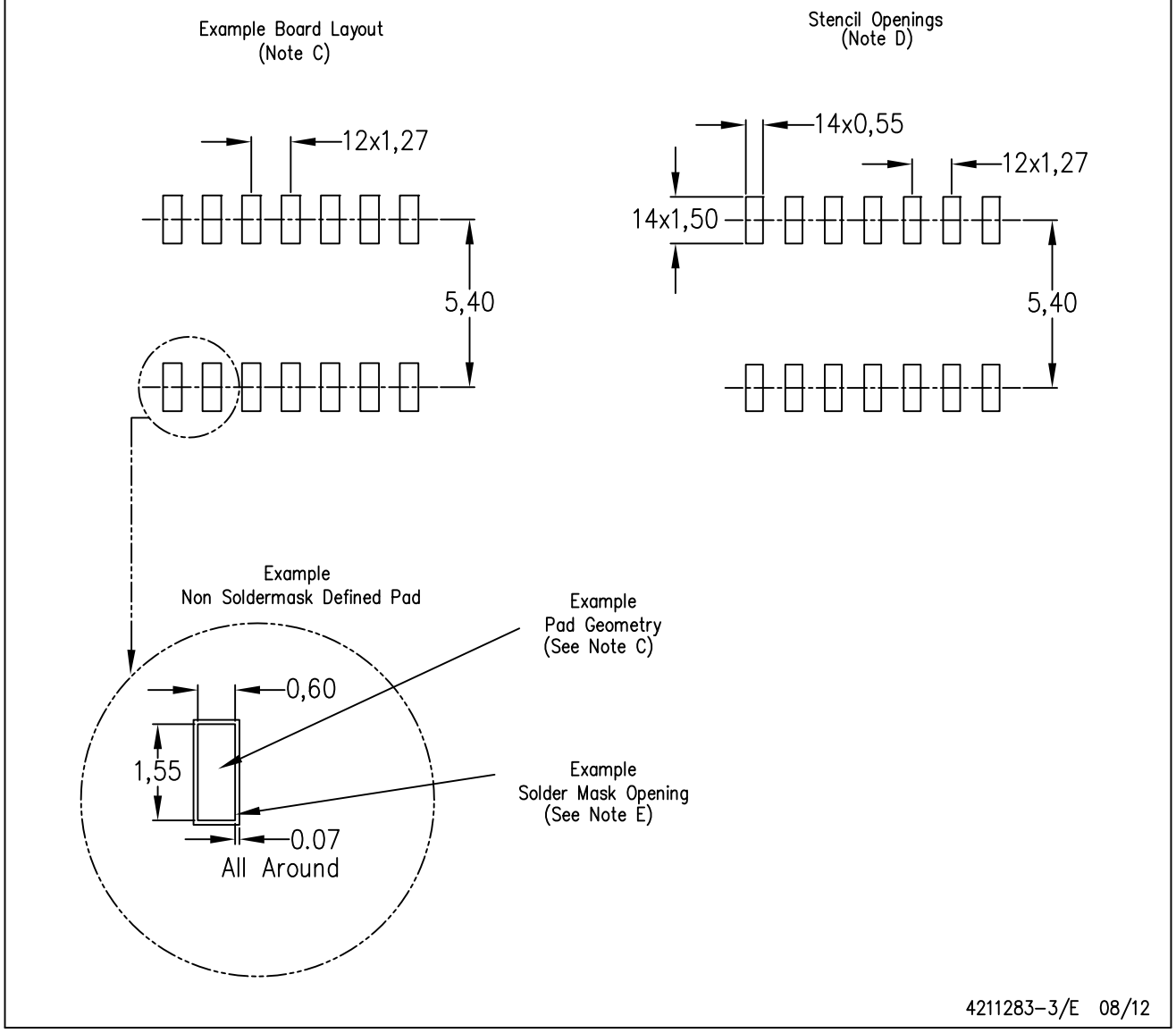
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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