TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9318AFAG, TC9318AFBG

Single Chip DTS Microcontroller (DTS-21)

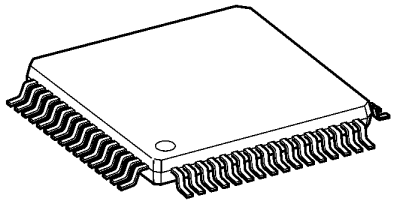
TC9318AFAG and TC9318AFBG are 4-bit CMOS microcontrollers for single-chip digital tuning systems incorporating 230 MHz prescaller, PLL and LCD driver.

The CPU has 4-bit parallel addition and subtraction instructions (e.g., AI, SI), logic operation instructions (e.g., OR, AN), bit judge and compare instructions (e.g., TM, SL), and time base functions.

The package is 64 -pin, 0.5/0.65-mm-pitch quad flat type. In addition to various input/output ports and a dedicated key-input port controlled by powerful input/output instructions (IN 1, 2, OUT 1, 2), there are many dedicated LCD pins, a buzzer port, a 6-bit A/D converter and an IF counter.

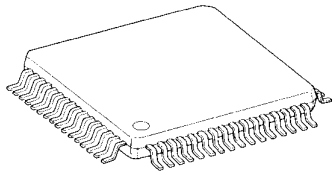
Because of low-voltage and low-current consumptions, this microcontroller is suitable for portable DTS equipment.

TC9318AFAG



P-LQFP64-1010-0.50E

TC9318AFBG



P-LQFP64-1212-0.65A

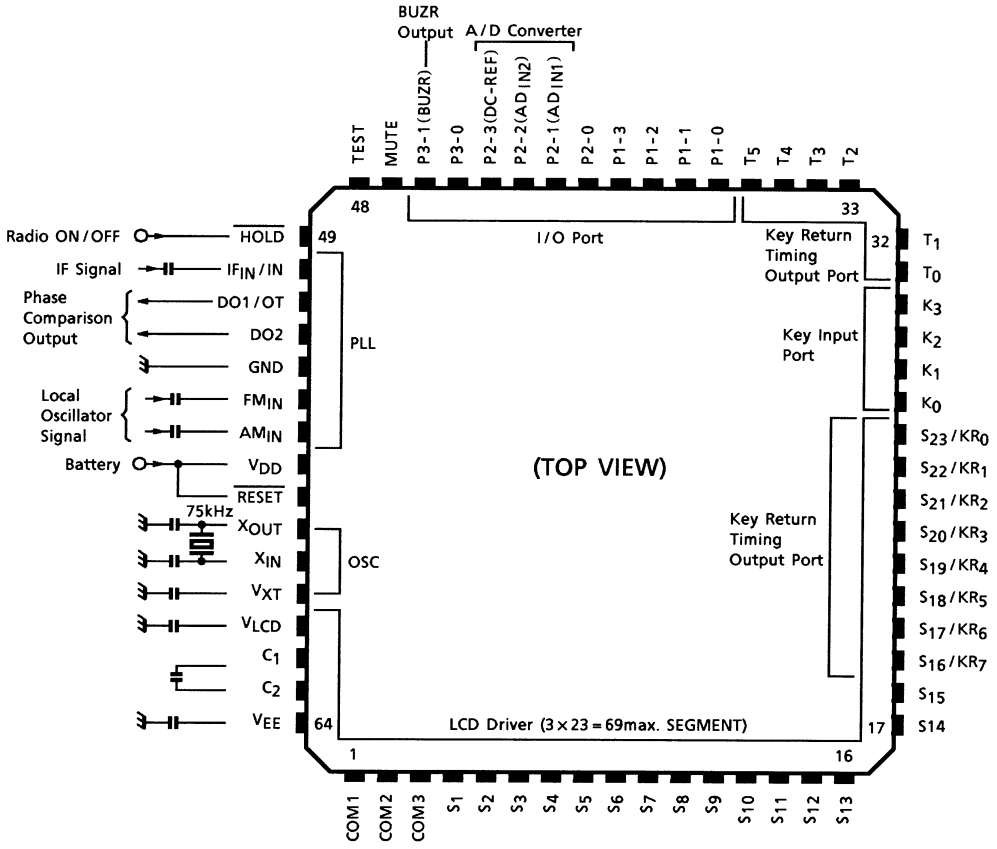
Weight
P-LQFP64-1010-0.50E: 0.32 g (typ.)
P-LQFP64-1212-0.65A: 0.45 g (typ.)

Features

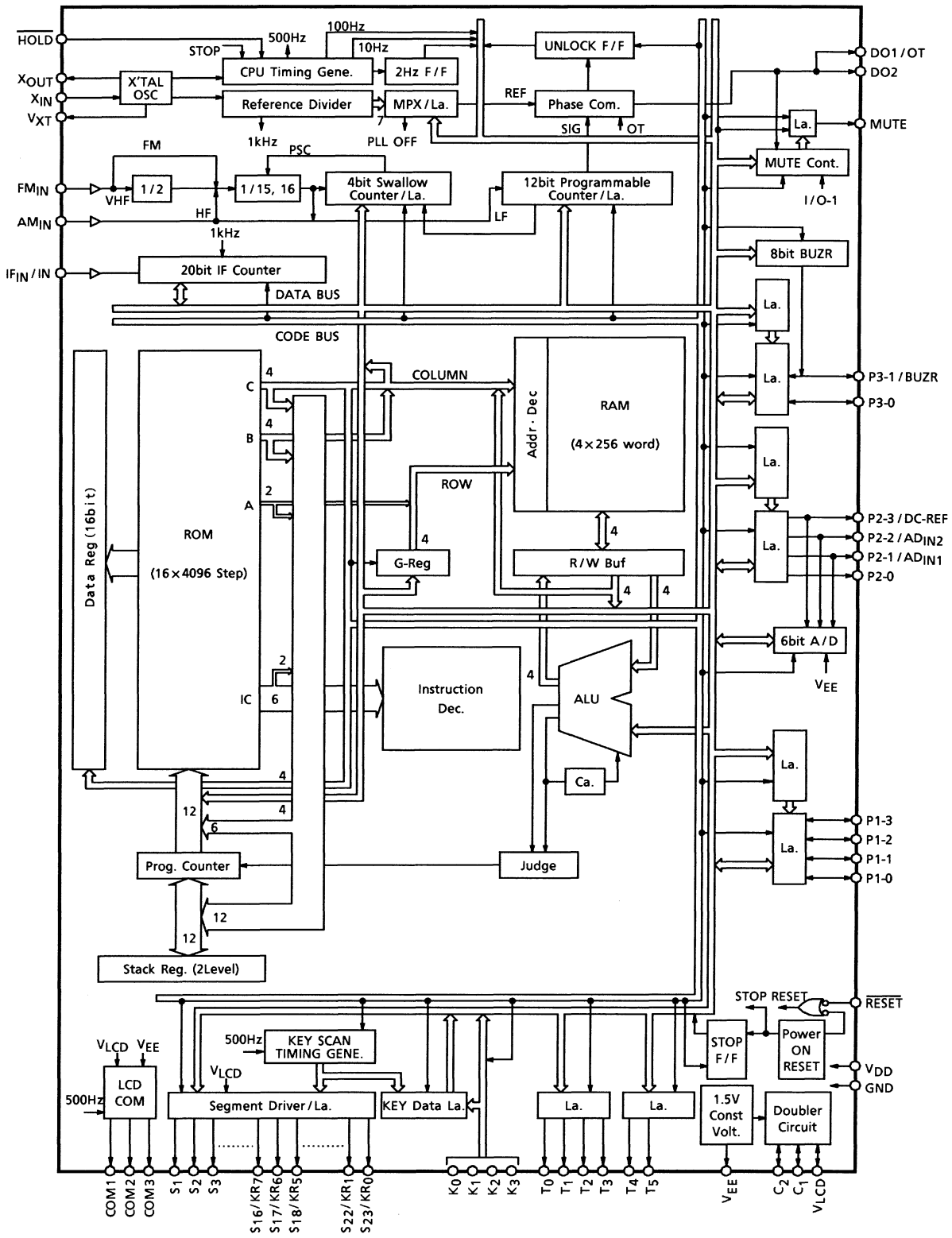
- 4-bit microcontroller for digital tuning systems
- Operating voltage: V_{DD} = 1.8 to 3.6 V
  Low current consumption because of CMOS circuitry
  When CPU operation: I_{DD} = 80 μA (max) at V_{DD} = 3 V
- Built-in prescaller (1/2 fixed divider + 2 modulus prescaller: fmax ≥ 230 MHz)
- Built-in 1/3-duty, 1/2-bias LCD drivers and 3-V booster circuit for the display
- Data memory (RAM) and ports are easily backed up.
- Program memory (ROM): 16-bit × 4096 steps
- Data memory (RAM): 4-bit × 256 words
- Instruction set consisting of 60 single-word instructions
- Instruction execution time: 40 μs (with 75 kHz crystal) (MVGS and DAL instructions: 80 μs)
- Many addition and subtraction instructions (12 types of addition instructions, 12 types of subtraction instructions)
- Powerful bit judgment instructions (TMTR, TMFR, TMT, TMF, TMTN and TMFN)
- Data transfer to the same row address is available (MVSR instruction)
- Register indirect transfer is available (MVGD and MVGS instructions).
- 16 powerful general registers (located in RAM)
- Stack levels: 2
- JUMP or CAL instruction can be used anywhere in the 4096 steps of program memory (ROM) as there are no pages or fields.
- 16 bit of any address in the 1024 steps in program memory (ROM) can be referenced (DAL instruction).
- Independent frequency input pins (FM_{IN} and AM_{IN}) and two (DO1 and DO2) phase comparator outputs for FM/VHF and AM.
- Seven types of reference frequencies selectable by the program
- Powerful input/output instructions (IN 1, 2, OUT 1, 2)
- Dedicated input ports (K_0 to K_3) for key input. 26 LCD drive pins (69 segments max) are available.
- 17 I/O ports: 10 with input/output programmable in 1-bit units, and 7 output-only ports. The IF_{IN} and DO1 pins can be switched by the instruction to IN (input-only port) or OT (output-only port).

- Three types of back-up modes selectable by the instruction: only CPU operation mode, only crystal oscillation mode, and clock stop mode.
- Built-in 2 Hz timer F/F and 10/100 Hz interval pulse output (internal port for time base)
- PLL lock status detection is available.
- 8 of the LCD segment outputs (S_{16} to S_{23}) can also operate as key return timing outputs (KR_0 to KR_7). The I/O ports are not dedicated to key return timing outputs, but can be used for other purposes.
- Built-in 20-bit general-purpose IF counter can detect stations during auto-tuning by counting the intermediate frequencies of each band.
- Built-in 8-bit buzzer output circuit can produce 254 different tone signals.
- Built-in 2-channel 6-bit A/D converter
- To prevent CPU malfunctions, a built-in supply voltage drop detection circuit shuts down the CPU when voltage falls below 1.5 V.

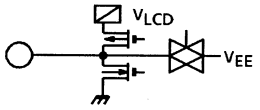
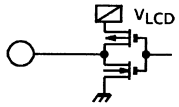
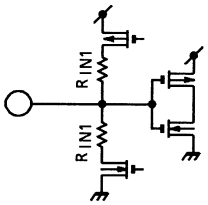
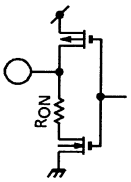
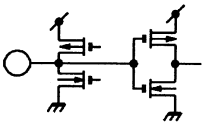
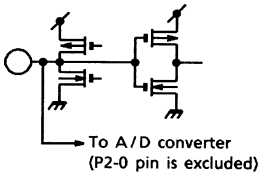
Pin Assignment (Top View)

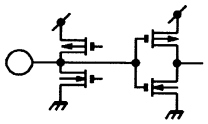
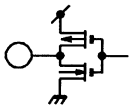
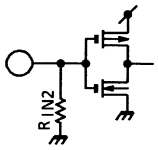
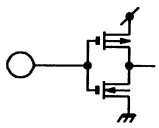


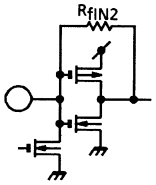
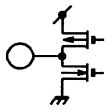
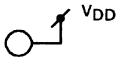
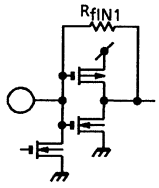
Block Diagram

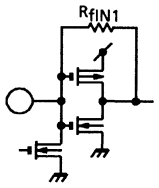
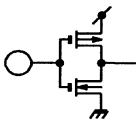


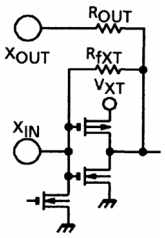
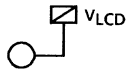
Explanation of Function

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
1	COM1	LCD common output	Output common signals to the LCD panel. Through a matrix with pins S_1 to S_{23}, a maximum of 69 segments can be displayed. Three levels, V_{LCD}, V_{EE}, and GND, are output at 83 Hz every 2 ms. V_{EE} is output after SYSTEM RESET and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0".	
2	COM2			
3	COM3			
4 to 18	S_1 toS_{15}	LCD segment output	Segment signal output pins for the LCD panel. Together with COM1, COM2, and COM3, a matrix is formed to display a maximum of 69 segments. The signals for the key matrix and the segment signals from pins S_{16}/KR_7 to S_{23}/KR_0 are output on a time division basis. $4 \times 8 = 32$ key matrix can be created in conjunction with key input ports K_0 to K_3.	
19 to 26	S_{16}/KR_7 to S_{23}/KR_0	LCD segment output/Key return timing output		
27 to 30	K_0 to K_3	Key input ports	4-bit input ports for key matrix input. Combined in a matrix with key return timing outputs of the LCD segment pins (KR0 to KR7), data from a maximum of $4 \times 8 = 32$ keys can be input and pins are pulled up. Combined in a matrix with T-port output pins (T0 to T5), data from $4 \times 6 = 24$ keys can be input and pins are pulled down. The WAIT mode is released when high level is applied to key input ports set to pull-down.	
31 to 36	T_0 to T_5	Key return timing output port	These ports output the timing signal for key matrix. To form the key matrix, load resistance is incorporated in the N-channel side. When the key matrix is combined with the push-key, a key matrix diode is not required.	
37 to 40	P1-0 to P1-3	I/O port 1	The input and output of these 4-bit I/O ports can be programmed in 1-bit units. By setting I/O ports to input, the CLOCK STOP mode can be released, and the MUTE bit of the MUTE pin can be set to "1".	
41to44	P2-0 P2-1/AD_{IN1} P2-2/AD_{IN2} P2-3/ DC-REF	I/O port 2 /AD analog voltage input /AD analog voltage input /Reference voltage input	4 bit I/O ports. Input and output can be programmed in 1-bit units. P2-1 to P2-2 can also be used as analog input to the built-in 6-bit 2-channel A/D converter. Conversion time of the built-in A/D converter using the successive comparison method is 280 μs. The necessary pin can be programmed to the AD analog input in 1-bit units. P2-3 can be set to the reference voltage input. Internal power supply (V_{DD}) or constant voltage (V_{EE}) can be used as the reference voltage. In addition, constant voltage (V_{EE}) can be input to the AD analog input so battery voltage can be detected easily. The reference voltage input for which a built-in operational amp is used is at high impedance. The A/D converter and all associated controls are all executed by the program.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
45to46	P3-0 P3-1/BUZR	I/O port 3 /Buzzer output	2-bit I/O ports whose input/output can be programmed in 1-bit units. The P3-1 pin also is used as the output for the built-in buzzer circuit. The buzzer sound can be output in 254 different tones between 18.75 kHz and 147 Hz, and at a duty of 50%. The buzzer output and all associated controls can be programmed.	
47	MUTE	Muting output port	1-bit output port. Normally, this port is used for muting control signal output. This pin can set the internal MUTE bit to "1" according to a change in the input to the I/O port 1. MUTE bit output logic can be changed; PLL phase difference can also be output using this pin.	
48	TEST	TEST mode control input	Input pin used for controlling TEST mode. High level indicates TEST mode, while low level indicates normal operation. The pin is normally used at low level or in no-connection (NC) state. (a pull-down resistor is built in).	
49	$\overline{\text{HOLD}}$	HOLD mode control input	Input pin for request/release HOLD mode. Normally, this pin is used to input radio mode selection signals or battery detection signals. HOLD mode includes CLOCK STOP mode (stops crystal oscillation) and WAIT mode (halts CPU). Setting is implemented with the CKSTP instruction or the WAIT instruction. When the CKSTP instruction is executed, request/release of the HOLD mode depends on the internal MODE bit. If the MODE bit is "0" (MODE-0), executing the CKSTP instruction while the $\overline{\text{HOLD}}$ pin is at low level stops the clock generator and the CPU, and changes to memory back-up mode. If the MODE bit is "1" (MODE-1), executing the CKSTP instruction enters memory back-up mode regardless of the level of the $\overline{\text{HOLD}}$ pin. Memory back-up is released when the $\overline{\text{HOLD}}$ pin goes high in MODE-0, or when the level of the $\overline{\text{HOLD}}$ pin changes in MODE-1. When memory back-up mode is entered by executing a WAIT instruction, any change in the $\overline{\text{HOLD}}$ pin input releases the mode. In memory back-up mode, current consumption is low (below 10 μA), and all the output pins (e.g., display output, output ports) are automatically set to low level.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
50	IF_{IN}/IN	IF signal input/Input port	IF signal input pin for the IF counter to count the IF signals of the FM and AM bands and to detect the automatic stop position. The input frequency is between 0.35 to 12 MHz (0.2 V_{p-p} (min)). A built-in input amp and C coupling allow operation at low-level input. The IF counter is a 20-bit counter with optional gate times of 1, 4, 16, and 64 ms. 20 bits of data can be readily stored in memory. This input pin can be programmed for use as an input port (IN port). CMOS input is used when the pin is set as an IN port.	
51 52	DO1/OT DO2	Phase comparator output/Output port Phase comparator output	PLL phase comparator tri-state output pins. When the programmable counter prescaller output is higher than the reference frequency, output is at high level. When output is lower than the reference frequency, output is at low level. When output equals the reference frequency, high impedance output is obtained. Because DO1 and DO2 are output in parallel, optimal filter constants can be designed for the FM/VHF and AM bands. DO1 can be programmed to high impedance or programmed as an output port (OT).Therefore, DO1 and DO2 can be used to improve lock-up time or used as output ports.	
56	V_{DD}	Power-supply pins	Pins to which power is applied. Normally, V_{DD} = 1.8 to 3.6 V (3.0 V typ.) is applied. In back-up mode (when CKSTP instructions are executed), the power supply voltage can be reduced to 1.0 V. If the power supply voltage falls below 1.5 V while the CPU is operating, the CPU stops to prevent malfunction (STOP mode). When the power supply voltage rises above 1.5 V, the CPU restarts.	
53	GND		STOP mode can be detected by checking the STOP F/F bit. If necessary, execute initialization or adjust clock by program. When detecting or preventing CPU malfunctions using an external circuit, STOP mode can be invalidated by program. In that case, all four bits of the internal TEST port should be set to "1". If more than 1.8 V is applied when the pin voltage is 0, the device system is reset and the program starts from address "0". (Power on reset) Note: To operate the power on reset, the power supply should start up in 10 to 100 ms.	
54	FM_{IN}	FM programmable counter input	Programmable counter input pin for FM/VHF band. The 1/2 + pulse swallow system (VHF mode) and the pulse swallow system (FM mode) are selectable freely by program. Local oscillation output (VCO output) of 50 to 230 MHz (0.2V_{p-p} (min)) is input in VHF mode; and 40 to 130 MHz (0.2V_{p-p} (min)) in FM mode. With an input amp incorporated, capacitive coupling, small-amplitude operation. Note: The input is pulled down in the PLL OFF mode or when set to AM_{IN} input	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
55	AM_{IN}	AM local oscillator signal input	Programmable counter input pin for AM band. The pulse swallow system (HF mode) and direct dividing system (LF mode) are freely selectable by program. Local oscillation output (VCO output) of 1 to 45 MHz (0.2 V_{p-p} (min)) is input in HF mode, and 0.5 to 12 MHz (0.2 V_{p-p} (min)) in LF mode. With an input amp incorporated, capacitive coupling, small-amplitude operation. Note: The input is pulled down in the PLL OFF mode or when set to FM_{IN} input.	
57	$\overline{RESET}$	Reset input	Input pin for system reset signals. $\overline{RESET}$ takes place while at low level; at high level, the program starts from address “0”. Normally, if more than 1.8 V is supplied to V_{DD} when the voltage is 0, the system is reset (power on reset). Accordingly, this pin should be set to high level during operation.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
58	X_{OUT}	Crystal oscillator pins	Crystal oscillator pins. A reference 75-kHz crystal oscillator is connected to the X_{IN} and X_{OUT} pins The oscillator stops oscillating during CKSTP instruction execution. The V_{XT} pin is the power supply for the crystal oscillator. A stabilizing capacitor (0.47 μF typ.) is connected.	
59	X_{IN}			
60	V_{XT}			
61	V_{LCD}	Voltage doubler boosting pins	Voltage doubler boosting pins for driving the LCD. A voltage doubler boosting capacitor (0.1 μF typ.) is connected to boost the voltage. The V_{LCD} pin outputs voltage (3.0 V), which has been doubled from the constant voltage (V_{EE}: 1.5 V) using the voltage doubler boosting capacitor between C_1 and C_2. That potential is supplied to the LCD drivers	
62	C_1			
63	C_2			
64	V_{EE}	Constant voltage supply pin	1.5 V constant voltage supply pin for driving the LCD. A stabilizing capacitor (0.1 μF typ.) is connected. This is a reference voltage for the A/D converter, key input, and the LCD common output's bias potential.	—

Note 1: When the device is reset (voltage higher than 1.8 V, or when $\overline{\text{RESET}}$ = Low → High) I/O ports are set to input, the pins for I/O ports and additional functions (e.g., A/D converter) are set to I/O port input pins, while the IF_{IN}/IN pins become IF input pins.

Note 2: In PLL OFF mode (when the three bits in the internal reference ports are set to "1"), IF_{IN}, FM_{IN} and AM_{IN} are pulled down, and DO1 and DO2 are at high impedance.

Note 3: In CLOCK STOP mode (during execution of CKSTP instruction), the output ports and LCD output pins are all at low level, while the constant voltage circuit (V_{EE}), the voltage doubler circuit (V_{LCD}), and the power supply for the crystal oscillator (V_{XT}) are all off.

Note 4: When the device is being reset, the contents of the output ports and internal ports are undefined and initialization by program is necessary.

Description of Operations

CPU

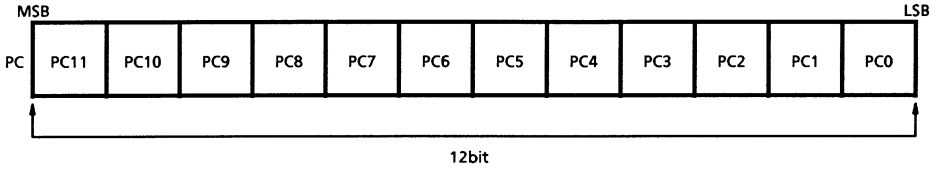
CPU is composed of program counter, stack register, ALU, program memory, data memory, G-register, carry F/F and judgment circuit.

1. Program Counter (PC)

The program counter consists of a 12-bit binary up-counter and addresses the program memory (ROM). The program counter is cleared by system reset, and the programs start from the 0 address.

Normally, the counter is increased in increments of one whenever an instruction is executed, but the address specified in the instruction operand is loaded when a JUMP instruction or CALL instruction is executed.

When an instruction that is equipped with the skip function (AIS, SLTI, TMT RNS instructions, etc.) is executed and the result of this includes a skip condition, the program counter is increased in increments of two and the subsequent instruction is skipped.



2. Stack Register (STACK)

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This is a register composed of 2 x 12 bits which stores the contents of the program counter + 1 (the return address) when the sub-routine call instruction is executed. The contents of the stack register are loaded into the program counter when the return instruction (RN, RNS instructions) is executed.

There are two stack levels available and nesting occurs up to two levels.

3. ALU

ALU is equipped with binary 4-bit parallel add/subtract functions, logical operation, comparison and multiple bit judgment functions.

This CPU is not equipped with an accumulator, and all operations are handled directly within the data memory.

4. Program Memory (ROM)

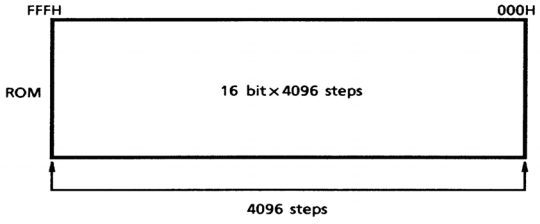
Program memory is composed of 16 bit × 4096 steps and is used to store programs. The usable address range consists of 16384 steps between address 000H and FFFH.

Program memory has no concept of pages or fields, so JUMP instruction and CAL instruction can be used anywhere in the 4096 steps of program memory (ROM).

Any program memory addresses may be used as data area. The 16-bit contents of this area can be loaded into the data register by execution the DAL instruction.

Note 5: Set the address for the data area of the program memory outside of the program loop.

Note 6: The DAL instruction can use 1024 steps between address 000H to 3FFH as the data area.



5. Data Memory (RAM)

The data memory is composed of 4 bit × 256 words and used to store data.

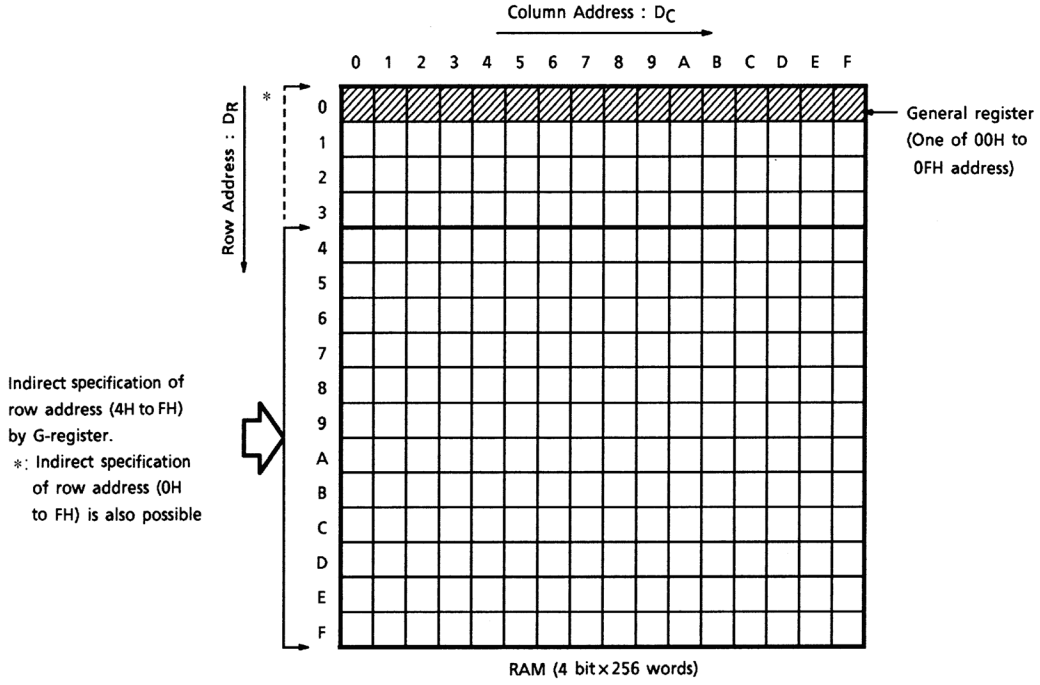
These 256 words are expressed in row address (4 bits) and column address (4 bits).

192 words (row address = 4H to FH) within the data memory are addressed indirectly by the G-register. Therefore, it is necessary to specify the row address with the G-register before the data in this area is processed.

The address 00H to 0FH within the data memory are known as general registers, and these can be used simply by specifying the relevant column address (4 bits). These sixteen general registers can be used for operations and transfers with the data memory, and may also be used as normal data memories.

Note 7: The column address (4 bits) to designate the general register is the register number of the general register.

Note 8: All row addresses (addresses 0H to FH) can be specified indirectly with the G-register.



6. G-Register (G-REG.)

The G-register is a 4-bitregister used for addressing row address (D_R = 4H to FH) of 192 words in data memory.

The contents of this register are effective during execution of the MVGD instruction or MVGS instruction, and not affected with the execution of any other instructions.

This register is used as one of the ports, and its contents are set by the execution of OUT1 instruction among input and output instructions.

7. Data Register (DATA REG.)

The data register consists of 1 x 16 bits and loads 16 bits of optional address data in the program memory during execution of the DAL instruction. This register is used as one of the ports, and the contents are loaded into the data memory in units of 4 bits when the IN1 instruction among the I/O instruction is executed.

8. Carry F/F (C·F/F)

This is set when either Carry or Borrow is issued in the result of calculation instruction execution and is reset if neither of these is issued.

The contents of carry F/F can only be modified through the execution of the addition and subtraction instructions, and not affected by the execution of any other instructions.

9. Judgment Circuit (J)

This circuit judges the skip conditions when an instruction with the skip function is executed. The program counter is increased by two when the skip conditions are satisfied, and the subsequent instruction is skipped.

There are 29 instructions equipped with a wide variety of skip functions.

(Refer to * marked instructions in "11.Table of Instruction Functions and Operational Instructions"

10. Instruction Set Table

A total of 60 instructions are available, and all of these are single-word instructions.

These instructions are expressed with 6-bits instruction codes.

Upper 2 Bits / Lower 4 Bits		00		01		10		11	
		0		1		2		3	
0000	0	AI	M, I	AD	r, M	TMTR	r, M	SLTI	M, I
0001	1	AIS	M, I	ADS	r, M	TMFR	r, M	SGEI	M, I
0010	2	AIN	M, I	ADN	r, M	SEQ	r, M	SEQI	M, I
0011	3	AIC	M, I	AC	r, M	SNE	r, M	SNEI	M, I
0100	4	AICS	M, I	ACS	r, M	LD	r, M	TMTN	M, N
0101	5	AICN	M, I	ACN	r, M	ST	M, r	TMT	M, N
0110	6	ORIM	M, I	ORR	r, M	MVGD	r, M	TMFN	M, N
0111	7	ANIM	M, I	ANDR	r, M	MVGS	M, r	TMF	M, N
1000	8	SI	M, I	SU	r, M	CALL $ADDR_1$		IN1	M, C
1001	9	SIS	M, I	SUS	r, M			IN2	M, C
1010	A	SIN	M, I	SUN	r, M			—	
1011	B	SIB	M, I	SB	r, M			OUT1	C, M
1100	C	SIBS	M, I	SBS	r, M	JUMP $ADDR_1$		OUT2	C, M
1101	D	SIBN	M, I	SBN	r, M			—	
1110	E	XORI	M, I	XORR	r, M			DAL $ADDR_2$, r	
1111	F	MVIM	M, I	MVSR	M_1, M_2			RN, RNS, WAIT CKSTP, NOOP	

11. Table of Instruction Functions and Operational Instructions (Description of the symbols used in the table)

M: Data memory address
Normally, one of the addresses among the addresses 00H to3FH in the data memory.
r: General register
One of the addresses among the addresses 00H to 0FH in the data memory.
PC: Program counter (12 bits)
STACK: Stack register (12 bits)
G: G-register (4 bits)
DATA: Data register (16 bits)
I: Immediate data (4 bits)
N: Bit position (4 bits)
—: All "0"
C: Port code number (4 bits)
C_N: Port code number (4 bits)
R_N: General register number (4 bits)
$ADDR_1$: Program memory address (12 bits)
$ADDR_2$: Upper 6 bits of the program memory address in the page 0
Ca: Carry
b: Borrow
IN1to IN2: Port used during the execution of IN1to IN2 instructions
OUT1to OUT2: Port used during the execution of OUT1the OUT2 instructions
( ): Contents of the register or data memory
[ ] C: Contents of the port indicated by the code No. C (4 bits)
[ ]: Contents of the data memory indicated by the contents of the register or data memory
[ ] P: Contents of the program memory (16 bits)
IC: Instruction code (6 bits)
*: Instruction equipped with the skip function
D_C: Data memory column address (4 bits)
D_R: Data memory row address (2 bits)
P: Wait condition

Inst. Gr.	Mnemonic		Skip Function	Function Description	Operation Description	Machine Language (16 bits)			
						IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
ADDITION INSTRUCTION	AI	M, I		Add immediate data to memory	M ← (M) + I	000000	D_R	D_C	I
	AIS	M, I	*	Add immediate data to memory, then skip if carry	M ← (M) + I Skip if carry	000001	D_R	D_C	I
	AIN	M, I	*	Add immediate data to memory, then skip if not carry	M ← (M) + I Skip if not carry	000010	D_R	D_C	I
	AIC	M, I		Add immediate data to memory with carry	M ← (M) + I + ca	000011	D_R	D_C	I
	AICS	M, I	*	Add immediate data to memory with carry, then skip if carry	M ← (M) + I + ca Skip if carry	000100	D_R	D_C	I
	AICN	M, I	*	Add immediate data to memory with carry, then skip if not carry	M ← (M) + I + ca Skip if not carry	000101	D_R	D_C	I
	AD	r, M		Add memory to general register	r ← (r) + (M)	010000	D_R	D_C	R_N
	ADS	r, M	*	Add memory to general register, then skip if carry	r ← (r) + (M) Skip if carry	010001	D_R	D_C	R_N
	ADN	r, M	*	Add memory to general register, then skip if not carry	r ← (r) + (M) Skip if not carry	010010	D_R	D_C	R_N
	AC	r, M		Add memory to general register with carry	r ← (r) + (M) + ca	010011	D_R	D_C	R_N
	ACS	r, M	*	Add memory to general register with carry, then skip if carry	r ← (r) + (M) + ca Skip if carry	010100	D_R	D_C	R_N
	ACN	r, M	*	Add memory to general register with carry, then skip if not carry	r ← (r) + (M) + ca Skip if not carry	010101	D_R	D_C	R_N

Inst. Gr.	Mnemonic		Skip Function	Function Description	Operation Description	Machine Language (16 bits)			
						IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
SUBTRACTION INSTRUCTION	SI	M, I		Subtract immediate data from memory	M ← (M) – I	001000	D_R	D_C	I
	SIS	M, I	*	Subtract immediate data from memory, then skip if borrow	M ← (M) – I Skip if borrow	001001	D_R	D_C	I
	SIN	M, I	*	Subtract immediate data from memory, then skip if not borrow	M ← (M) – I Skip if not borrow	001010	D_R	D_C	I
	SIB	M, I		Subtract immediate data from memory with borrow	M ← (M) – I – b	001011	D_R	D_C	I
	SIBS	M, I	*	Subtract immediate data from memory with borrow, then skip if borrow	M ← (M) – I – b Skip if borrow	001100	D_R	D_C	I
	SIBN	M, I	*	Subtract immediate data from memory with borrow, then skip if not borrow	M ← (M) – I – b Skip if not borrow	001101	D_R	D_C	I
	SU	r, M		Subtract memory from general register	r ← (r) – (M)	011000	D_R	D_C	R_N
	SUS	r, M	*	Subtract memory from general register, then skip if borrow	r ← (r) – (M) Skip if borrow	011001	D_R	D_C	R_N
	SUN	r, M	*	Subtract memory from general register, then skip if not borrow	r ← (r) – (M) Skip if not borrow	011010	D_R	D_C	R_N
	SB	r, M		Subtract memory from general register with borrow	r ← (r) – (M) – b	011011	D_R	D_C	R_N
	SBS	r, M	*	Subtract memory from general register with borrow, then skip if borrow	r ← (r) – (M) – b Skip if borrow	011100	D_R	D_C	R_N
	SBN	r, M	*	Subtract memory from general register with borrow, then skip if not borrow	r ← (r) – (M) – b Skip if not borrow	011101	D_R	D_C	R_N
COMPARE INSTRUCTION	SLTI	M, I	*	Skip if memory is less than immediate data	Skip if (M) < I	110000	D_R	D_C	I
	SGEI	M, I	*	Skip if memory is greater than or equal to immediate data	Skip if (M) ≧ I	110001	D_R	D_C	I
	SEQI	M, I	*	Skip if memory is equal to immediate data	Skip if (M) = I	110010	D_R	D_C	I
	SNEI	M, I	*	Skip if memory is not equal to immediate data	Skip if (M) ≠ I	110011	D_R	D_C	I
	SEQ	r, M	*	Skip if general register is equal to memory	Skip if (r) = (M)	100010	D_R	D_C	R_N
	SNE	r, M	*	Skip if general register is not equal to memory	Skip if (r) ≠ (M)	100011	D_R	D_C	R_N

Inst. Gr.	Mnemonic		Skip Function	Function Description	Operation Description	Machine Language (16 bits)			
						IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
TRANSFER INSTRUCTION	LD	r, M		Load memory to general register	$r \leftarrow (M)$	100100	D_R	D_C	R_N
	ST	M, r		Store general register to memory	$M \leftarrow (r)$	100101	D_R	D_C	R_N
	MVSR	M_1, M_2		Move memory to memory in the same row	$(D_R, D_{C1}) \leftarrow (D_R, D_{C2})$	011111	D_R	D_{C1}	D_{C2}
	MVIM	M, I		Move immediate data to memory	$M \leftarrow I$	001111	D_R	D_C	I
	MVGD	r, M		Move memory to destination memory referring to G-register and general register	$[(G), (r)] \leftarrow (M)$	100110	D_R	D_C	R_N
	MVGS	M, r		Move source memory referring to G-register and general register to memory	$M \leftarrow [(G), (r)]$	100111	D_R	D_C	R_N
INPUT AND OUTPUT INSTRUCTION	IN1	M, C		Input IN1 port data to memory	$M \leftarrow [IN1]_C$	111000	D_R	D_C	C_N
	OUT1	C, M		Output contents of memory to OUT1 port	$[OUT1]_C \leftarrow (M)$	111011	D_R	D_C	C_N
	IN2	M, C		Input IN2 port data to memory	$M \leftarrow [IN2]_C$	111001	D_R	D_C	C_N
	OUT2	C, M		Output contents of memory to OUT2 port	$[OUT2]_C \leftarrow (M)$	111100	D_R	D_C	C_N
LOGICAL OPERATION INSTRUCTION	ORR	r, M		Logical OR of general register and memory	$r \leftarrow (r) \vee (M)$	010110	D_R	D_C	R_N
	ANDR	r, M		Logical AND of general register and memory	$r \leftarrow (r) \wedge (M)$	010111	D_R	D_C	R_N
	ORIM	M, I		Logical OR of memory and immediate data	$M \leftarrow (M) \vee I$	000110	D_R	D_C	I
	ANIM	M, I		Logical AND of memory and immediate data	$M \leftarrow (M) \wedge I$	000111	D_R	D_C	I
	XORIM	M, I		Logical exclusive OR of memory and immediate data	$M \leftarrow (M) \oplus I$	001110	D_R	D_C	I
	XORR	r, M		Logical exclusive OR of general register and memory	$r \leftarrow (r) \oplus (M)$	011110	D_R	D_C	R_N
BIT JUDGE INSTRUCTION	TMTR	r, M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r [N (M)] = all “1”	100000	D_R	D_C	R_N
	TMFR	r, M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r [N (M)] = all “0”	100001	D_R	D_C	R_N
	TMT	M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = all “1"	110101	D_R	D_C	N
	TMF	M, N	*	Test memory bits, then skip if all bits specified are false	Skip if M (N) = all “0”	110111	D_R	D_C	N
	TMTN	M, N	*	Test memory bits, then not skip if all bits specified are true	Skip if M (N) = not all “1"	110100	D_R	D_C	N
	TMFN	M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = not all “0”	110110	D_R	D_C	N

Inst. Gr.	Mnemonic	Skip Function	Function Description	Operation Description	Machine Language (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
SUBROUTINE INSTRUCTION	CALL $ADDR_1$		Call subroutine	STACK ← (PC) + 1 and PC ← $ADDR_1$	1010	$ADDR_1$ (12 bit)		
	RN		Return to main routine	PC ← (STACK)	111111	00	—	—
	RNS	*	Return to main routine and skip unconditionally	PC ← (STACK) and skip	111111	01	—	—
JUMP INST.	JUMP $ADDR_1$		Jump to the address specified	PC ← $ADDR_1$	1011	$ADDR_1$ (12 bit)		
OTHER INSTRUCTION	DAL $ADDR_2$, r		Load program memory in page 0 to DATA register	DATA ← $[ADDR_2 + (r)]_P$ in page 0	111110			R_N
	WAIT P		At P = "0" H, the condition is CPU waiting (soft wait mode)	Wait at condition P	111111	10	0000	P
			At P = "1" H, except for clock generator, all function is waiting (hard wait mode)					
	CKSTP		Clock generator stop	Stop clock generator at MODE condition	111111	10	1000	—
	NOOP		No operation	—	111111	11	—	—

Note 9: The lower four bits among the ten-bit address of the program memory specified with the DAL instruction are addressed indirectly with the contents of the general register.

The execution period for the DAL instruction is 80 μs (two machine cycles.)

Note 10: The execution period for the MVGS instruction is 80 μs (two machine cycles.)

I/O Map

All of the ports within the device are expressed with a matrix of four I/O instructions (OUT 1 to 2 instructions and IN 1 to 2 instructions) and a 4-bit code number.

The allocation of these ports is shown on the following page in the form of an I/O map. The ports used in the execution of the various I/O instructions on the horizontal axis of the I/O map are allocated to the port code numbers indicated on the vertical axis. The G-register, data register, DAL address register and DAL bits are also used as ports.

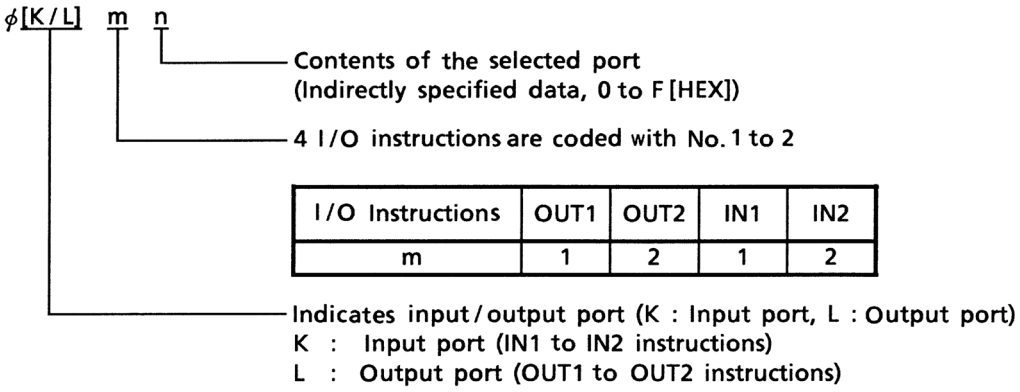
The OUT1 to 3 instructions are specified as output ports and the IN 1 to 2 instructions are specified as input ports.

Note 11: The ports indicated by the angled lines on the I/O map do not actually exist within the device. The contents of other ports and data memories are not affected when data is output to a non-existent output port with the execution of the output instruction. The data loaded from data memories is "1" when a non-existent input port has been specified with the execution of an input instruction.

Note 12: The output ports marked with an asterisk (*) on the I/O map are not used. Data output to these ports assume the don't care's status

Note 13: The Y1 contents of the ports expressed in 4 bits correspond to the least significant bit of the data memory and the Y8 contents correspond to the most significant bit.

The ports specified with the four I/O instructions and code No. C are coded in the following manner:



I/O Instructions	OUT1	OUT2	IN1	IN2
m	1	2	1	2

(Example) The setting for the G-register is allocated to code "F" in the OUT1 instruction. The encoded expression at this time becomes "ϕL1F".

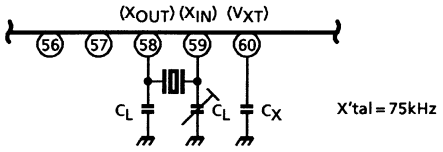
I/O Map

	I/O	φL1				φL2				φK1				φK2			
		OUT1				OUT2				IN1				IN2			
	Code	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
CN	0	HF	IF OFFSET		FM	A/D CONTROL				IF CONTROL			1	A/D DATA			
			+1	−1		AD SEL0	AD SEL1	REF SEL0	REF SEL1	BUSY	MANUAL	OVER		AD0	AD1	AD2	AD3
	1	PROGRAMMABLE COUNTER				A/D CONTROL				IF DATA				A/D DATA			1
		P0	P1	P2	P3	STA	DCREF ON	AD1 ON	AD2 ON	F0	F1	F2	F3	AD4	AD5	BUSY	
	2	PROGRAMMABLE COUNTER				I/O-1 DATA				IF DATA				I/O-1 DATA			
		P4	P5	P6	P7	−0	−1	−2	−3	F4	F5	F6	F7	−0	−1	−2	−3
	3	PROGRAMMABLE COUNTER				I/O-2 DATA				IF DATA				I/O-2 DATA			
		P8	P9	P10	P11	−0	−1	−2	−3	F8	F9	F10	F11	−0	−1	−2	−3
	4	PROGRAMMABLE COUNTER				I/O-3 DATA		*		IF DATA				I/O-3 DATA		1	
		P12	P13	P14	P15	−0	−1			F12	F13	F14	F15	−0	−1		
	5	REFERENCE SELECT			PROGURAMMABLE COUNTER	I/O-1 CONTROL				IF DATA							
		R0	R1	R2	P16	−0	−1	−2	−3	F16	F17	F18	F19				
	6	IF COUNTER CONTROL				I/O-2 CONTROL								KEY INPUT DATA			
		IF/IN	*	*	*	−0	−1	−2	−3					K0	K1	K2	K3
	7	IF COUNTER CONTROL				I/O-3 CONTROL				UNLOCK		IN PORT		KEY SCAN DIGIT			1
		STA/$\overline{\text{STP}}$	MANUAL	G0	G1	−0	−1	*	*	F/F	ENABLE	IN	1	KS0	KS1	KS2	
	8	MUTE	MUTE CONTROL			KEY RETURN TIMING								KEY SCAN INPUT DATA-0			
			I/O	POL	UNLOCK	T0	T1	T2	T3					KS00	KS01	KS02	KS03
	9	UNLOCK RESET	DO1 CONTROL			KEY RETURN TIMING		*						KEY SCAN INPUT DATA-1			
			OTC	OT	Hz	T4	T5							KS10	KS11	KS12	KS13
	A	TIMER RESET		TEST DATA						TIMER			STOP F/F	KEY SCAN INPUT DATA-2			
		2Hz F/F	TIMER	#4	#5					2Hz F/F	10 Hz	100 Hz		KS20	KS21	KS22	KS23
	B	BUZR DATA								$\overline{\text{HOLD}}$	1			KEY SCAN INPUT DATA-3			
		B0	B1	B2	B3									KS30	KS31	KS32	KS33
	C	BUZR DATA								DATA-reg				KEY SCAN INPUT DATA-4			
		B4	B5	B6	B7					d0	d1	d2	d3	KS40	KS41	KS42	KS43
	D	TEST DATA				SEG DATA SELECT				DATA-reg				KEY SCAN INPUT DATA-5			
		#0	#1	#2	#3	S1	S2	S4	S8	d4	d5	d6	d7	KS50	KS51	KS52	KS53
	E	*	BUZR ON	*	CKSTP MODE	SEG-1 DATA				DATA-reg				KEY SCAN INPUT DATA-6			
						COM1	COM2	COM3	*	d8	d9	d10	d11	KS60	KS61	KS62	KS63
	F	G REGISTER				SEG-2 DATA				DATA-reg				KEY SCAN INPUT DATA-7			
		G0	G1	G2	G3	COM1	COM2	COM3	*	d12	d13	d14	d15	KS70	KS71	KS72	KS73

Connecting Crystal Oscillator

75-kHz crystal oscillator is connected to the device's crystal oscillator pin (X_{IN}, X_{OUT}) as indicated below Usually, the oscillation signal is supplied to the clock generator, the reference frequency divider and other elements to generate the various CPU timing signals and reference frequency.

The power supply for the crystal oscillator circuit is the voltage (V_{XT} = 1.4 V typ.) supplied by the built-in constant voltage circuit. This stabilizes the crystal oscillation and reduces the current consumption.



Note 14: It is necessary to use a crystal oscillator with a low CI value and favorable start-up characteristics

System Reset

The device's system will be reset when the $\overline{RESET}$ pin is subject to the "L" level or when a voltage of 0 V to 1.8 V or more is supplied to the V_{DD} pin (power-on reset). The program starts from 0 address immediately after about 100 ms stand-by time. The $\overline{RESET}$ pin should be fixed at the "H" level as the power-on reset function is used under normal condition.

Note 15: The LCD common signal and the segment output will be fixed at the "L" level during system reset and the subsequent stand-by period.

Note 16: After a system reset, the internal ports shown in the following table are fixed at the specified levels. The states of the other ports after a reset are undefined. Therefore, initialize the ports in the program when necessary.

Fixed Internal Ports

Ports Set to "0"	Ports Set to "1"
MANUAL bit (ϕL17)	REFERENCE PORT (ϕL15)
IO, POL, UNLOCK bit (ϕL18)	MUTE bit (ϕL18)
DO1 CONTROL PORT (ϕL19)	IF/$\overline{IN}$ bit (ϕL16)
BUZR ON bit (ϕL1E)	DISP OFF bit (ϕL2FF)
TEST PORT (ϕL1A, ϕL1D)	
CKSTP MODE bit (ϕL1E)	
AD CONTROL PORT (ϕL20, ϕL21)	
TIMER PORT (ϕK1A)	
KEY RETURN SELECT bit (ϕL2FF)	
IO-1~IO-3 IO CONTROL PORT (ϕL25~ϕL27)	

Backup Modes

By executing CKSTP instruction or WAIT instruction, three kinds of back-up mode can be activated.

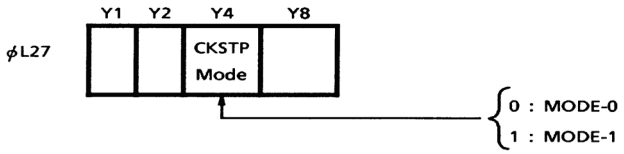
1. Clock Stop Mode

The clock stop mode is a function that halts system operations and maintains the internal status immediately prior to halt at a low level of current consumption (10 μA or below, at V_{DD} = 3.0 V). Crystal oscillations halt simultaneously, and output ports and output pins for LCD display are automatically fixed at the "L" level or fixed to off status (high impedances) automatically. The supply voltage can be reduced to 1.0 V with the clock stop mode.

Halt is activated at the CKSTP instruction execution address when the CKSTP instruction is executed. The next address is executed after approximately 100 ms of stand-by time when the clock stop mode is cancelled.

(1) Setting clock stop mode

There are two types of mode setting for the clock stop mode. The required setting is selected with the CKSTP MODE bit. This bit is accessed with the OUT1 instruction with the operand [CN = EH].



1) MODE-0

By setting this mode, the clock stop mode is assumed if the CKSTP instruction is executed when the $\overline{\text{HOLD}}$ pin is in the "L" level. The same operations as the NOOP instruction is assumed if the CKSTP instruction is executed when the $\overline{\text{HOLD}}$ pin is in the "H" level.

2) MODE-1

By setting this mode, the clock stop mode is assumed when the CKSTP instruction is executed regardless of the $\overline{\text{HOLD}}$ pin level.

Note 17: The PLL turns off during execution of the CKSTP instruction.

(2) Canceling clock stop mode

1) MODE-0

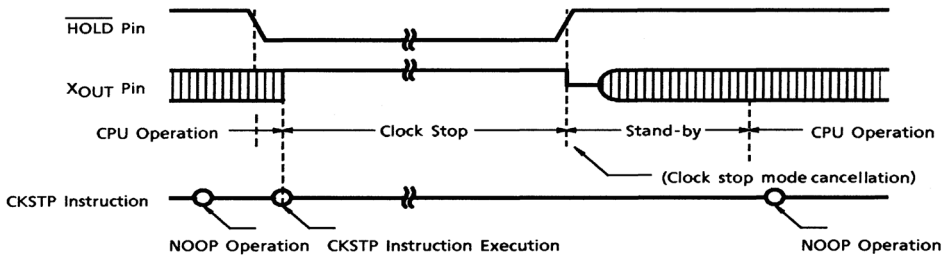
In MODE-0, the clock stop mode is cancelled by changing the "H" level of the $\overline{\text{HOLD}}$ pin or the input status of I/O port (P1-0 to 3) specified in the input port.

2) MODE-1

In MODE-1, the clock stop mode is cancelled by changing the $\overline{\text{HOLD}}$ pin or the input status of I/O port (P1-0 to 3) specified in the input port.

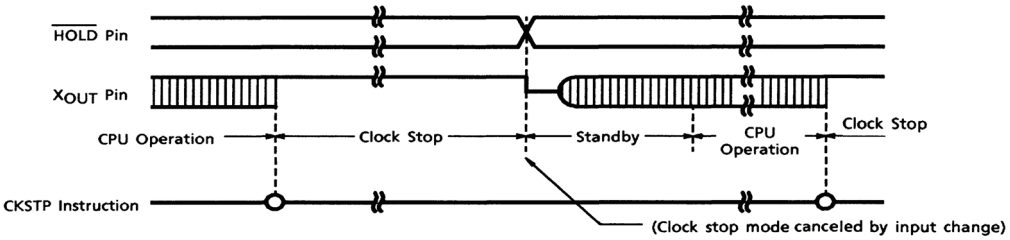
(3) Clock stop mode timing

1) MODE-0



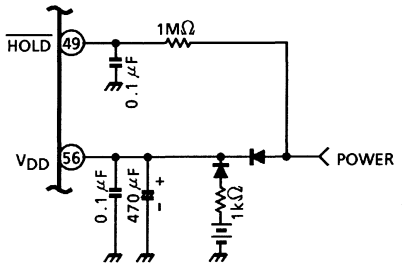
(The clock stop mode is assumed when the CKSTP is executed during the "L" level of the $\overline{\text{HOLD}}$ input.)

2) MODE-1

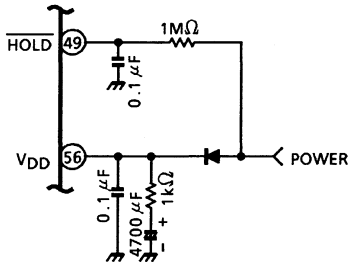


(The clock stop mode is assumed whenever the CKSTP instruction is executed.)

(4) Circuit example (MODE-0)



Example of a batterry back-up circuit



Example of a capacitor back-up circuit

2. Wait Mode

Wait mode halts the system and maintains, with reduced current consumption, the internal state of the system immediately prior to halting. Two wait modes are available: "soft wait" and "hard wait". When the WAIT instruction is executed, execution halts at the address of the WAIT instruction. Therefore, when wait mode is released, execution starts again from the next instruction without delaying for the standby time. The wait mode halts system operations, and maintains the internal status immediately prior to halt to reduce current consumption. Two wait modes are available; the SOFT WAIT mode and the HARD WAIT mode. When the WAIT instruction is executed, execution halts at the address of the WAIT instruction. The next address is executed immediately after the wait mode is cancelled without entering a stand-by status.

(1) Soft wait mode

Executing the WAIT instruction with the operand [P = 0H] stops only the CPU inside the device. In this mode, the crystal oscillator, display circuit, and other circuitry continue to operate normally. Using the soft wait mode in the program for clock functions reduces the current consumed during clock operation.

Note 18: The current consumption depends on the program.

(2) Hard wait mode

Executing the WAIT instruction with the operand [P = 1H] stops all operation other than the crystal oscillator. This reduces current consumption still further than the soft wait mode. In this state, the CPU and display circuits are halted, and the LCD display output pins are all automatically fixed at the low level. (15 μA typ. at V_{DD} = 3 V)

(3) Setting wait mode

Executing the WAIT instruction always sets wait mode.

Note 19: While The PLL OFF status is assumed during the hard wait mode, this status is not assumed during the soft wait mode. Before setting a soft wait, turn the PLL off by software.

(4) Wait mode cancellation conditions

The wait mode is cancelled when the following conditions are fulfilled:

1) When the input status of the $\overline{\text{HOLD}}$ pin changes.
2) When a high level is input to a key input pin (K0 to K3)

(Note 20: depends on the key input mode)

3) When the 2 Hz timer flip-flop is set to "1". (Only with the soft wait mode)
4) When the input state of an I/O-1 port (P1-0 to P1-3) set to an input port changes

3. $\overline{\text{HOLD}}$ Input Port

	Y1	Y2	Y4	Y8
ϕK1B	$\overline{\text{HOLD}}$	1	1	1

The $\overline{\text{HOLD}}$ pin can be used as an input port. Executing the IN1 instruction with the operand [C_N = BH] loads the data input from this bit into the data memory.

It is necessary to access this port prior to the execution of the CKSTP instruction in order to set the clock stop mode. Bear in mind that the clock stop mode will not be activated if the CKSTP instruction is executed without this port being accessed.

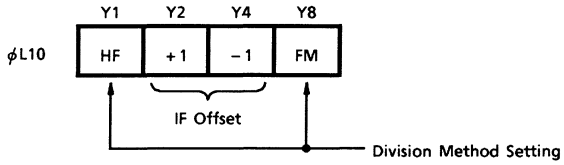
Programmable Counter

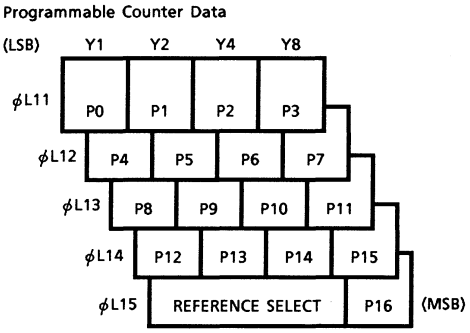
The programmable counter consists of a two-modulus prescaller, a 4-bit + 13-bit programmable counter and a port to control these elements.

The programmable counters can be turned on and off by the contents of the reference ports.

1. Programmable Counter Control Ports

These ports control the divisor, division method, and the IF correction (IF offset) for the FM band.





.The division method and power control of prescaller are accessed with the OUT1 instruction with the operand [C_N = 0H].

The division frequency setting is accessed with the OUT1 instruction with the operand [C_N = 1H to 5H], and programmable counter data is set by setting the data to the port. All data between P0 to P16 is updated when P16 is set. It is therefore necessary to access P16 even when updating only certain items of data and to perform setting as the final process. It should be noticed that the reference frequency is set at the same time.

2. Setting Division Method

The pulse swallow method or direct method are selected with the HF and FM bits.

There are four methods as shown below. Select the appropriate method in accordance with the frequency band used.

Mode	HF	FM	Division Method	Example of Reception Band	Operating Frequency Range	Input Pin	Divisor (Note 20)
LF	0	0	Direct division method	MW/LW	0.5~12 MHz	AM_{IN}	n
HF	1	0	(1/15 or 1/16) Pulse swallow method	SW	1.0~45 MHz		
FM	0	1		FM	40~130 MHz	FM_{IN}	
VHF	1	1	1/2 × (1/15 or 1/16) Pulse swallow method	VHF	50~230 MHz		2n

Note 21: n indicates the programmed divisor.

3. IF Correction Function for FM Band

When the pulse swallow method is selected, the ΔIF ± 1 ports allow the actual divisor to be varied by ±1 without changing the programmed divisor. This can be used for IF offset in FM.

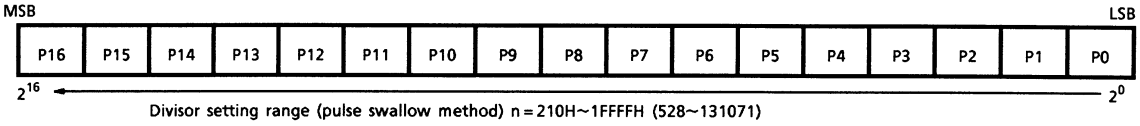
When the direct division method is selected, the IF offset function is not operated.

ΔIF + 1	ΔIF – 1	Divisor (at FM_H)	Divisor (at FM_L, HF)
0	0	2·n	n
0	1	2·(n – 1)	n – 1
1	0	2·(n + 1)	n + 1
1	1	Prohibited	Prohibited

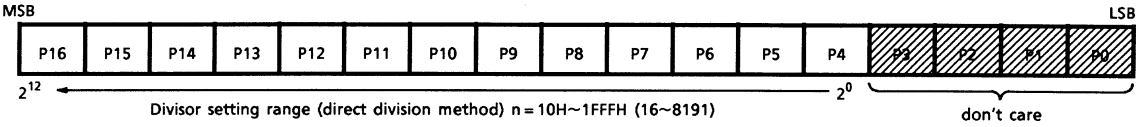
4. Setting Divisor

The divisor of the programmable counter is set in bits P0 to P16 in binary.

- Pulse swallow method (17 bits)



- Direct division method (13 bits)



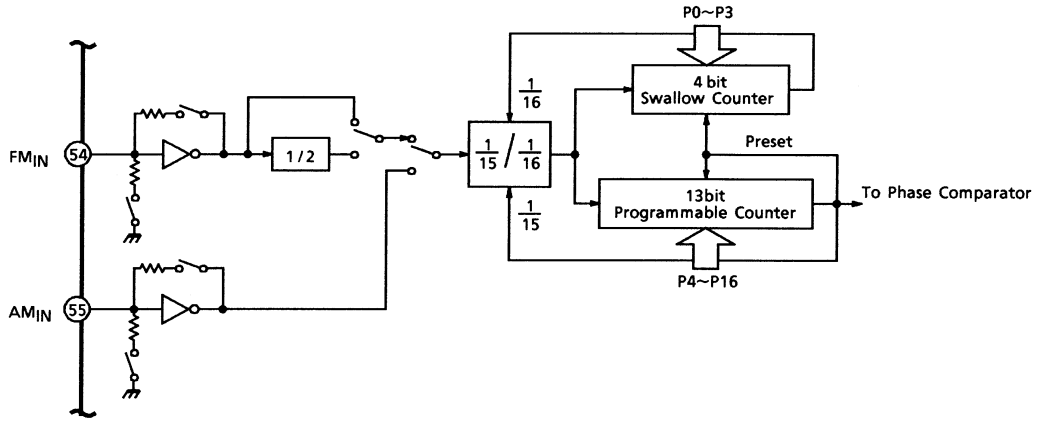
Note 22: In direct dividing mode, Pϕ to P3 (ϕL11) data is ineffective, and then the P4 port becomes LSB.

Note 23: In VHF mode, the divisor becomes double the programmed divisor.

5. Programmable Counter Circuit Structure

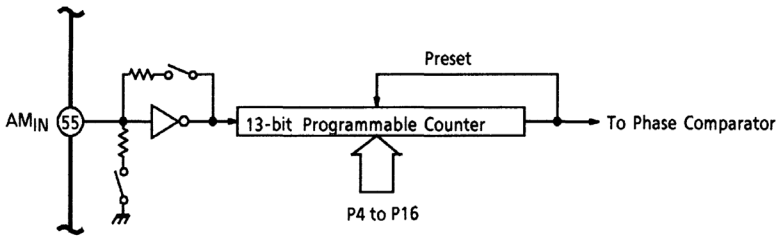
- Pulse swallow method circuit structure

This circuit consists of a 1/15 or 1/16 two-modulus prescaller, 4-bit swallow counter and 13-bit binary programmable counter. A 1/2 frequency divider is added to the front stage of the prescaller in the VHF mode.



- Direct division method circuit structure

  The prescaller is not required if this is selected, and instead, the13-bit programmable counter is used.



Note 24: The FM_{IN} and AM_{IN} pins incorporate amplifiers. Connecting a capacitor permits low-amplitude operation. The input pins non-selected by the division method are pulled down. In PLL off mode (set by the reference port), the inputs are also pulled down.

Reference Frequency Divider

The reference frequency divider divides the frequency of the external 75-kHz crystal oscillator to generate seven types of PLL reference frequency signals: 1 kHz, 3 kHz, 3.125 kHz, 5 kHz, 6.25 kHz, 12.5 kHz, and 25 kHz. These frequency signals are selected by the reference port data.

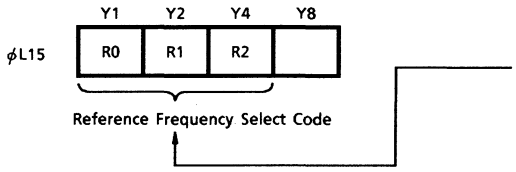
The selected signal is supplied as the reference frequency for the phase comparator, as shown below.

The PLL is turned on or off by the reference port setting.

1. Reference Port

The reference port is an internal port used to select the reference frequency signal (from the seven frequencies). This port is accessed by the OUT1 instruction with the operand [C_N = 5H] (ϕL15). When the contents of the reference port are all "1", the programmable counter, IF counter, and reference counter are halted, and the PLL is turned off.

When the reference port is set, the frequency division data of the programmable counter are updated. Therefore, it is necessary to set the frequency division data of the programmable counter prior to setting reference port.



R2	R1	R0	/	REFERENCE FREQUENCY
0	0	0	0	1kHz
0	0	1	1	3kHz
0	1	0	2	3.125kHz
0	1	1	3	5kHz
1	0	0	4	6.25kHz
1	0	1	5	12.5kHz
1	1	0	6	25kHz
1	1	1	7	PLL OFF MODE

Phase Comparator and Lock Detection Port

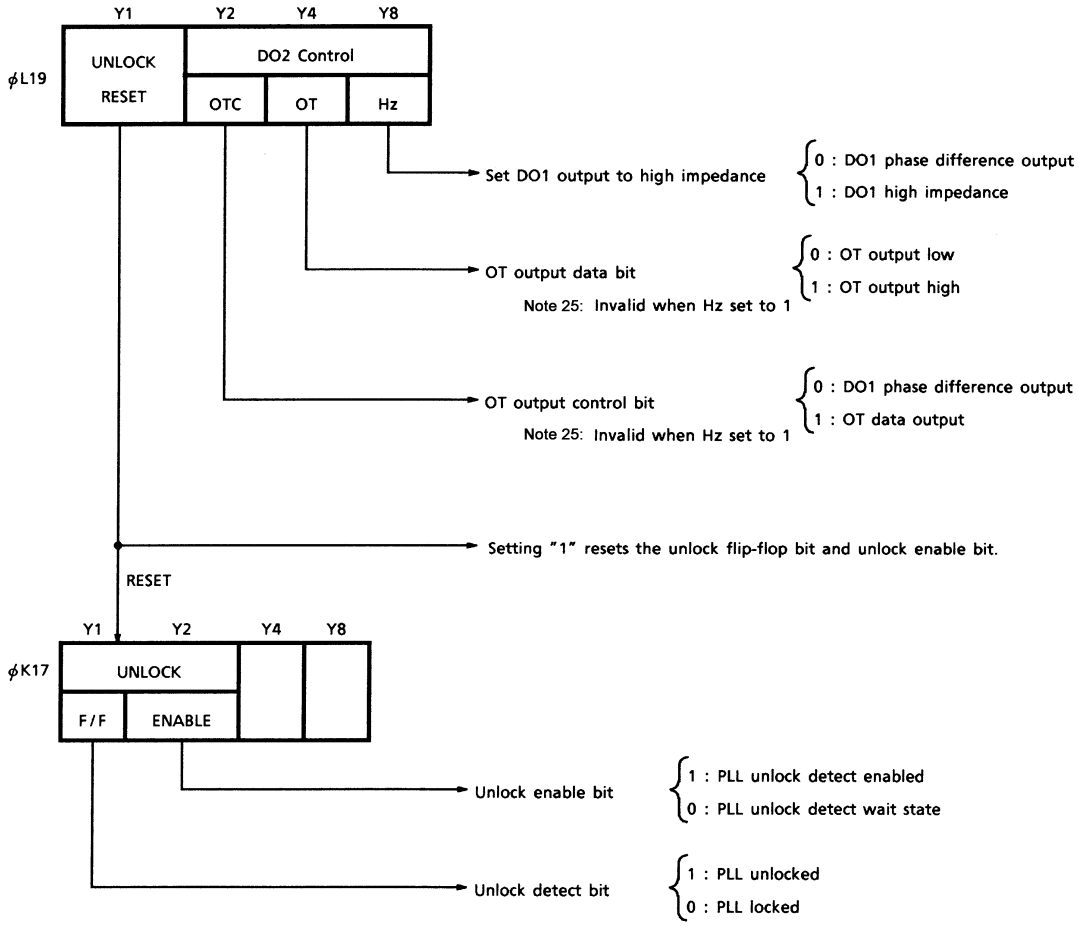
The phase comparator compares the reference frequency signal supplied by the reference frequency divider with the divided signal output by the programmable counter, and outputs the phase difference. The output of the phase comparator is used to control the voltage control oscillator (VCO) via the low pass filter in order to eliminate the frequency and phase difference between the two signals.

Data is output from the phase comparator to the tristate buffered DO1 and DO2 pins in parallel. This enables the optimal filter constants to be designed for both FM and AM bands.

Also the DO1 pin can be set for general-purpose output by the DO1 control port. The DO1 pin can be set to high impedance. By using the DO1 and DO2 pins, PLL loop characteristics, such as the lockup time, can be improved.

The lock detection port can be used to detect the PLL lock state.

1. DO2 Control Port and Unlock Detection Port



The OTC, OT, and Hz control bits of the DO1 control port set the DO1 output pin as a general-purpose output port, and control whether DO1 goes to high impedance instead of outputting the phase difference.

Set these bits to the required values by program.

When the phase is shifted approximately 180 degree, the unlock flip-flop bit detects the phase difference between the divided output of the programmable counter and the reference frequency. If the phase difference does not match, that is, if the PLL is unlocked, the unlock flip-flop is set. Also, setting the unlock reset bit to "1" resets the unlock flip-flop.

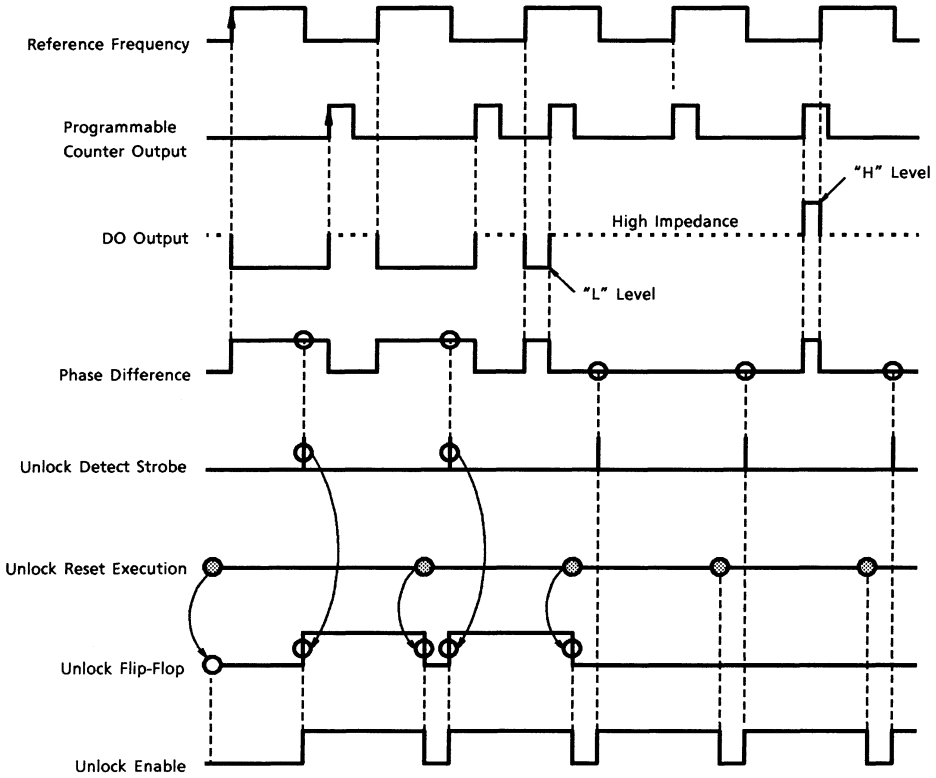
To detect the phase difference during the reference voltage period, reset the unlock flip-flop, then access the unlock flip-flop after waiting for a time longer than the reference frequency period. An enable bit is supplied for this purpose. After confirming that the unlock enable bit is set to "1", access the unlock flip-flop.

Setting the unlock reset bit to "1" resets the unlock enable bit.

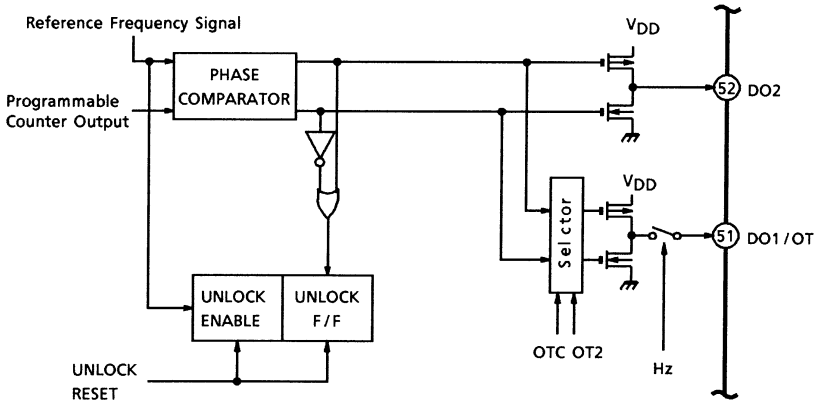
Use the OUT1 and IN1 instructions with the operand [C_N = 7 or 9H] to control these ports and load data.

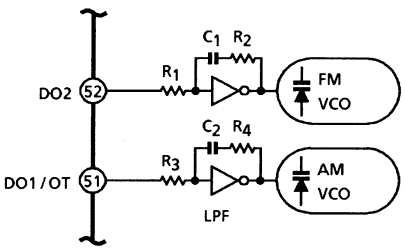
Note 26: When the PLL is off, the DO output is set to high impedance. However, when DO1 is set as an output port (OT output), the data is output from the port without change.

2. Phase Comparator and Unlock Port Timing

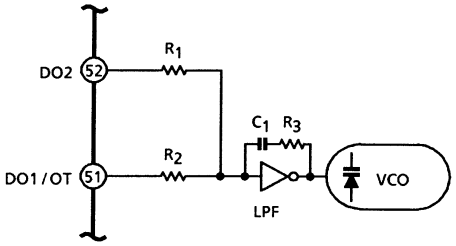


3. Phase Comparator, Unlock Port Circuit Structure

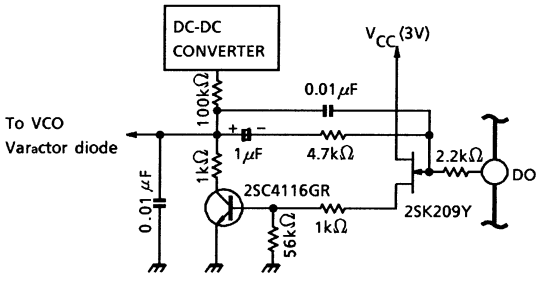




When setting different filter constants for each band



When using the same low pass filter for both bands (set DO1 to high impedance to switch the filter constant)



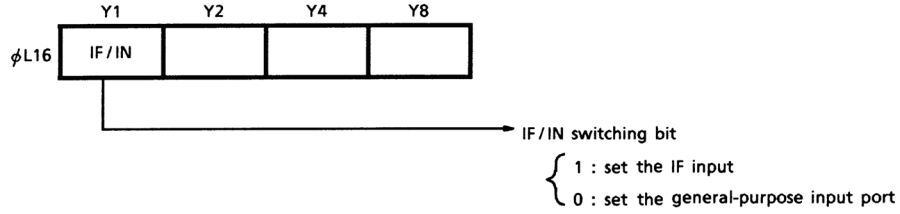
Example of an active low pass filter circuit (For reference)

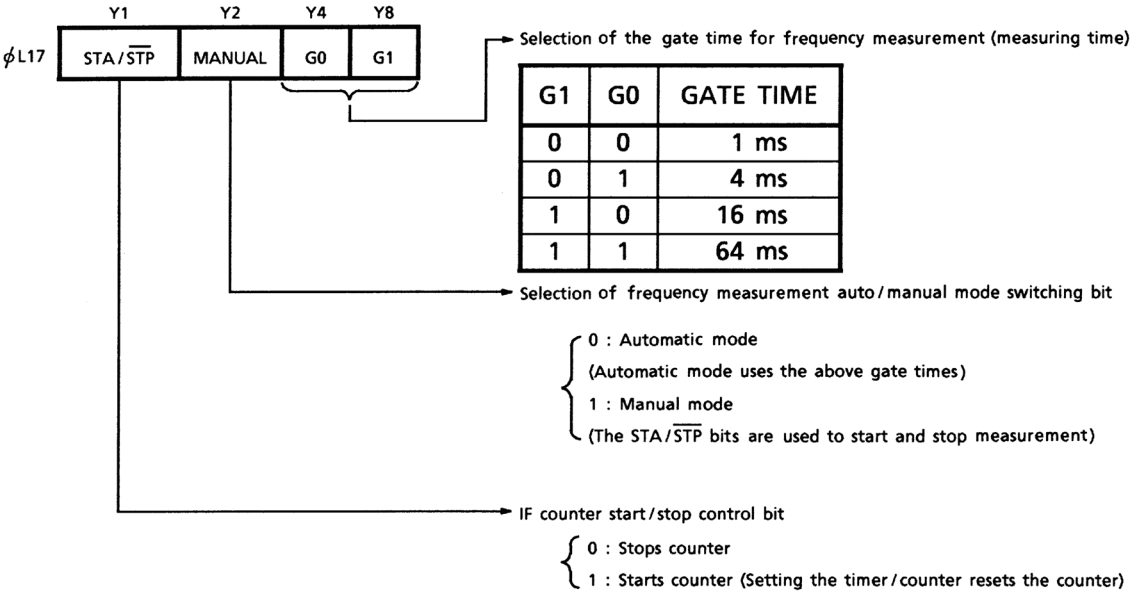
Note 27: The filter circuits shown in the above figures are for reference purpose only. The actual circuit should be investigated and designed conforming to the system band construction and the required characteristics.

IF Counter

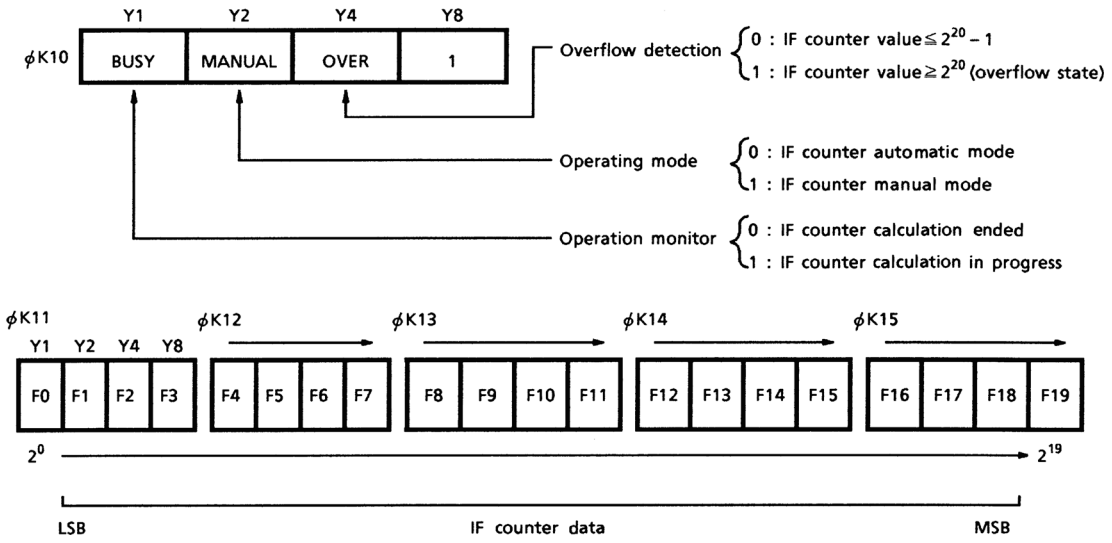
The IF counter is 20-bit general-purpose IF counter that calculates FM and AM intermediate frequencies (IF) during auto-tuning and can be used for detecting auto-stop signals, etc. The IF counter block consists of a 20-bit binary counter and a control port.

1. IF Counter Control Port and Data Port





G1	G0	GATE TIME
0	0	1 ms
0	1	4 ms
1	0	16 ms
1	1	64 ms



Note 28: When the PLL is off, the IF counter is disabled.

(1) IF counter auto mode (frequency measuring)

To use the IF counter auto mode, use the IF/$\overline{\text{IN}}$ switching bit to set the IF pin to IF input.

Set the gate time based on the IF input frequency band. Set the MANUAL bit to "0" and the STA/$\overline{\text{STP}}$ bit to "1" to start the IF counter.

As a result, the clock for the 20-bit binary counter is input from the IF pin for the specified gate time. The IF counter counts the number of input pulses. To determine when the IF counter has finished counting, check the BUSY bit. When the count equals or exceeds 2^{20} input pulses, the OVER bit is set to "1".

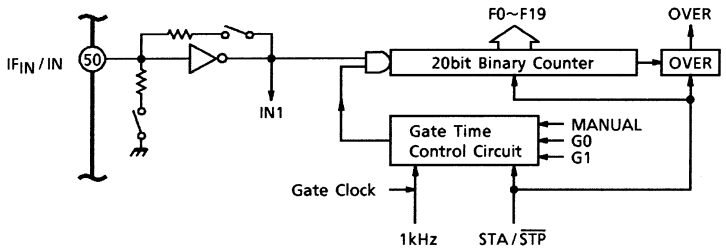
To measure the frequency input to the IF input pin, load the F0 to F19 IF data when the BUSY and OVER bits are both "0".

(2) IF counter manual mode (frequency measuring)

The manual mode is used to measure the frequency by controlling the gate time with an internal time base (e.g., 10 Hz).

Perform the same IF counter input settings as for auto mode, and set the G0 and G1 bits to other than "1". Set the MANUAL bit to "1" and the STA/$\overline{\text{STP}}$ bit to "1" to start the count. Setting the STA/$\overline{\text{STP}}$ bit to "0" terminates the count and loads the data in binary format.

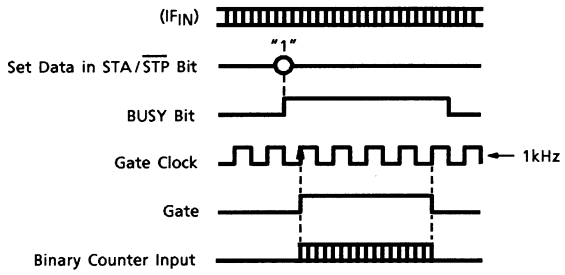
2. IF Counter Circuit Structure



The IF counter block consists of an input amplifier, a gate timer control circuit, and a 20-bit binary counter.

When the PLL is turned off, the IF counter is off. However, the block can still operate when set as a timer/counter.

Note 29: The IF_{IN1} pins incorporate amplifiers. Connecting the pins via a capacitor permits low-amplitude operation.



IF Counter Auto Mode

LCD Driver

The LCD driver has a 1/3 duty and 1/2 bias drive (frame frequency is 83 Hz).

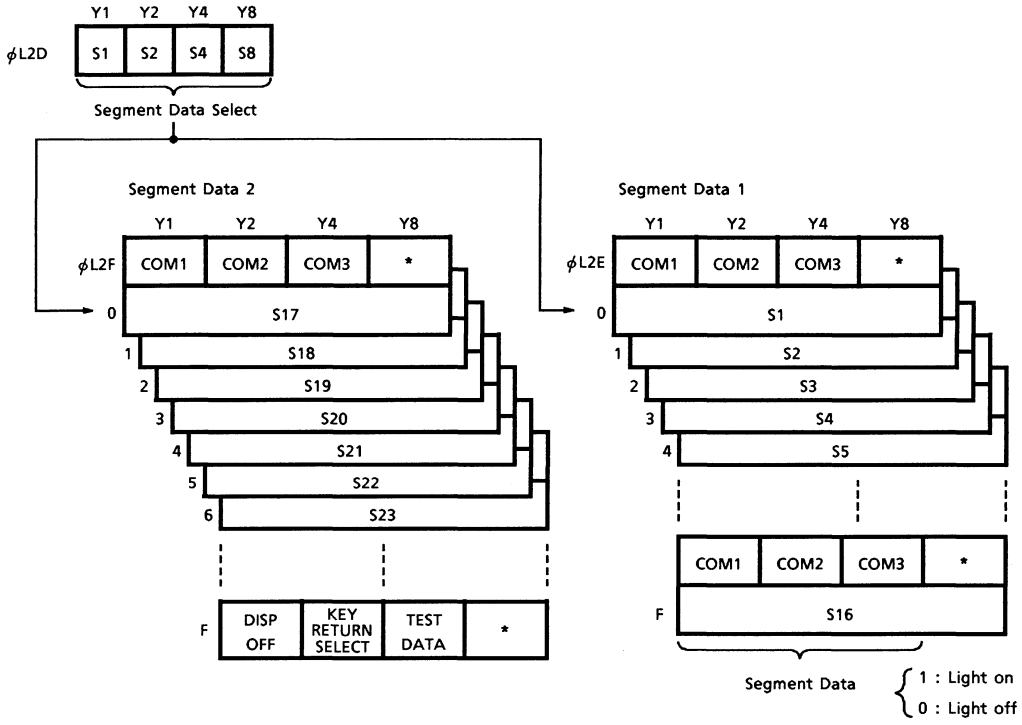
The common outputs are at three voltages: V_{LCD}, $V_{LCD}/2V_{EE}$, and GND. The segment outputs are at two voltages: V_{LCD} and GND.

The combination of three common outputs and 23 segment outputs enables the LCD driver to drive a maximum of 69 segments.

LCD driver segment output pins S16 to S23 are also used for the key return timing signals for loading key matrix data.

The LCD driver incorporates a constant voltage circuit (V_{EE} = 1.5 V) and voltage doubler circuit (V_{LCD} = 3.0 V) for the display. This maintains an even LCD contrast regardless of fluctuations in the supply voltage.

1. LCD Driver Port



*: Don't care

Note 30: The segment data controls whether or not the segments corresponding to the common and segment outputs are lit.

Note 31: The DISP OFF bit is set to "1" at a system reset and at cancellation of the clock stop mode.

The LCD driver control ports consist of a segment data selection port and segment data ports. These ports are accessed by the OUT2 instruction with the operand [C_N = DH to FH].

Set the LCD driver segment data using the segment data ports (ϕL2E, ϕL2F). Set the segment data port to "0" to turn the LCD display off and set "1" to turn the LCD display on. When FH is specified for the segment data select port, the DISP OFF and KEY RETURN SELECT bits are selected as segment-2 data port (ϕL2FF). The DISP OFF bit can turn the whole LCD display off without setting segment data.

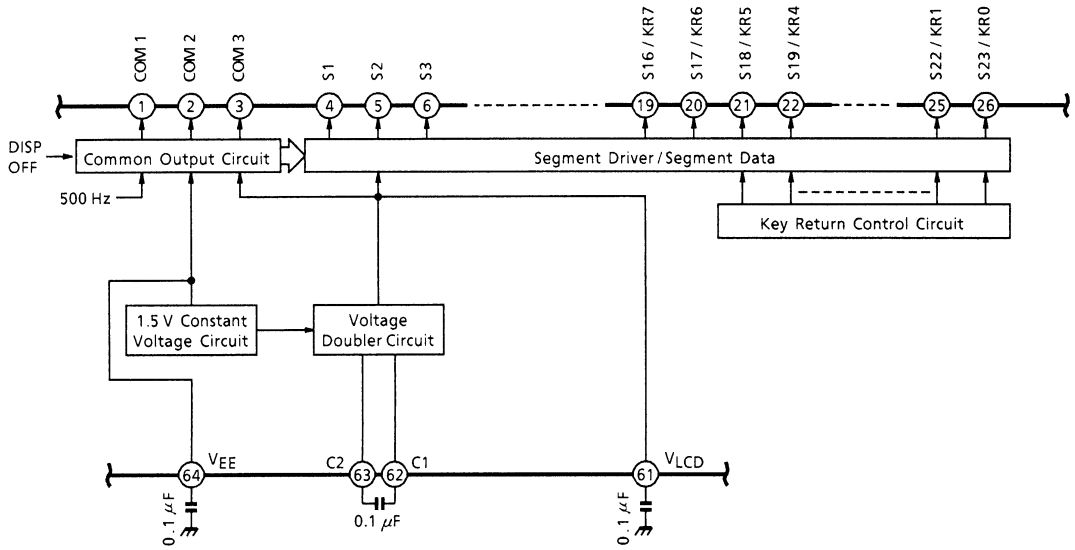
Setting this bit to "1" outputs the de-selected waveform from the common outputs and turns off the entire LCD display. The segment contents are preserved. Setting the DISP OFF bit back to "0" displays the previous LCD screen.

Segment data can be rewritten during DISP OFF. After a reset, and after CKSTP execution, the DISP OFF bit is set to "1".

The KEY RETURN SELECT bit allows an external power supply to be used. This is useful for changing the LCD drive voltage.

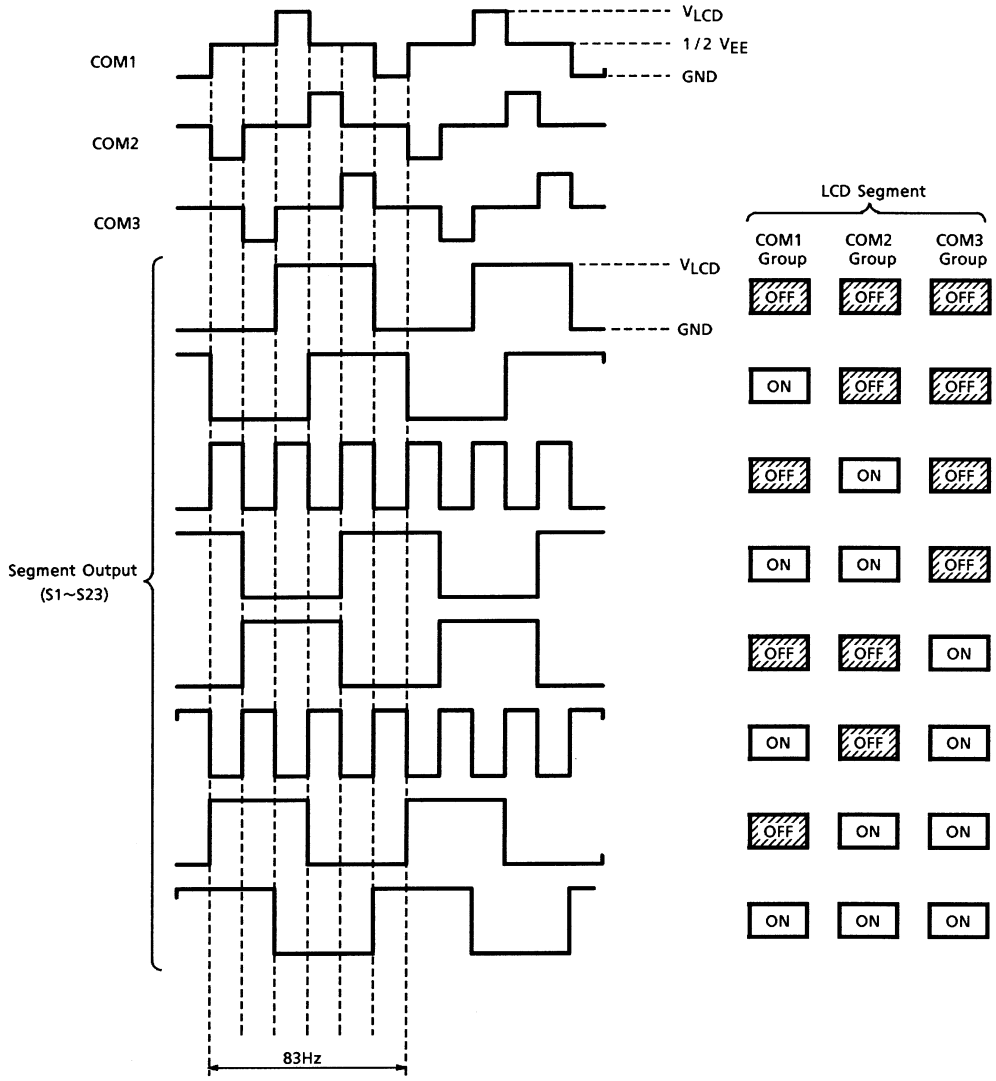
The data are set according to the segment data select port (ϕL2D). Segment output pins S16 toS23 are also used for the key return timing signals for loading key matrix data. At the timing for loading the key matrix data, the segment output is set to the GND level.

2. LCD Driver Circuit Structure



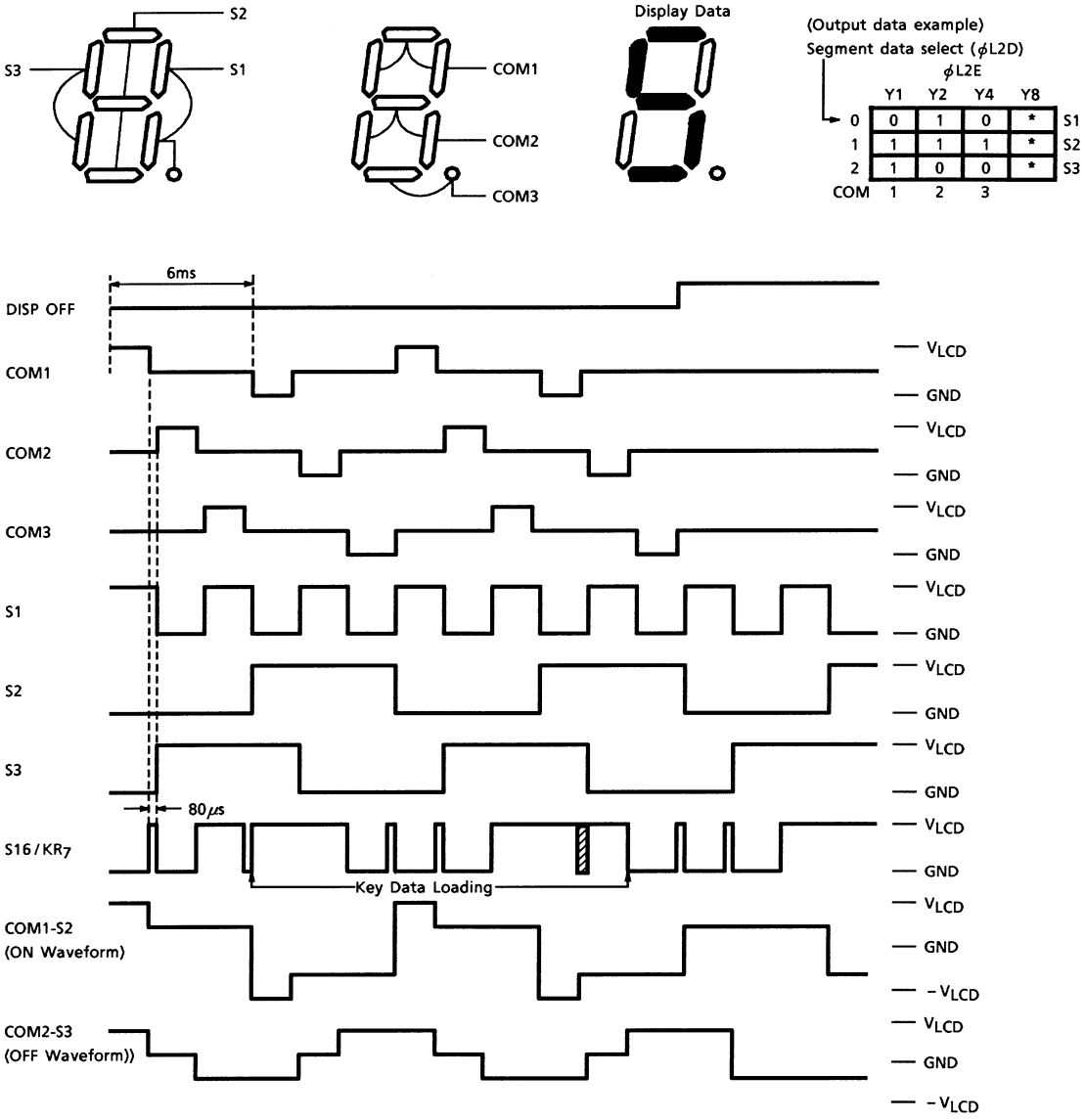
3. LCD Driver Timing Chart

The following chart shows the timing for the COM1 to COM3 output waveforms and the eight types of segment output waveform.



4. Example of Timing Chart for LCD Driver Output Data and Loading Key Data

The following chart shows the output waveform timing and key return data loading timing when the common and segment outputs are allocated, as shown below.



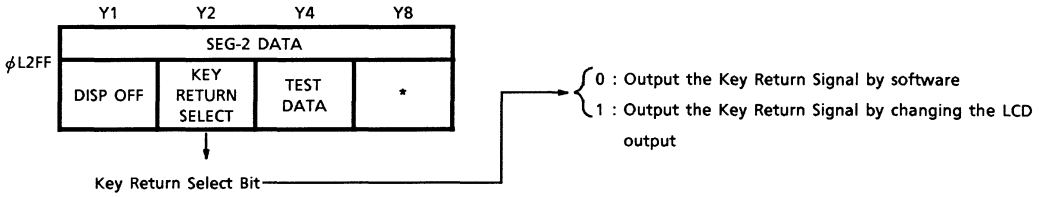
The voltages output in the LCD driver waveform are V_{LCD}, GND, and an intermediate voltage halfway between the two. Pins S16 to S23 output the key return signals at the timing for switching between these levels. During key return data loading, the segment outputs are at the V_{LCD} level for 80 μs.

Note 32: At CKSTP instruction execution or at a system reset, the common and segment pins go to the low level.

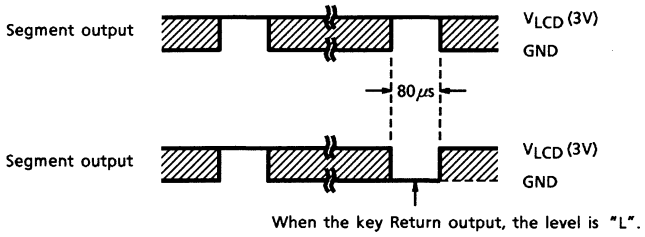
Key Input, Key Scan Timing

The following are the two basic methods of loading key data.
Select the appropriate method for the system.

1. Key Control Port and Key Scan Data



When "1" is set to the key Return Select bit, the output timing of the segment output becomes as shown below.



When "0"is set to the key Return Select bit, the key Return signal is not output.

Key Scan Digit Port

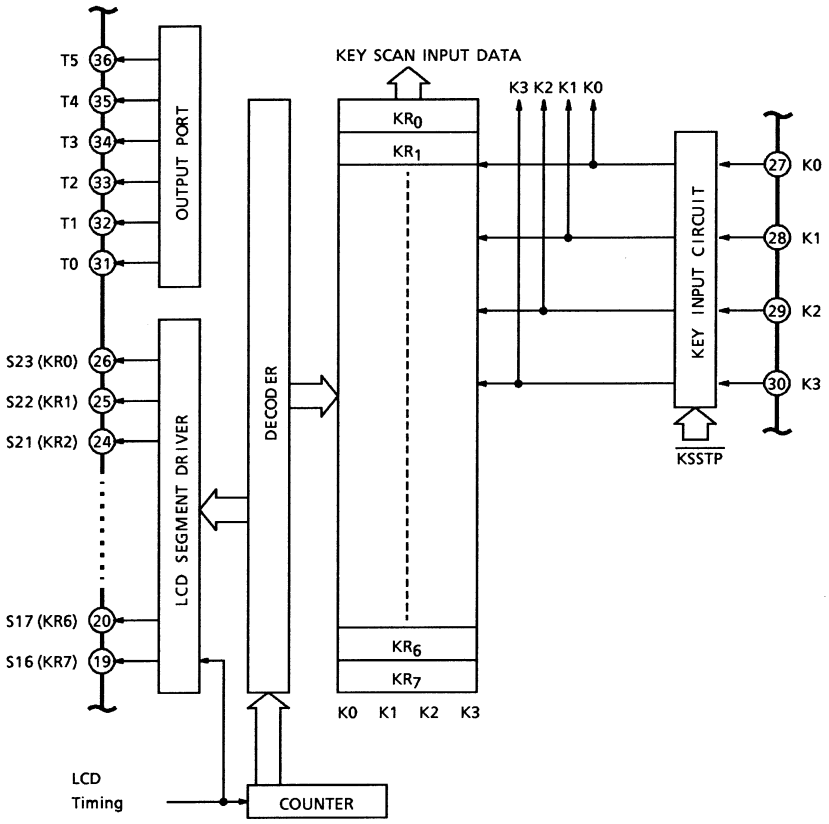
	Y1	Y2	Y3	Y4
ϕK27	KEY SCAN DIGIT			
	KS0	KS1	KS2	1

Key Scan Input Data Port

	Y1	Y2	Y3	Y4
ϕK28	KEY SCAN INPUT DATA-0			
	KS00	KS01	KS02	KS03
ϕK29	KEY SCAN INPUT DATA-1			
	KS10	KS11	KS12	KS13
ϕK2A	KEY SCAN INPUT DATA-2			
	KS20	KS21	KS22	KS23
ϕK2B	KEY SCAN INPUT DATA-3			
	KS30	KS31	KS32	KS33
ϕK2C	KEY SCAN INPUT DATA-4			
	KS40	KS41	KS42	KS43
ϕK2D	KEY SCAN INPUT DATA-5			
	KS50	KS51	KS52	KS53
ϕK2E	KEY SCAN INPUT DATA-6			
	KS60	KS61	KS62	KS63
ϕK2F	KEY SCAN INPUT DATA-07			
	KS70	KS71	KS72	KS73

The key Return Select bit is the bit used to set the loading key method.
The data is loaded by the digit timing of the key Return Signals from the key scan digit Port.
The key data by key scan is input to the key scan input data port. By accessing this port, the key data is loaded into the data memory.

2. Key Scan Circuit Structure



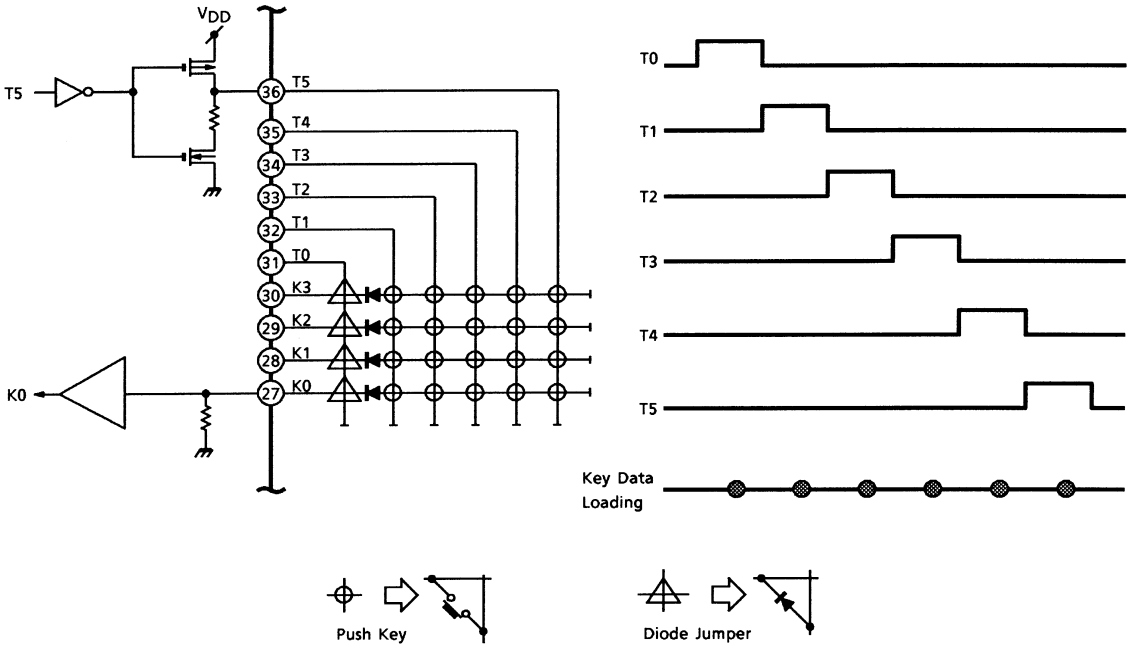
The key input block in the key scan circuit consists of the key input circuit and latch circuit used to load key data.

The key return timing output block consists of the LCD segment driver, decoder and counter blocks.

3. Key Matrix Structure

The key matrix can have one of the following two structures.

(1) Key data loading by software



When loading key data by software, use a key matrix with the above structure. For this method, set high to the key timing output port data (ϕL28, ϕL29) for the key line to be loaded. Then to determine which keys are pressed, load the key input port (ϕK26) data to memory. At this timing, set the other key timing output ports to low. If the corresponding key is pressed, the key input port data are "1"; if not pressed, "0". This structure allows up to 24 (4 × (6)) keys to be used. The key data can be loaded at high speed. Also, as the structure has a high resistance in the N channel FETs of pins T0~T5, there is no need to use a diode to prevent reverse current flow caused by, for example, multiple keys being pressed.

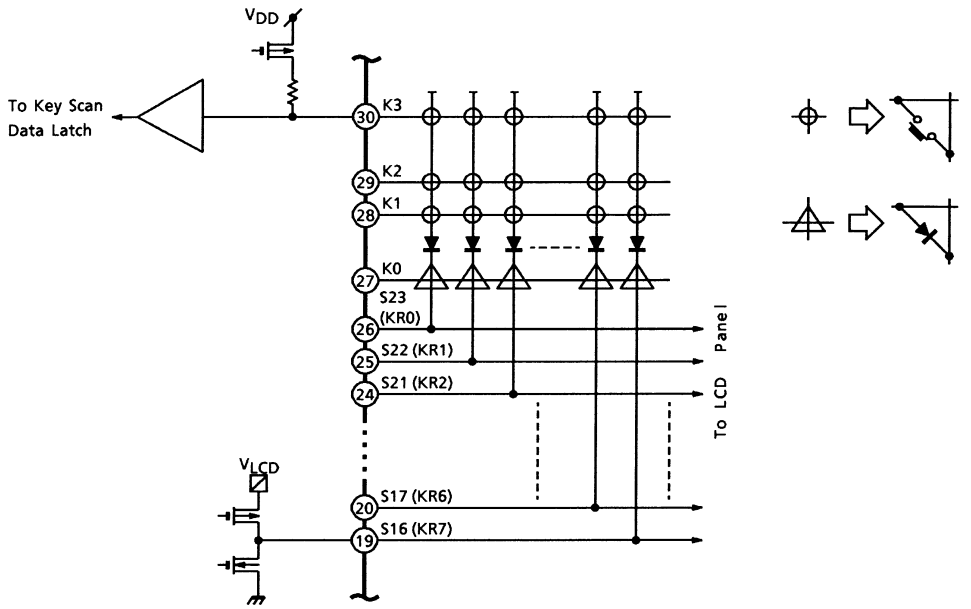
When loading key data by software, set to "0" to the key return select bit.

Note 33: In case of structuring a diode jumper, the key input voltage is input/low voltage of VF (≃ 0.6 V) voltage of diode. This structure requires the diode for diode jumper malfunction prevention to structure of double push of a key, as shown above.

The diode is not required when no diode jumper is included. Therefore, key input threshold level is set to low.

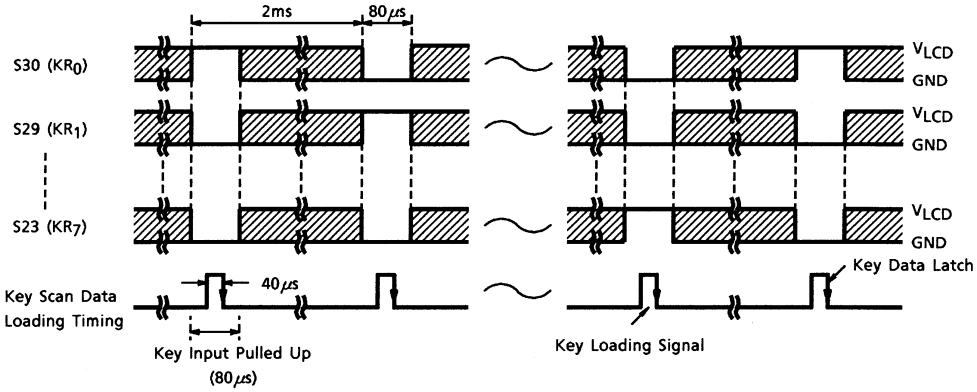
When executing a wait instruction (in WAIT mode) in this mode structure, applying a high level to a key input pin releases WAIT mode and restarts the CPU.

(2) Key data loading by LCD segment output (hardware scan)



Note 34: A key matrix with 4 × 8 = 32 structure can be created.

Note 35: The same key line cannot contain both push keys and diode jumpers. Place diode jumpers on the key return signal output side.



When loading key data by LCD segment output, use a key matrix with the above structure. In this structure, diode is required to prevent reverse current flow. Care must be taken in the direction of diode and diode jumper.

The V_{LCD} and GND potential are output from a segment pin at the timing of changing LCD output.

When loading key data, segment signal to be loaded becomes to the GND potential and key input pin is pulled up to the V_{DD} potential at changing LCD output.

At this timing, if key is not pressed (or without diode jumper), V_{DD} potential is input to the key input pin; if key is pressed (or with diode jumper), one diode potential (≃ 0.6 V) from GND potential is input to the key input pin. Therefore, key input threshold level is set up high.

The input key data is latched into the key scan data port corresponding to the segment output line of loading the key. If a key is pressed, the key data is "1"; if not pressed, the key data is "0".

Loading the key data for each line requires 2 ms. The key scan data (ϕK26) is loaded to the data memory by referring the key scan action monitor.

Key Return Timing Output Ports (T0 toT5)

T0 toT5 are exclusive output ports of 6 bits with N-channel load resistors. Normally, T0 toT5 are used as output of key return timing signal for key matrix.

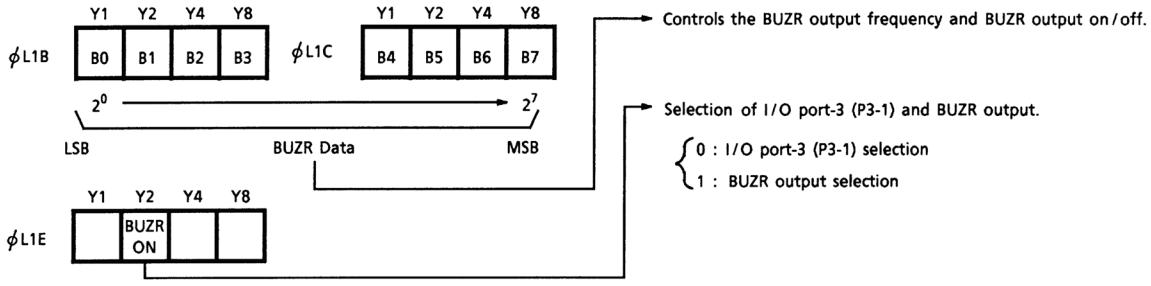
These output ports are accessed by the OUT2 instruction with the operand part [C_N = 8 or 9] (ϕL28 or ϕL29).

Note 36: During the clock stop mode (excusing CKSTP instruction), T0to T5 outputs are fixed at “L” level automatically, but the previous data is held in the contents of the ports. .

Buzzer Output (BUZR)

The buzzer output is used for the purposes such as audible alarms or confirmation beeps for key-presses or tuning scan mode. The buzzer frequency can be set as desired. 50% duty waveform is output.

1. BUZR Control Port and Data port



The BUZR output can also be used as the P3-1 I/O port. Switching the P3-1 output to BUZR output sets “1” to BUZR ON bit.

It is necessary to set of the BUZR data before setting “1” to the BUZRON bit.

When the data is set to the BUZR data port (ϕL1C), the BUZR data is transferred to the BUZR data latch, and then the BUZR frequency is changed.

The BUZR output has a frequency of 75 kHz divided by 2 × n (n = B0 toB7). The B0 to B7 setting range and frequency range is $2 \leqq n \leqq 255$. This can be expressed as a formula as shown below.

$$\frac{75\ \text{kHz}}{2 \times 2} = 18.75\ \text{kHz} \leqq f_{BUZR} \leqq \frac{75\ \text{kHz}}{2 \times 255} = 147\ \text{Hz}$$

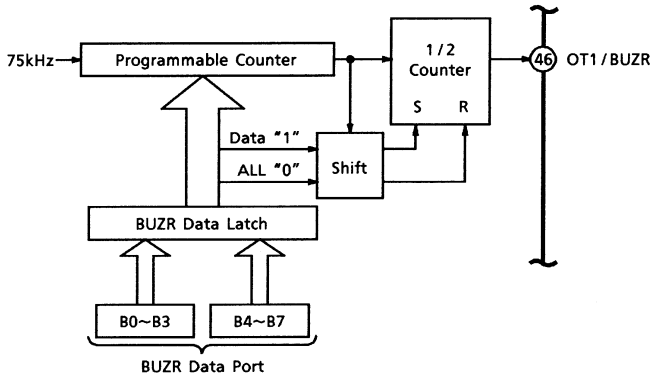
Set B0 toB7 to 1 or 0 to use the pin for OT1 output. The output states are as follows.

B7	B6	B5	B4	B3	B2	B1	B0	OT1 Output
0	0	0	0	0	0	0	0	Low level output
0	0	0	0	0	0	0	1	High level output

To set the above data, use the OUT1 instruction with the operand [C_N = BH to EH].

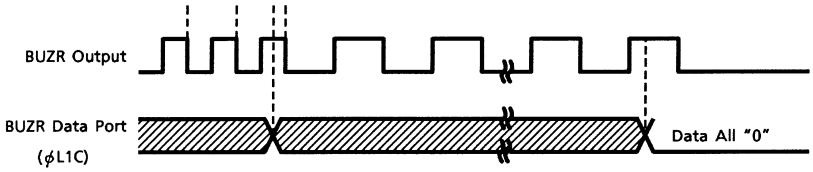
Note 37: After a system reset, the BUZR data port is reset to “0”.

2. BUZR Circuit Structure



The buzzer circuit consists of an 8-bit programmable counter, a 1/2 counter, a buzzer latch and a buzzer data port.

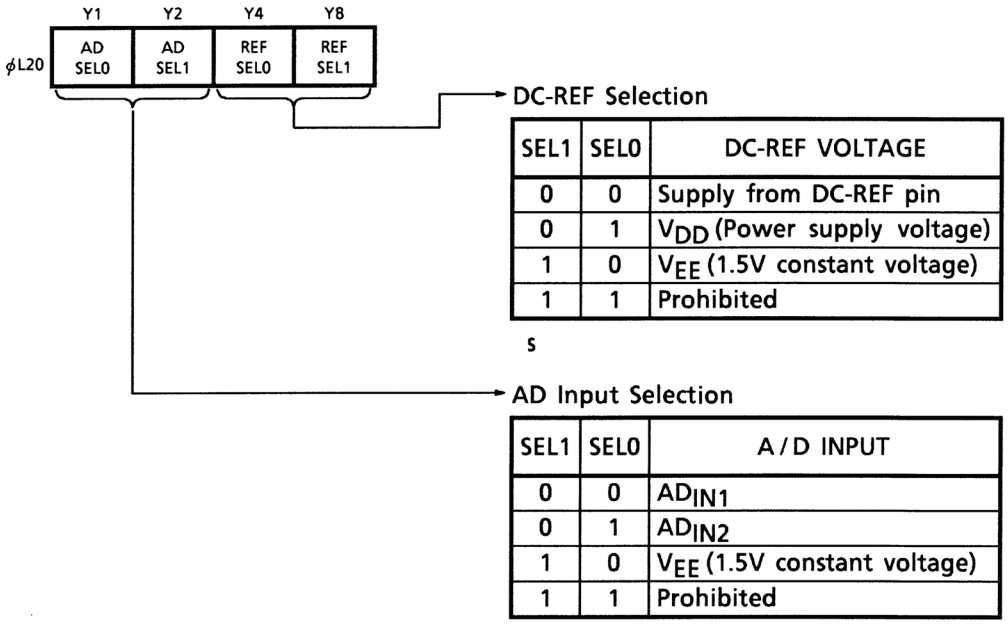
3. BUZR Output Timing (When the BUZR ON bit is set to“1”)



A/D Converter

The 2-channel 6-bit resolution A/D converter is used for measuring the strength of electric fields and the voltage of batteries.

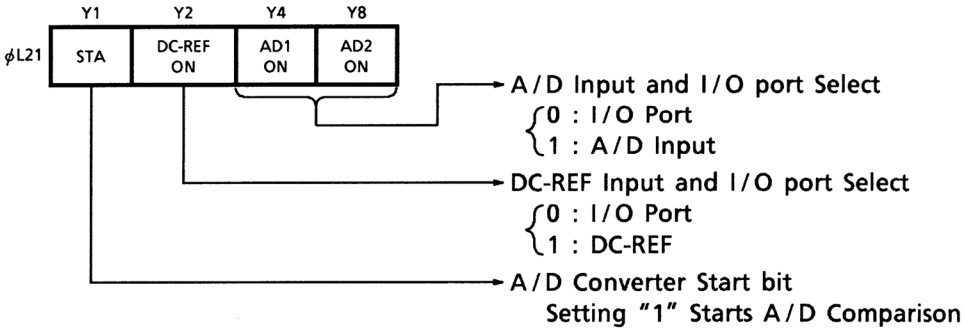
1. A/D Converter Control Port and Data Port

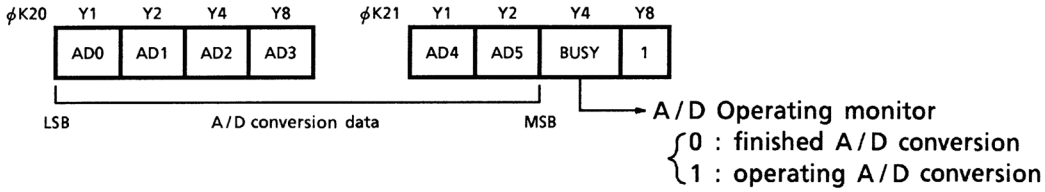


SEL1	SEL0	DC-REF VOLTAGE
0	0	Supply from DC-REF pin
0	1	V_{DD} (Power supply voltage)
1	0	V_{EE} (1.5V constant voltage)
1	1	Prohibited

S

SEL1	SEL0	A/D INPUT
0	0	AD_{IN1}
0	1	AD_{IN2}
1	0	V_{EE} (1.5V constant voltage)
1	1	Prohibited





The A/D converter has a 6-bit resolution. The reference voltage of A/D conversion can select the external voltage (DC-REF pin), supply voltage and 1.5-V constant voltage (V_{EE}). The A/D conversion input is performed by the multiplex method of 2-channel external input pin (AD_{IN1}, AD_{IN2}pin) and also switchable to 1.5-V constant voltage (V_{EE}).

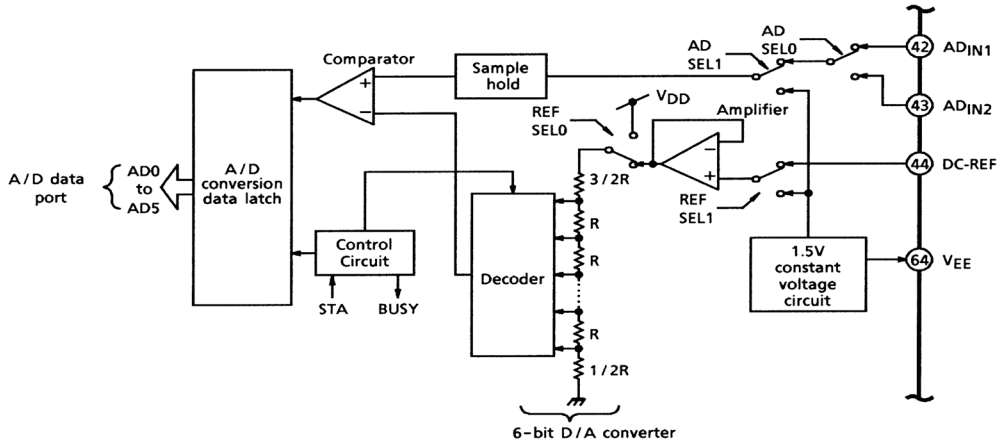
Normally field strength and volume level are measured by selecting external voltage or supply voltage as reference voltage and A/D converting the external input level.

The A/D converter can also measure battery and supply voltages. It outputs a battery signal or controls the backup mode when battery voltage or supply voltage drops.

The A/D converter performs A/D conversion whenever setting "1" to STA bit and the conversion will be completed after 7 machine cycles (280 μs). Whether A/D conversion is completed can be judged by referring to the BUSY bit. After A/D conversion is completed, the data will be loaded into the data memory.

These controls are accessed when OUT2/IN2 instruction designated to [C_N = 0H, 1H] in the operand is executed.

2. A/D Converter Circuit Configuration



The A/D converter consists of: 6 bit D/A converter, a comparator, an A/D conversion latch, a control circuit, an A/D data port and a 1.5-V constant voltage circuit (supply for the LCD driver).

The A/D converter will latch the data to A/D conversion data latch sequentially by means of the 6-bit sequential comparison method.

Note 38: The DC-REF pin incorporates an amplifier and is high impedance input.

Note 39: During A/D conversion, appropriate data is not obtained even if referring to the A/D conversion data. You must be aware that the conversion has been completed by referring to the A/D operation monitor.

Input and Output Port

1. I/O Port P1-0~P1-3 (ϕKL22), P2-0~P2-3 (ϕKL23), P3-0~P3-1 (ϕKL24)

CMOS-type 4-bit I/O port (P1-0 to P1-3, P2-0 to P2-3) and 2-bit I/O port (P3-0 to P3-1) can set input or output status to individual bit.

The I/O port is set with the contents of the I/O control data port. "0" is set in the I/O control data port bit which corresponds to the relevant port when setting the input port, and "1" is set when setting the output port.

The data input in the I/O port is loaded into the data memory by executing the IN2 instruction with the operand [C_N = 2 to 4] (ϕK22, ϕK23, ϕK24) during input port setting.

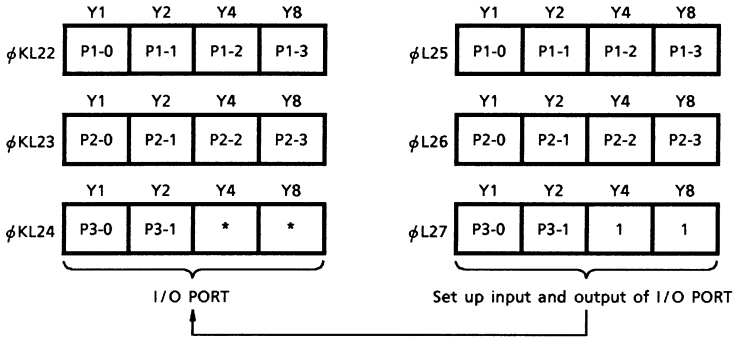
The output status of the I/O port is controlled by executing the OUT2 instruction with the operand part [C_N = 2 to 4] (ϕL22, ϕL23, ϕL24) during output port setting. The contents of the data currently output can also be loaded into the data memory by executing the IO instruction. (ϕK22, ϕK23, ϕK24)

I/O port 2and 3 are also used as A/D converter and BUZR output.
After system reset, these ports are set to I/O ports.

Note 40: I/O control port is accessed by the OUT2 instruction designated the operand part [C_N = 5~7].

Note 41: During the clock stop mode (executing CKSTP instruction), output condition of I/O port set in output mode is fixed at "L" level automatically. However, each output latch holds the data before the clock stop mode.

Note 42: At the time of changing input condition of P1-0 to P1-3 ports set to input mode, the execution of WAIT and CKSTP instructions is canceled and the operation is restarted When "1" is set to the I/O bit of MUTE control port, MUTE port is forced to "1" by the same condition.



Register Port

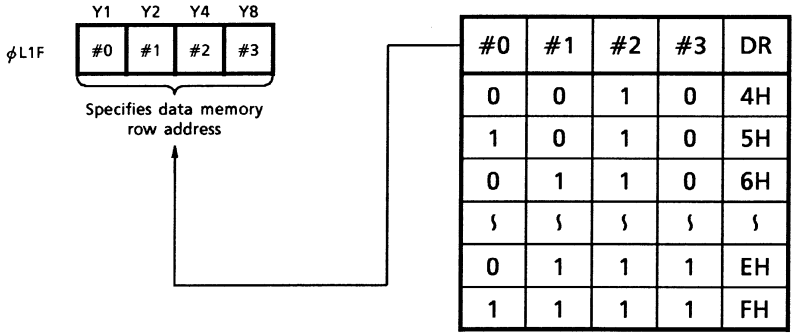
The G-register and data register mentioned in the CPU description are also used as a single internal port.

1. G-Register (ϕL1F)

This register addresses row addresses (D_R = 4H to FH) in the data memory during execution of the MVGD and MVGS instructions. This register is accessed with the OUT1 instruction with the operand [C_N = FH].

Note 43:

The contents of this register are only valid when the MVGD and MVGS instructions are executed and are ineffective when any other instruction is executed.



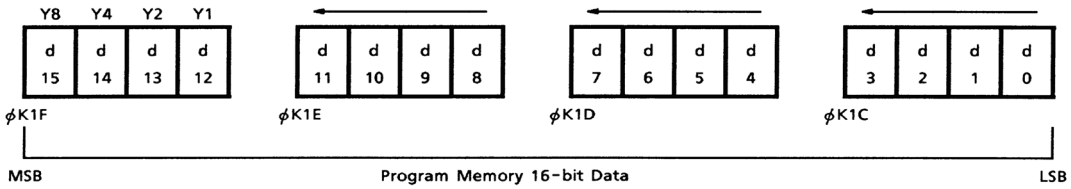
#0	#1	#2	#3	DR
0	0	1	0	4H
1	0	1	0	5H
0	1	1	0	6H
≀	≀	≀	≀	≀
0	1	1	1	EH
1	1	1	1	FH

Note 44: Setting data to 0H~FH in the G register allows all the data memory row addresses to be specified indirectly. (D_R = 0H~FH)

2. Data Register (ϕK1C to ϕK1F)

This is a 16-bit register to load the program memory data when the DAL instruction is executed. The contents of the register are loaded into the data memory in 4-bit units by the IN1 instruction with the operands [C_N = CH to FH].

This register can be used for LCD segment decoding, radio band edge data, or for factor for binary-to-BCD conversion.

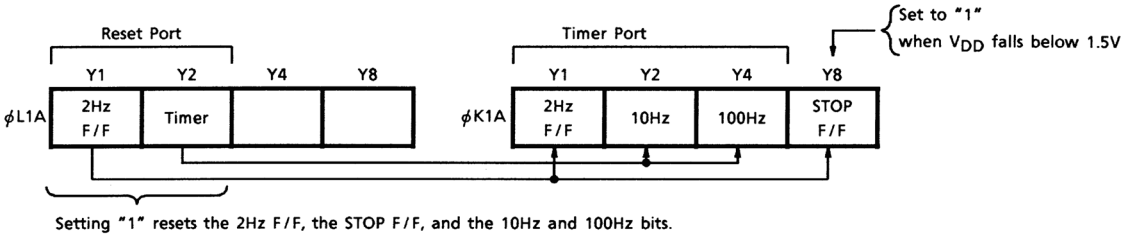


Timer and CPU Stop Function

The timer is equipped with 100-Hz, 10-Hz, and 2-Hz flip-flop bits, and used for counting clock operations and tuning scan mode.

The CPU stop function uses a voltage detector circuit to shut down the CPU when the V_{DD} voltage applied to the CPU falls below 1.5 V. This prevents CPU malfunction.

1. Timer Port and STOP Flip-Flop Bit

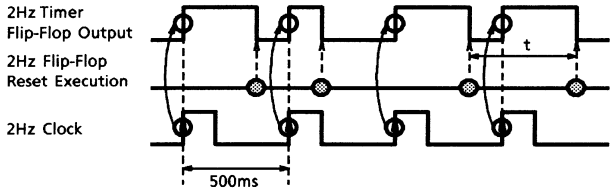


The timer ports and the STOP flip-flop bit are accessed with the OUT1/IN1 instructions with the operand [C_N = AH].

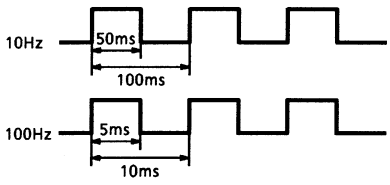
2. Timer Port Timing

The 2-Hz timer flip-flop is set by the 2 Hz-(500-ms) signal, and reset by setting the RESET port 2-Hz flip-flop to "1". This bit can normally be used for the clock count.

The 2-Hz timer flip-flop is reset only by the 2-Hz flip-flop in the RESET port. Therefore, if the flip-flop is not reset within 500 ms, the next count is missed and the correct time is not obtained.



The 10-Hz and 100-Hz timers are output to the 10-Hz and 100-Hz bits with a duty 50% of 100-ms and 10-ms cycles, respectively. Counters at 1 kHz or below are reset whenever the RESET port timer bit is set to "1"..



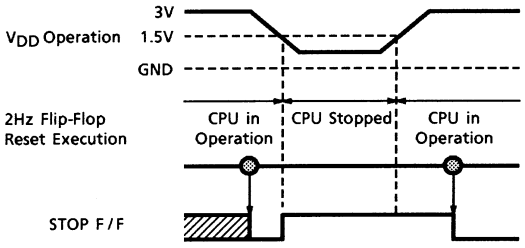
3. CPU Stop Function, STOP Flip-Flop Bit

The STOP flip-flop bit is set to "1" when the V_{DD} voltage applied to the CPU falls below 1.5 V.

This prevents CPU malfunction by shutting down the CPU. When a voltage of 1.5 V or less is applied to the V_{DD} pin, the program counter stops and instruction execution halts in the CPU.

When a voltage higher than 1.5 V is applied to the V_{DD} pin, the CPU is restarted. Since the CPU was shut down, the clock and other timings become invalid. Use the STOP flip-flop to test whether the CPU stop function is operated. Perform initialization or clock correction if required.

The STOP flip-flop bit is reset to "0" whenever the RESET port 2-Hz flip-flop is set to "1".



Note 45: After a system reset or execution of the CKSTP instruction, the timer port and the STOP flip-flop are reset to "0".

Note 46: If the V_{DD} voltage falls below 1.5 V when clock-stop mode is set, the CKSTP instruction cannot be executed. Be careful with the supply voltage timing when the radio is off.

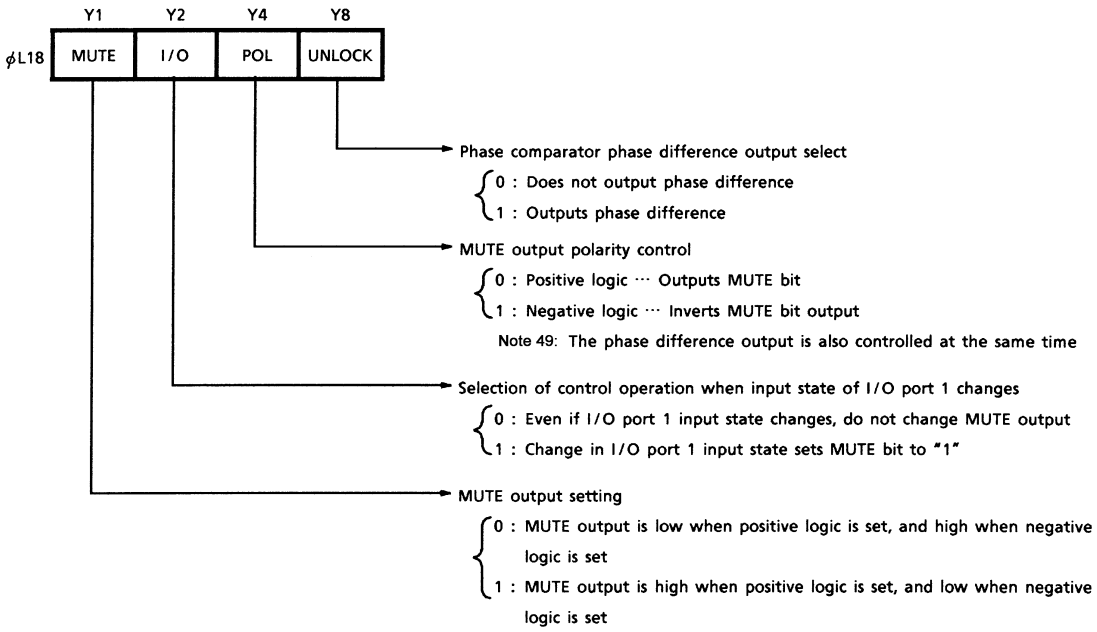
Note 47: The key scan input data immediately after restarting the CPU is undefined.

Note 48: If the internal Test port from #0 to #3 bit (ϕL1D) is set to "1", the CPU stop function is inhibited.

MUTE Output

This is a 1-bit CMOS-format output-only port for muting control.

1. MUTE Port



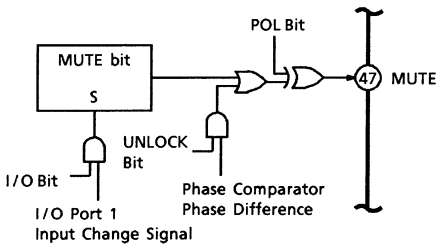
Access the MUTE port by executing the OUT1 instruction with the operand [C_N = 8H]. The MUTE output is used for muting control. At such times as switching bands using the I/O port 1 input, the MUTE bit can be set to "1".

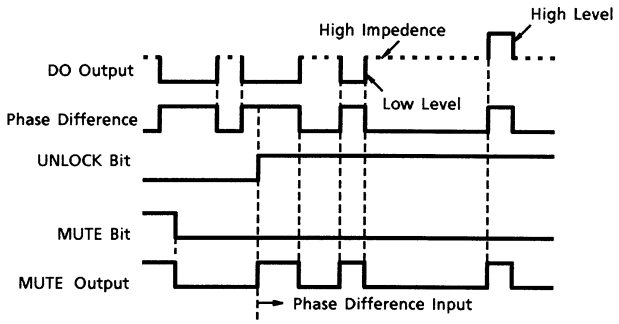
When using the I/O port 1 input to switch bands (using a slide switch, for example), this function prevents linear circuit switching noise. This control is based on I/O bit values.

The POL bit sets the MUTE output logic.

The mute output can also control muting using the phase difference output. A pulse is output to indicate when the PLL is not locked. By connecting an external low-pass filter to the MUTE output, the output can be used as a MUTE signal. Use the UNLOCK bit to perform selection.

2. MUTE Output Structure and Timing





Note 50: When POL bit = 0

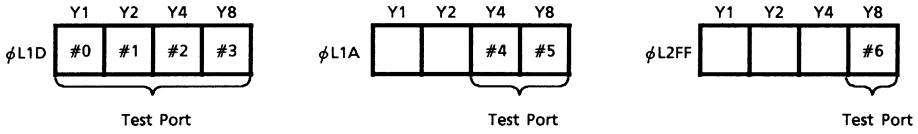
Note 51: When using the phase difference output by the phase comparator, externally connect a low-pass filter to the MUTE output.

Test Ports

These are internal ports for testing the device functions. Access the ports by executing the OUT1 instruction with the operand [C_N = AH] or [C_N = DH], or the OUT2 instruction with the operands [C_N = FFH]. The ports are normally set to "0" by software.

If the data "1" is set to Test port bit from #0 to #3, the CPU stop function is inhibited . If the data "0" is set, the CPU function is operated.

In case of using supply voltage detection externally, set CPU stop function as inhibition.



Note 52: The ports are reset to "0" after a system reset.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~4.0	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	100	mW
Operating temperature	T_{opr}	−10~60	°C
Storage temperature	T_{stg}	−55~125	°C

Electrical Characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 3.0 V)

Characteristics	Symbol	Test Circuit	Test Condition		Min.	Typ.	Max.	Unit
Range of operating supply voltage	V_{DD}	—	*		1.8	3.0	3.6	V
Range of memory retention voltage	V_{HD}	—	Crystal oscillation stopped (CKSTP instruction executed) *		1.0	~	3.6	V
Operating current	I_{DD1}	—	Under normal operation, no output load FM_{IN} = 230 MHz input	V_{DD} = 3.0 V	—	7.0	12	mA
			Under normal operation, no output load FM_{IN} = 130 MHz input	V_{DD} = 3.0 V	—	6.0	10	
	I_{DD2}	—	Under CPU operation only (PLL off, display turned on)	V_{DD} = 3.0 V	—	40	80	μA
	I_{DD3}	—	Soft Wait mode (Crystal oscillator, display circuit operation, CPU stopped, PLL off)		—	25	50	
	I_{DD4}	—	Hard Wait mode (Crystal oscillator operation only)		—	15	30	
Memory retention current	I_{HD}	—	Crystal oscillation stopped (CKSTP instruction executed)		—	0.1	10	μA
Crystal oscillation frequency	f_{XT}	—	*		—	75	—	kHz
Crystal oscillation start-up time	t_{ST}	—	Crystal oscillation f_{XT} = 75 kHz		—	—	1.0	s

Note 53: For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8to 3.6 V, Ta = −10to 60°C.

Voltage Doubler Circuit

Characteristics	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Voltage doubler reference voltage	V_{EE}	—	GND reference (V_{EE})	1.3	1.5	1.7	V
Constant voltage temperature characteristics	D_V	—	GND reference (V_{EE})	—	−5	—	mV/°C
Voltage doubler boosting voltage	V_{LCD}	—	GND reference (V_{LCD})	2.6	3.0	3.4	V

Operating Frequency Ranges for Programmable Counter and IF Counter

Characteristics	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
FM_{IN} (VHF mode)	f_{VHF}	—	When V_{IN} = 0.2 V_{p-p} *	50	~	230	MHz
FM_{IN} (FM mode)	f_{FM}	—	when V_{IN} = 0.2 V_{p-p} *	40	~	130	MHz
AM_{IN} (HF mode)	f_{HL}	—	when V_{IN} = 0.2 V_{p-p} *	1	~	45	MHz
AM_{IN} (LF mode)	f_{LF}	—	when V_{IN} = 0.2 V_{p-p} *	0.5	~	12	MHz
IF_{IN}	f_{IF}	—	when V_{IN} = 0.2 V_{p-p} *	0.35	~	12	MHz
Input amplitude	V_{IN}	—	FM_{IN}, AM_{IN}, IF_{IN} input *	0.2	~	V_{DD} − 0.8	V_{p-p}

Note 53: For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8~3.6 V, Ta = −10~60°C.

LCD Common Output/Segment Output (COM1to COM3, $S_1$to S_{23})

Characteristics		Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Output current	"H" level	I_{OH1}	—	V_{LCD} = 3 V, V_{OH} = 2.7 V	−0.5	−1.0	—	mA
	"L" level	I_{OL1}	—	V_{LCD} = 3 V, V_{OL} = 0.3 V	0.5	1.0	—	
Output voltage 1/2 level		V_{BS}	—	No load	1.3	1.5	1.7	V

$\overline{HOLD}$ Input Port

Characteristics		Symbol	Test Circuit	Test Condition	Min.	Typ..	Max.	Unit
Input leak current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH1}	—	—	2.4	~	3.0	V
	"L" level	V_{IL1}	—	—	0	~	1.2	

A/D Converter (A/D_{IN1}, A/D_{IN2}, DC-REF)

Characteristics	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Analog input voltage range	V_{AD}	—	AD_{IN1}, AD_{IN2}	0	~	V_{DD}	V
Analog reference voltage range	V_{REF}	—	DC-REF, V_{DD} = 2.0~3.6 V	1.0	~	V_{DD} × 0.9	V
Resolution	V_{RES}	—	—	—	6.0	—	bit
Conversion total error	—	—	V_{DD} = 2.0 to 3.6 V	—	±1.0	±4.0	LSB
Analog input leak	I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V (AD_{IN1}, AD_{IN2}, DC-REF)	—	—	±1.0	μA

Key Input Port (K_0~K_3)

Characteristics		Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
N-ch/P-ch input resistance		R_{IN1}	—	—	75	150	300	kΩ
Input voltage	"H" level	V_{IH2}	—	When input with pull-down resistance	1.8	~	3.0	V
	"L" level	V_{IL2}	—	When input with pull-down resistance	0	~	0.3	
Input voltage	"H" level	V_{IH3}	—	When input with pull-up resistance	2.7	~	3.0	V
	"L" level	V_{IL3}	—	When input with pull-up resistance	0	~	1.2	
Input leak current		I_{LI}	—	When input resistance off, V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA

Timing Output Port (T0~T5)

Characteristics		Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Output current	"H" level	I_{OH1}	—	V_{OH} = 2.7 V	−0.5	−1.0	—	mA
	"L" level	I_{OL1}	—	V_{OL} = 0.3 V, Use LCD key-return mode	0.5	1.0	—	
N-ch load resistance		R_{ON}	—	When LCD key-return mode is not used	75	150	300	kΩ

DO1/OT, DO2 Output; MUTE Output

Characteristics		Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Output current	"H" level	I_{OH1}	—	V_{OH} = 2.7 V	−0.5	−1.0	—	mA
	"L" level	I_{OL1}	—	V_{OL} = 0.3 V	0.5	1.0	—	
Output off leak current		I_{TL}	—	V_{TLH} = 3.0 V, V_{TLL} = 0 V (DO1, DO2)	—	—	±100	nA

General-Purpose I/O Ports (P1-0~P3-1)

Characteristics		Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Output current	"H" level	I_{OH1}	—	V_{OH} = 2.7 V	−0.5	−1.0	—	mA
	"L" level	I_{OL1}	—	V_{OL} = 0.3 V	0.5	1.0	—	
Input leak current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH4}	—	—	2.4	~	3.0	V
	"L" level	V_{IL4}	—	—	0	~	0.6	

IN, $\overline{\text{RESET}}$ Input Port

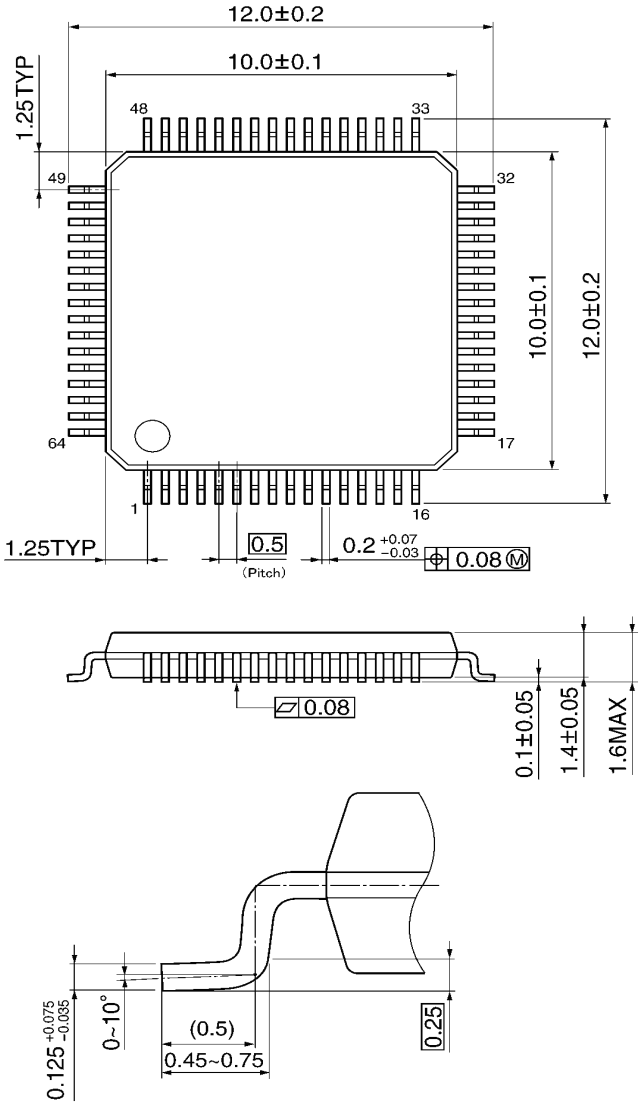
Characteristics		Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Input leak current		I_{LI}	—	V_{IH} = 3.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH4}	—	—	2.4	~	3.0	V
	"L" level	V_{IL4}	—	—	0	~	0.6	

Others

Characteristics	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Input pull-down resistance	R_{IN2}	—	(TEST)	25	50	100	kΩ
X_{IN} amp feedback resistance	R_{fXT}	—	(X_{IN}-X_{OUT})	—	20	—	MΩ
X_{OUT} output resistance	R_{OUT}	—	(X_{OUT})	—	3	—	kΩ
Input amp feedback resistance	R_{fIN1}	—	(FM_{IN}, AM_{IN})	150	300	600	kΩ
	R_{fIN2}	—	(IF_{IN})	500	1000	2000	
Voltage used to detect supply voltage drop	V_{STP}	—	(V_{DD})	1.35	1.55	1.75	V
Supply voltage drop detection temperature characteristics	D_S	—	(V_{DD})	—	−2	—	mV/°C

Package Dimensions

P-LQFP64-1010-0.50E Unit: mm

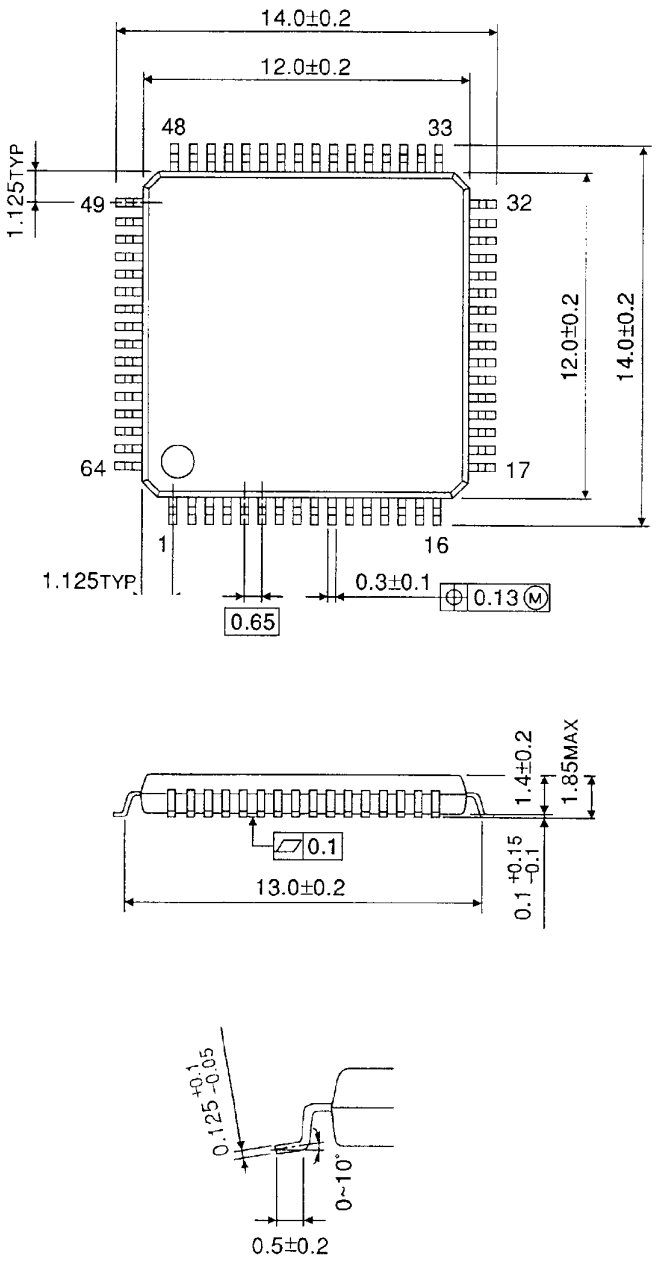


Note: Pd-plated leads

Weight: 0.32 g (typ.)

Package Dimensions

P-LQFP64-1212-0.65A Unit : mm



Note: Pd-plated leads

Weight: 0.45 g (typ.)

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