



64K × 8 CMOS FLASH MEMORY

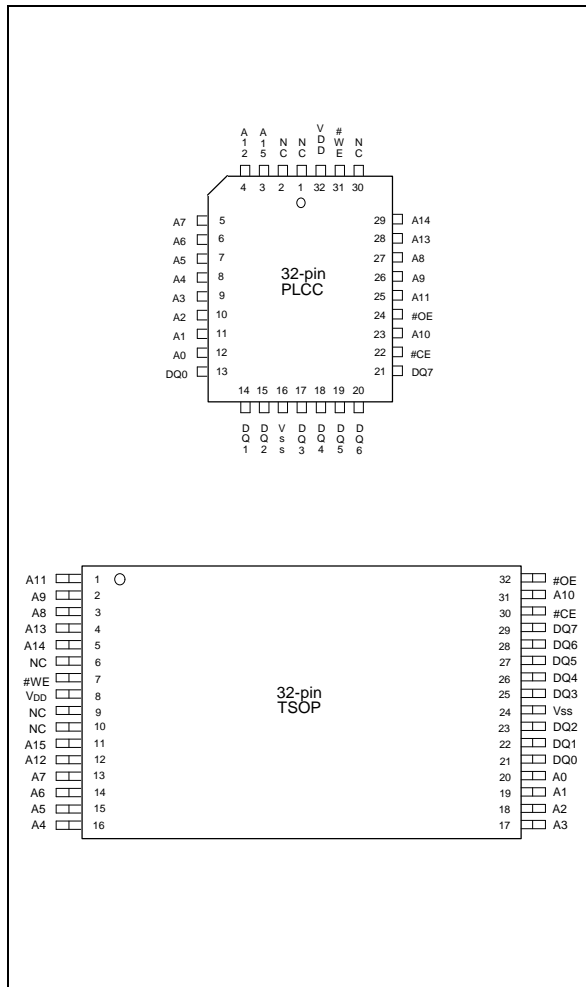
GENERAL DESCRIPTION

The W29C512A is a 512K bit, 5-volt only CMOS flash memory organized as 64K × 8 bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt VPP is not required. The unique cell architecture of the W29C512A results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

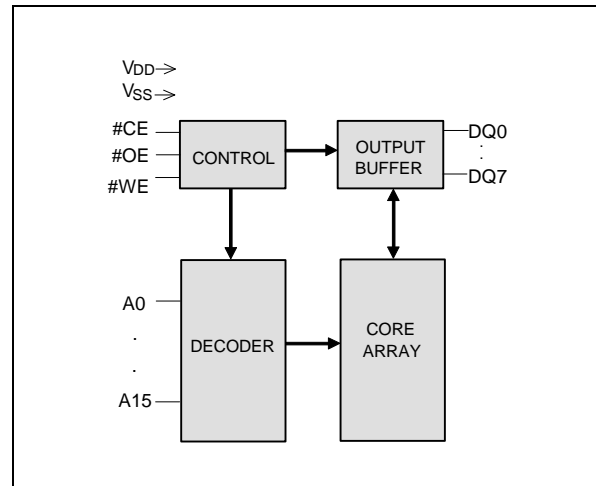
FEATURES

- Single 5-volt program and erase operations
- Fast page-write operations
 - 128 bytes per page
 - Page program cycle: 10 mS (max.)
 - Effective byte-program cycle time: 39 μS
 - Optional software-protected data write
- Fast chip-erase operation: 50 mS
- Read access time: 90 nS
- Typical page program/erase cycles: 1K (typ.)
- Ten-year data retention
- Software and hardware data protection
- Low power consumption
 - Active current: 50 mA (max.)
 - Standby current: 100 μA (max.)
- Automatic program timing with internal VPP generation
- End of program detection
 - Toggle bit
 - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard byte-wide pinouts
- Available packages: 32-pin PLCC and TSOP

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

| SYMBOL | PIN NAME |
|-----------|---------------------|
| A0 – A15 | Address Inputs |
| DQ0 – DQ7 | Data Inputs/Outputs |
| $\#CE$ | Chip Enable |
| $\#OE$ | Output Enable |
| $\#WE$ | Write Enable |
| V_{DD} | Power Supply |
| V_{SS} | Ground |
| NC | No Connection |

FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W29C512A is controlled by #CE and #OE, both of which have to be low for the host to obtain data from the outputs. #CE is used for device selection. When #CE is high, the chip is de-selected and only standby power will be consumed. #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either #CE or #OE is high. Refer to the timing waveforms for further details.

Page Write Mode

The W29C512A is programmed on a page basis. Every page contains 128 bytes of data. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded will be erased to "FFh" during programming of the page.

The write operation is initiated by forcing #CE and #WE low and #OE high. The write procedure consists of two steps. Step 1 is the byte-load cycle, in which the host writes to the page buffer of the device. Step 2 is an internal programming cycle, during which the data in the page buffers are simultaneously written into the memory array for non-volatile storage.

During the byte-load cycle, the addresses are latched by the falling edge of either #CE or #WE, whichever occurs last. The data are latched by the rising edge of either #CE or #WE, whichever occurs first. If the host loads a second byte into the page buffer within a byte-load cycle time (TBLC) of 150 μ S, after the initial byte-load cycle, the W29C512A will stay in the page load cycle. Additional bytes can then be loaded consecutively. The page load cycle will be terminated and the internal programming cycle will start if no additional byte is loaded into the page buffer. A7 to A15 specify the page address. All bytes that are loaded into the page buffer must have the same page address. A0 to A6 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

In the internal programming cycle, all data in the page buffers, i.e., 128 bytes of data, are written simultaneously into the memory array. Before the completion of the internal programming cycle, the host is free to perform other tasks such as fetching data from other locations in the system to prepare to write the next page.

Software-protected Data Write

The device provides a JEDEC-approved optional software-protected data write. Once this scheme is enabled, any write operation requires a series of three-byte program commands (with specific data to a specific address) to be performed before the data load operation. The three-byte load command sequence begins the page load cycle, without which the write operation will not be activated. This write scheme provides optimal protection against inadvertent write cycles, such as cycles triggered by noise during system power-up and power-down.

The W29C512A is shipped with the software data protection enabled. To enable the software data protection scheme, perform the three-byte command cycle at the beginning of a page load cycle. The device will then enter the software data protection mode, and any subsequent write operation must be preceded by the three-byte program command cycle. Once enabled, the software data protection will remain enabled unless the disable commands are issued. A power transition will not reset the software data protection feature. To reset the device to unprotected mode, a six-byte command sequence is required.



Hardware Data Protection

The integrity of the data stored in the W29C512A is also hardware protected in the following ways:

- (1) Noise/Glitch Protection: A #WE pulse of less than 15 nS in duration will not initiate a write cycle.
- (2) VDD Power Up/Down Detection: The programming and read operation are inhibited when VDD is less than 2.8V.
- (3) Write Inhibit Mode: Forcing #OE low, #CE high, or #WE high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

Data Polling (DQ7)-Write Status Detection

The W29C512A includes a data polling feature to indicate the end of a programming cycle. When the W29C512A is in the internal programming cycle, any attempt to read DQ7 of the last byte loaded during the page/byte-load cycle will receive the complement of the true data. Once the programming cycle is completed, DQ7 will show the true data.

Toggle Bit (DQ6)-Write Status Detection

In addition to data polling, the W29C512A provides another method for determining the end of a program cycle. During the internal programming cycle, any consecutive attempts to read DQ6 will produce alternating 0's and 1's. When the programming cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

5-Volt-only Software Chip Erase

The chip-erase mode can be initiated by a six-byte command sequence. After the command loading cycles, the device enters the internal chip erase mode, which is automatically timed and will be completed in 50 mS. The host system is not required to provide any control or timing during this operation.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-byte command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code (DAh). A read from address 0001H outputs the device code (C8h). The product ID operation can be terminated by a three-byte command sequence.

In the hardware access mode, access to the product ID is activated by forcing #CE and #OE low, #WE high, and raising A9 to 12 volts.

TABLE OF OPERATING MODES

Operating Mode Selection

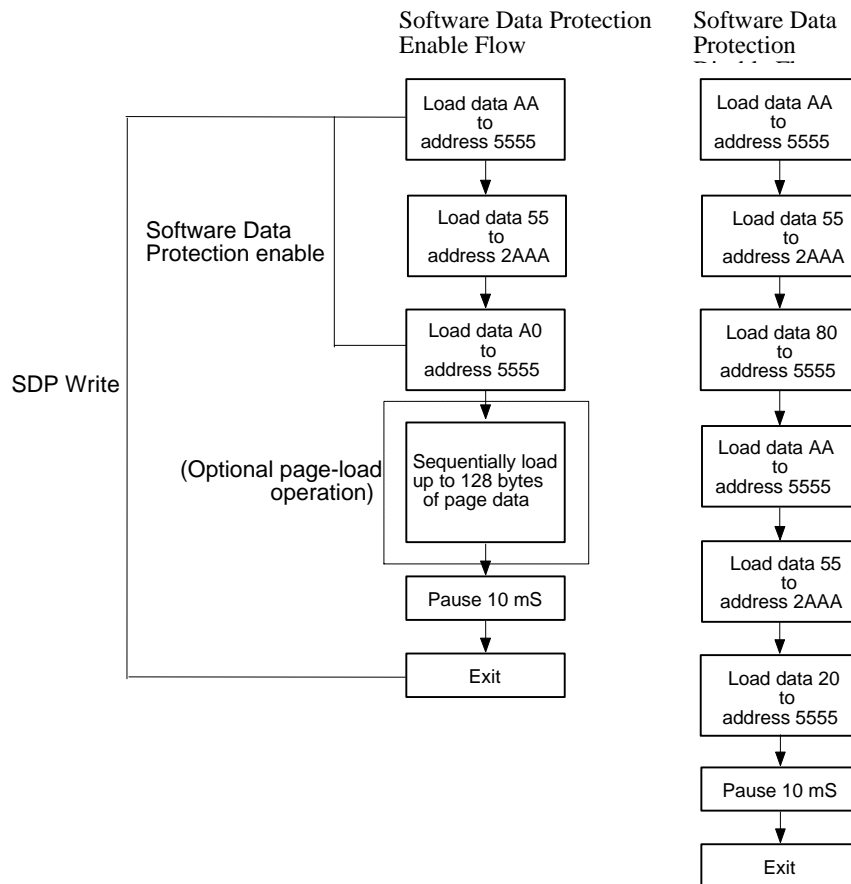
(Operating Range = 0 to 70° C (Ambient Temperature), V_{DD} = 5V ±10%, V_{SS} = 0V, V_{HH} = 12V)

| MODE | PINS | | | | |
|----------------------------|------|-----|-----|---------------------------------------|-------------------------------|
| | #CE | #OE | #WE | ADDRESS | DQ. |
| Read | VIL | VIL | VIH | A1N | Dout |
| Write | VIL | VIH | VIL | A1N | Din |
| Standby | VIH | X | X | X | High Z |
| Write Inhibit | X | VIL | X | X | High Z/DOUT |
| | X | X | VIH | X | High Z/DOUT |
| Output Disable | X | VIH | X | X | High Z |
| 5-Volt Software Chip Erase | VIL | VIH | VIL | A1N | D1N |
| Product ID | VIL | VIL | VIH | A0 = VIL; A1 – A15 = VIL; A9 = VHH | Manufacturer Code DA (Hex) |
| | VIL | VIL | VIH | A0 = VIH; A1 – A15 = VIL; A9 = VHH | Device Code C8 (Hex) |

Command Codes for Software Data Protection

| BYTE SEQUENCE | TO ENABLE PROTECTION | | TO DISABLE PROTECTION | |
|---------------|----------------------|------|-----------------------|------|
| | ADDRESS | DATA | ADDRESS | DATA |
| 0 Write | 5555H | AAH | 5555H | AAH |
| 1 Write | 2AAAH | 55H | 2AAAH | 55H |
| 2 Write | 5555H | A0H | 5555H | 80H |
| 3 Write | - | - | 5555H | AAH |
| 4 Write | - | - | 2AAAH | 55H |
| 5 Write | - | - | 5555H | 20H |

Software Data Protection Acquisition Flow

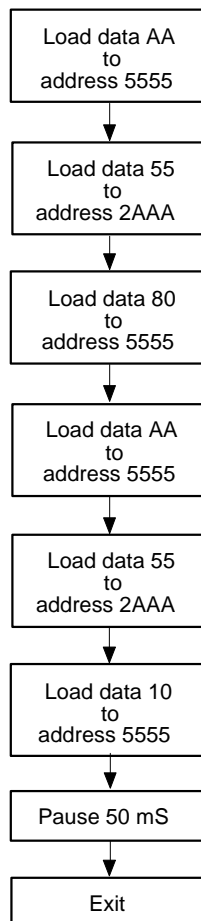


Notes for software program code:
 Data Format: DQ7 – DQ0 (Hex)
 Address Format: A14 – A0 (Hex)

Command Codes for Software Chip Erase

| BYTE SEQUENCE | ADDRESS | DATA |
|---------------|---------|------|
| 0 Write | 5555H | AAH |
| 1 Write | 2AAAH | 55H |
| 2 Write | 5555H | 80H |
| 3 Write | 5555H | AAH |
| 4 Write | 2AAAH | 55H |
| 5 Write | 5555H | 10H |

Software Chip Erase Acquisition Flow



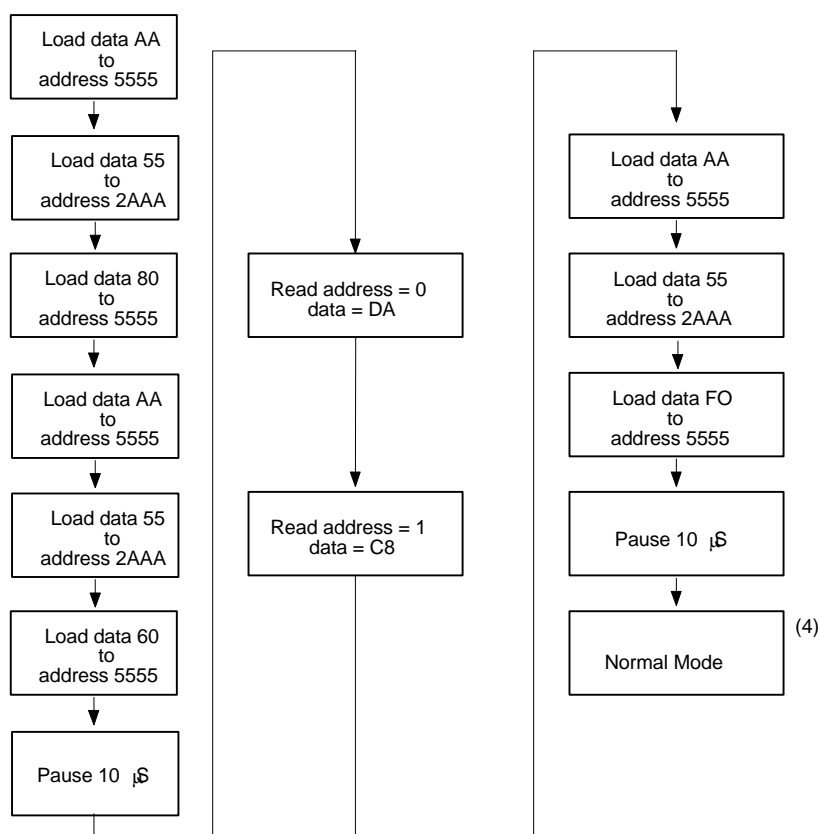
Notes for software chip erase:
 Data Format: DQ7 – DQ0 (Hex)
 Address Format: A14 – A0 (Hex)

Command Codes for Product Identification

| BYTE SEQUENCE | ALTERNATE SOFTWARE (5) PRODUCT IDENTIFICATION ENTRY | | SOFTWARE PRODUCT IDENTIFICATION ENTRY | | SOFTWARE PRODUCT IDENTIFICATION EXIT | |
|---------------|---|------|---------------------------------------|------|--------------------------------------|------|
| | ADDRESS | DATA | ADDRESS | DATA | ADDRESS | DATA |
| 0 Write | 5555H | AAH | 5555H | AAH | 5555H | AAH |
| 1 Write | 2AAAH | 55H | 2AAAH | 55H | 2AAAH | 55H |
| 2 Write | 5555H | 90H | 5555H | 80H | 5555H | F0H |
| 3 Write | - | - | 5555H | AAH | - | - |
| 4 Write | - | - | 2AAAH | 55H | - | - |
| 5 Write | - | - | 5555H | 60H | - | - |
| | Pause 10 μ S | | Pause 10 μ S | | Pause 10 μ S | |

Software Product Identification Acquisition Flow

Product Identification Entry (1) Product Identification Mode (2,3) Product Identification Exit (1)



Notes for software product identification:

- (1) Data format: DQ7 – DQ0 (Hex); address format: A14 – A0 (Hex).
- (2) A1 – A16 = V_{IL} ; manufacture code is read for A0 = V_{IL} ; device code is read for A0 = V_{IH} .
- (3) The device does not remain in identification mode if power down.
- (4) The device returns to standard operation mode.
- (5) This product supports both the JEDEC standard 3 byte command code sequence and original 6 byte command code sequence. For new designs, Winbond recommends that the 3 byte command code sequence be used.



DC CHARACTERISTICS

Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|---|------------------------------|------|
| Power Supply Voltage to V _{ss} Potential | -0.5 to +7.0 | V |
| Operating Temperature | 0 to +70 | °C |
| Storage Temperature | -65 to +150 | °C |
| D.C. Voltage on Any Pin to Ground Potential except A9 | -0.5 to V _{DD} +1.0 | V |
| Transient Voltage (< 20 nS) on Any Pin to Ground Potential | -1.0 to V _{DD} +1.0 | V |
| Voltage on A9 and #OE Pin to Ground Potential | -0.5 to 12.5 | V |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5.0V ± 5%, V_{ss} = 0V, T_A = 0 to 70° C)

| PARAMETER | SYM. | TEST CONDITIONS | LIMITS | | | UNIT |
|--|------------------|---|--------|------|------|------|
| | | | MIN. | TYP. | MAX. | |
| Power Supply Current | I _{CC} | #CE = #OE = V _{IL} , #WE = V _{IH} , all I/Os open Address inputs = V _{IL} /V _{IH} , at f = 5 MHz | - | - | 50 | mA |
| Standby V _{DD} Current (TTL Input) | I _{SB1} | #CE = V _{IH} , all I/Os open Other inputs = V _{IL} /V _{IH} | - | 2 | 3 | mA |
| Standby V _{DD} Current (CMOS Input) | I _{SB2} | #CE = V _{DD} -0.3V, all I/Os open Other inputs = V _{DD} -0.3V /V _{ss} | - | 20 | 100 | μA |
| Input Leakage Current | I _{LI} | V _{IN} = V _{ss} to V _{DD} | - | - | 10 | μA |
| Output Leakage Current | I _{LO} | V _{IN} = V _{ss} to V _{DD} | - | - | 10 | μA |
| Input Low Voltage | V _{IL} | - | - | - | 0.8 | V |
| Input High Voltage | V _{IH} | - | 2.0 | - | - | V |
| Output Low Voltage | V _{OL} | I _{OL} = 2.1 mA | - | - | 0.45 | V |
| Output High Voltage | V _{OH1} | I _{OH} = -0.4 mA | 2.4 | - | - | V |
| Output High Voltage CMOS | V _{OH2} | I _{OH} = -100 μA; V _{DD} = 4.5V | 4.2 | - | - | V |

Power-up Timing

| PARAMETER | SYMBOL | TYPICAL | UNIT |
|-----------------------------|-----------|---------|---------|
| Power-up to Read Operation | TPU.READ | 100 | μ S |
| Power-up to Write Operation | TPU.WRITE | 5 | mS |

CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

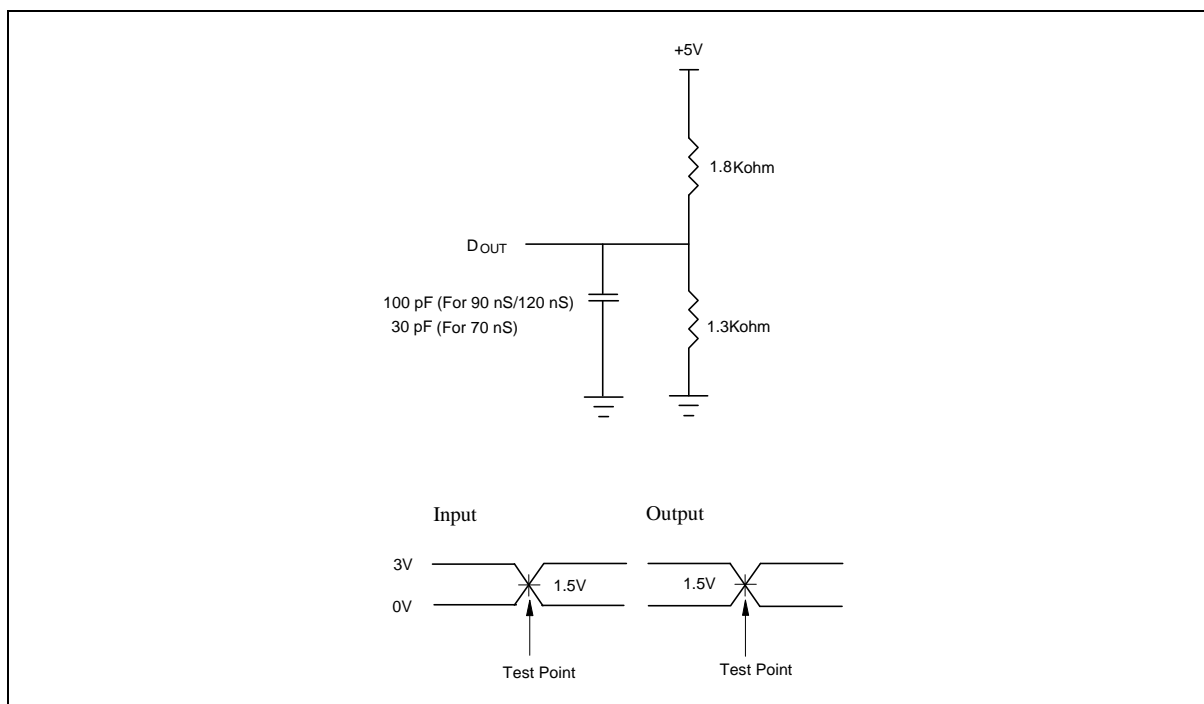
| PARAMETER | SYMBOL | CONDITIONS | MAX. | UNIT |
|---------------------|------------------|-----------------------|------|------|
| I/O Pin Capacitance | C _{I/O} | V _{I/O} = 0V | 12 | pF |
| Input Capacitance | C _{IN} | V _{IN} = 0V | 6 | pF |

AC CHARACTERISTICS

AC Test Conditions

| PARAMETER | CONDITIONS |
|---------------------------|---|
| Input Pulse Levels | 0V to 3V |
| Input Rise/Fall Time | < 5 nS |
| Input/Output Timing Level | 1.5V/1.5V |
| Output Load | 1 TTL Gate and C _L = 100 pF/ 30 pF |

AC Test Load and Waveform





Read Cycle Timing Parameters

(V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = 0 to 70° C)

| PARAMETER | SYM. | W29C512A-90 | | UNIT |
|---------------------------------|------|-------------|------|------|
| | | MIN. | MAX. | |
| Read Cycle Time | TRC | 90 | - | nS |
| Chip Enable Access Time | TCE | - | 90 | nS |
| Address Access Time | TAA | - | 90 | nS |
| Output Enable Access Time | TOE | - | 40 | nS |
| #CE High to High-Z Output | TCHZ | - | 25 | nS |
| #WE High to High-Z Output | TOHZ | - | 25 | nS |
| Output Hold from Address Change | TOH | 0 | - | nS |

Byte/Page-write Cycle Timing Parameters

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---------------------------------|--------|------|------|------|------|
| Write Cycle (Erase and Program) | TWC | - | - | 10 | mS |
| Address Setup Time | TAS | 0 | - | - | nS |
| Address Hold Time | TAH | 50 | - | - | nS |
| #WE and #CE Setup Time | TCS | 0 | - | - | nS |
| #WE and #CE Hold Time | TCH | 0 | - | - | nS |
| #OE High Setup Time | TOES | 0 | - | - | nS |
| #OE High Hold Time | TOEH | 0 | - | - | nS |
| #CE Pulse Width | TCP | 90 | - | - | nS |
| #WE Pulse Width | TWP | 90 | - | - | nS |
| #WE High Width | TWPH | 100 | - | - | nS |
| Data Setup Time | TDS | 35 | - | - | nS |
| Data Hold Time | TDH | 0 | - | - | nS |
| Byte Load Cycle Time | TBLC | - | - | 150 | μS |

Notes: All AC timing signals observe the following guidelines for determining setup and hold times:

- (1) High level signal's reference level is V_{IH}.
- (2) Low level signal's reference level is V_{IL}.



#DATA Polling Characteristics (1)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|-------------------------|-------------------|------|------|------|------|
| Data Hold Time | T _{DH} | 10 | - | - | nS |
| #OE Hold Time | T _{OE} H | 10 | - | - | nS |
| #OE to Output Delay (2) | T _{OE} | - | - | - | nS |
| Write Recovery Time | T _{WR} | 0 | - | - | nS |

Notes:

(1) These parameters are characterized and not 100% tested.

(2) See T_{OE} spec in A.C. Read Cycle Timing Parameters.

Toggle Bit Characteristics (1)

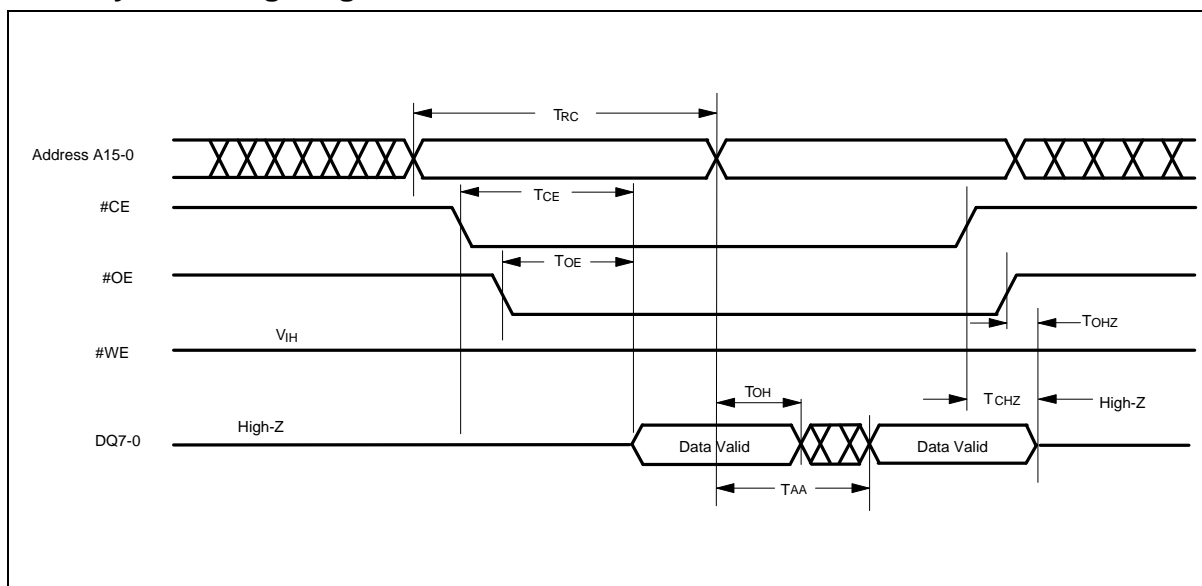
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|-------------------------|-------------------|------|------|------|------|
| Data Hold Time | T _{DH} | 10 | - | - | nS |
| #OE Hold Time | T _{OE} H | 10 | - | - | nS |
| #OE to Output Delay (2) | T _{OE} | - | - | - | nS |
| #OE High Pulse | T _{OEHP} | 150 | - | - | nS |
| Write Recovery Time | T _{WR} | 0 | - | - | nS |

Notes:

(1) These parameters are characterized and not 100% tested.

(2) See T_{OE} spec in A.C. Read Cycle Timing Parameters.

Read Cycle Timing Diagram



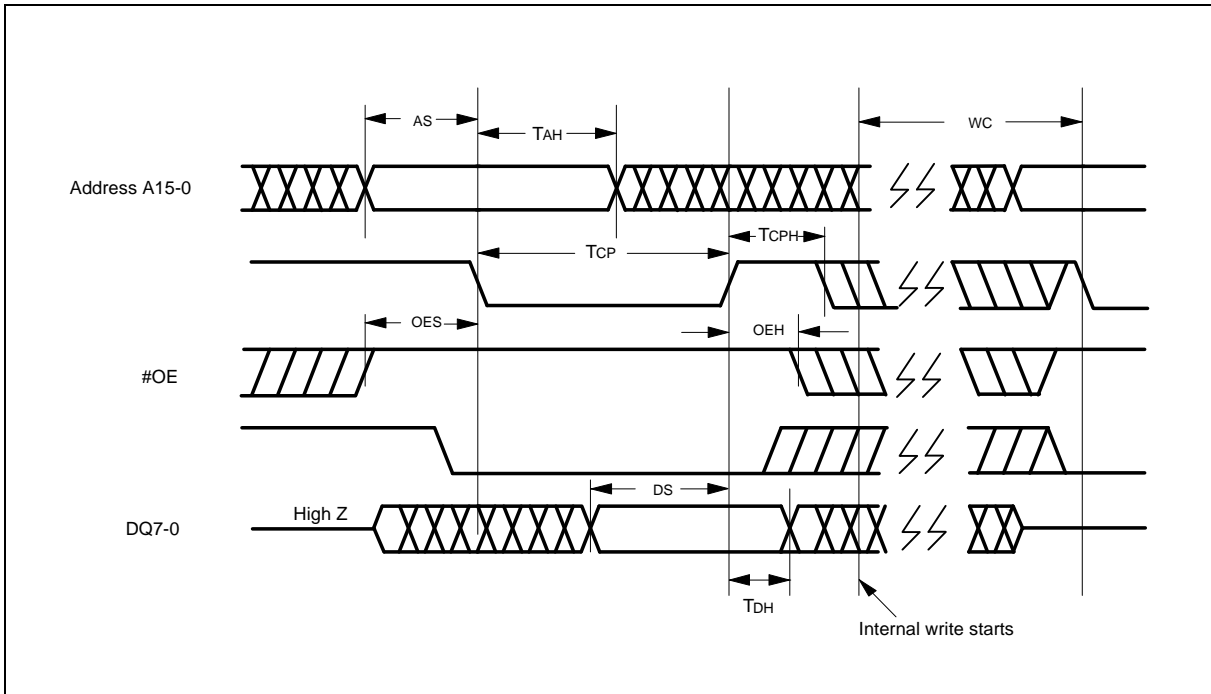
The diagram illustrates the timing for a write operation. The signals shown are Address A15-0, #CE, #OE, #WE, and DQ7-0. The timing parameters are defined as follows:

- T_{AS} : Address setup time before #CE falls.
- T_{AA} : Address hold time after #CE rises.
- T_{CS} : #CE setup time before #OE falls.
- T_{CH} : #CE hold time after #OE rises.
- T_{OES} : #OE setup time before #WE falls.
- T_{OEH} : #OE hold time after #WE rises.
- T_{WP} : #WE pulse width.
- T_{DP} : Data setup time before #WE falls.
- T_{DH} : Data hold time after #WE rises.
- T_{WC} : Write cycle time from #WE falls to #OE rises.

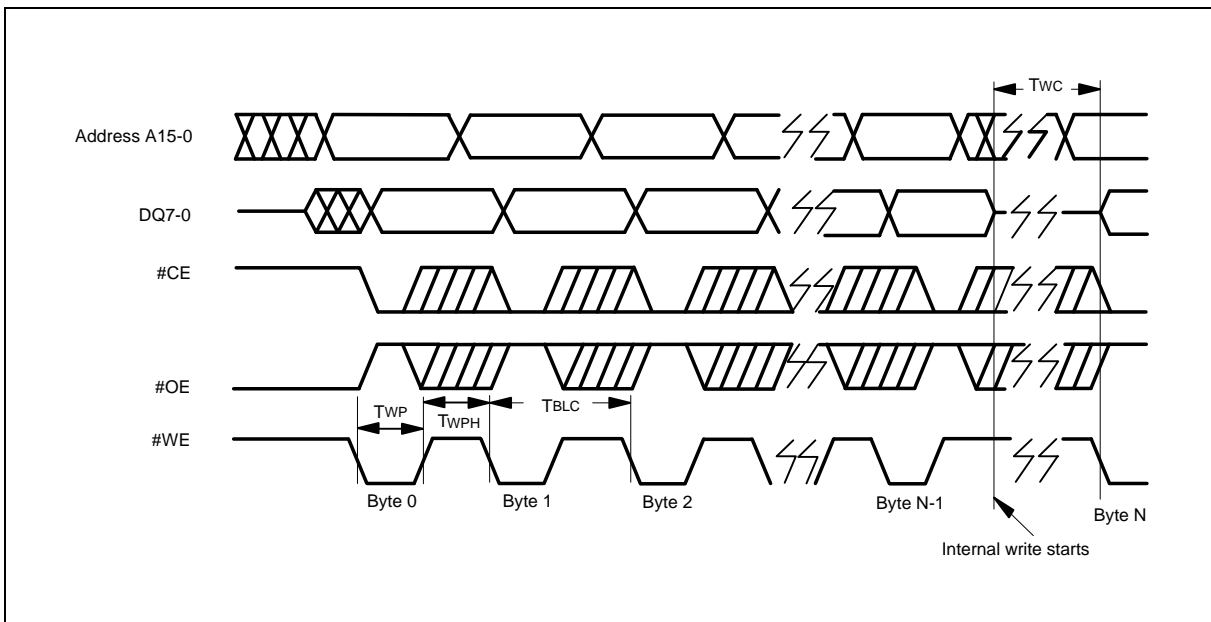
A note indicates "Internal write starts" at the point where #OE rises and #WE falls.

Timing Waveforms, continued

#CE Controlled Write Cycle Timing Diagram

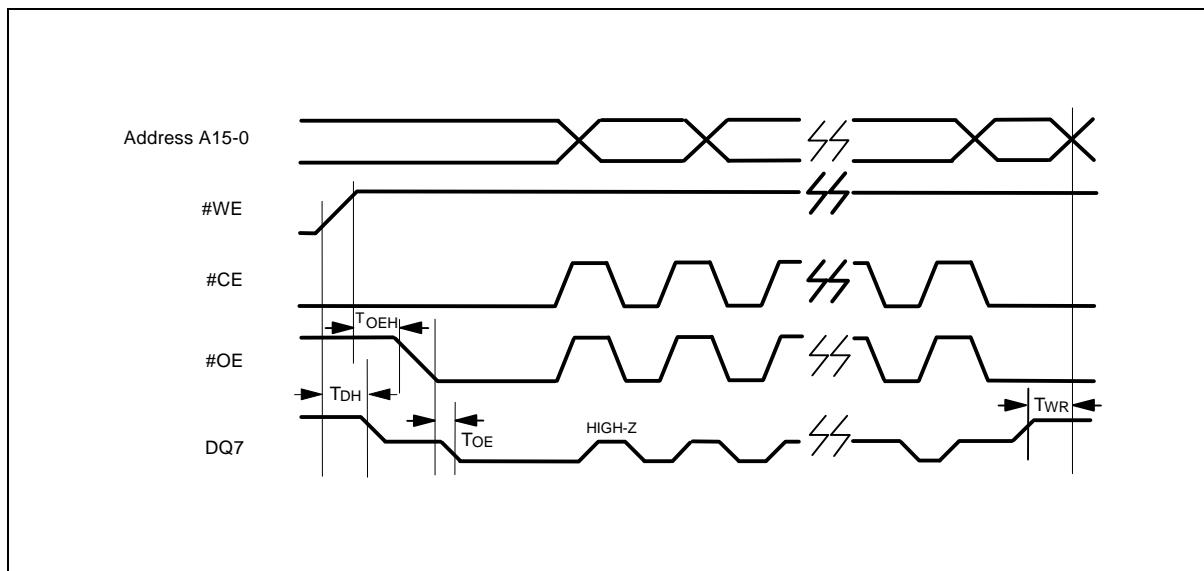


Page Write Cycle Timing Diagram

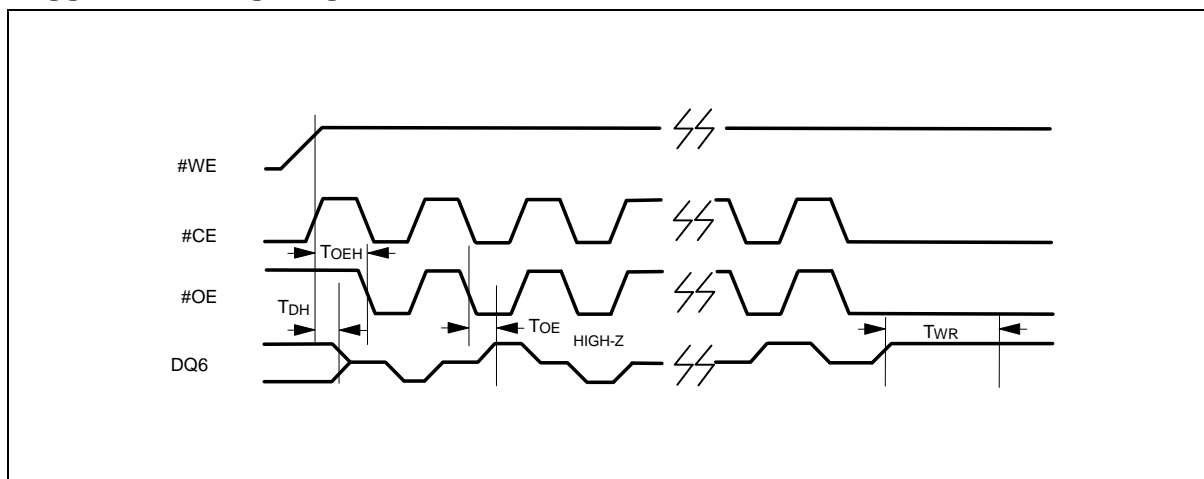


Timing Waveforms, continued

#DATA Polling Timing Diagram

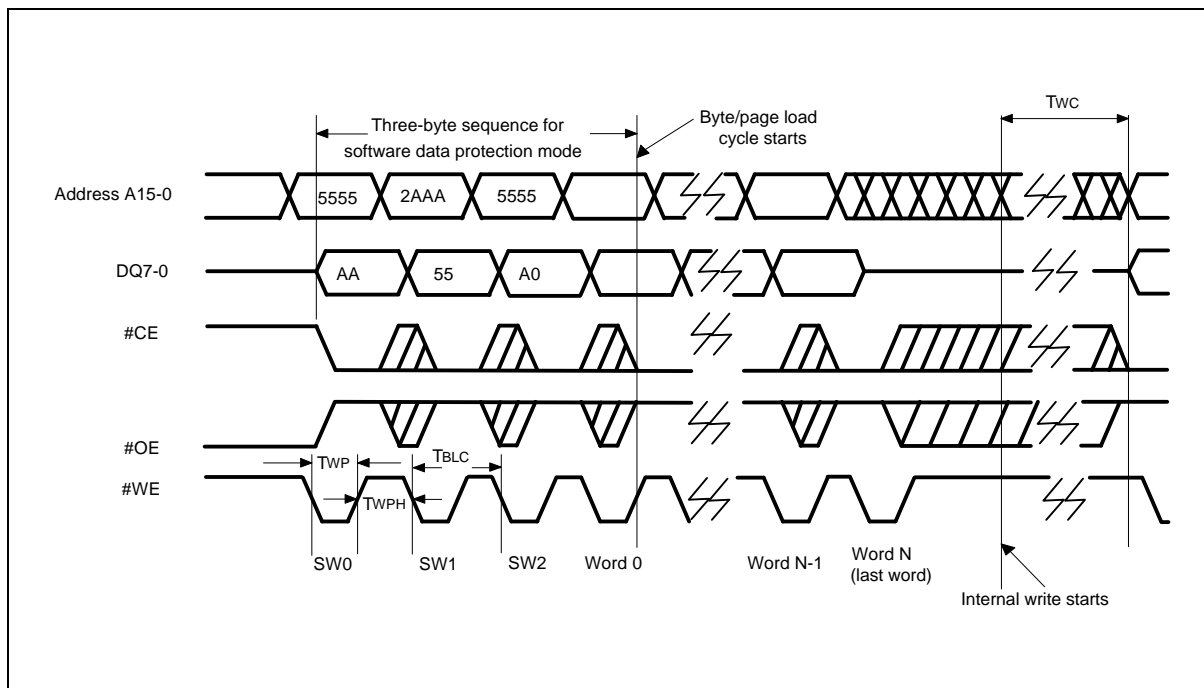


Toggle Bit Timing Diagram

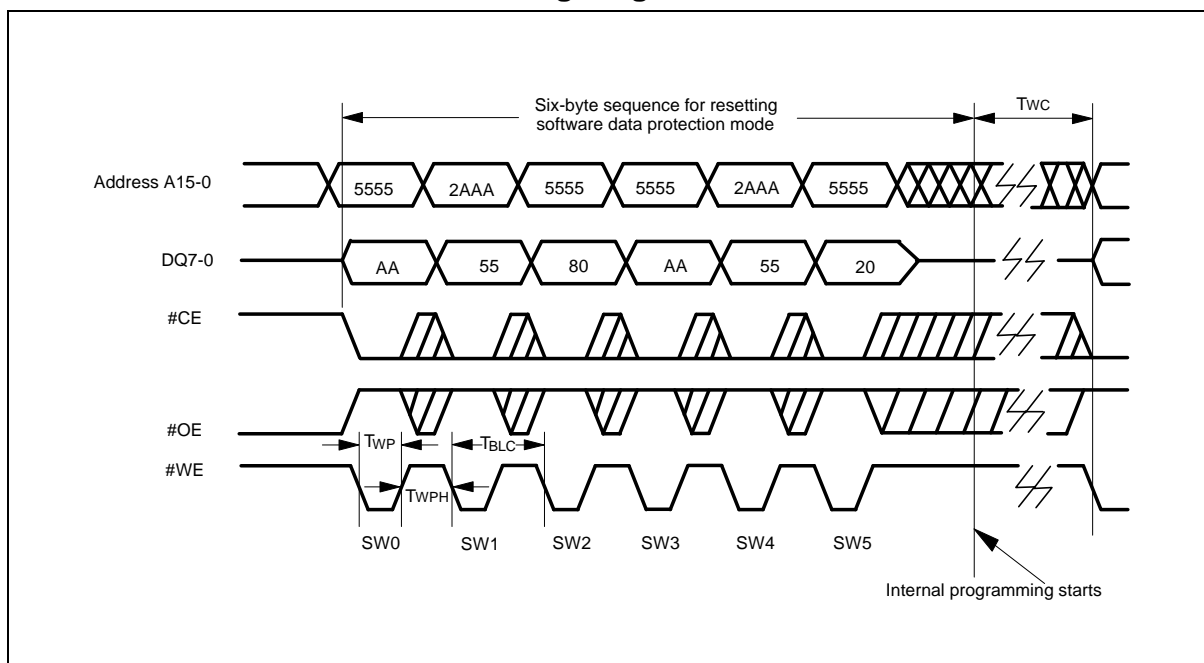


Timing Waveforms, continued

Page Write Timing Diagram Software Data Protection Mode

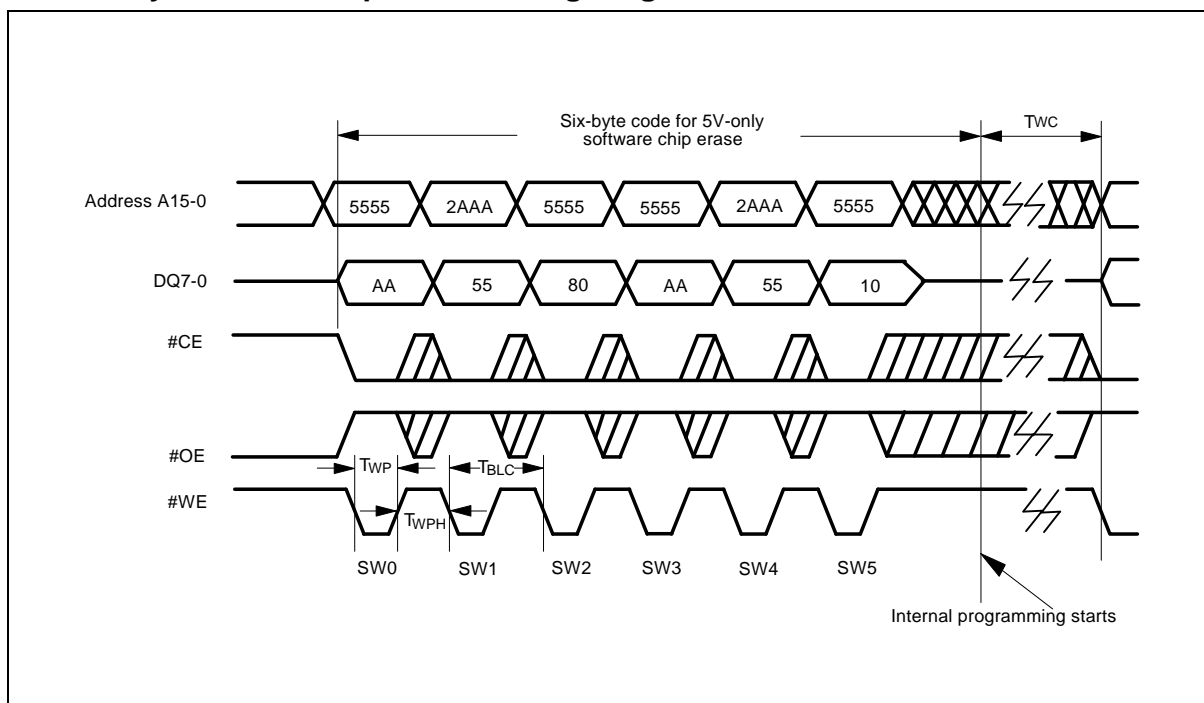


Reset Software Data Protection Timing Diagram



Timing Waveforms, continued

5-Volt-only Software Chip Erase Timing Diagram





ORDERING INFORMATION

| PART NO. | ACCESS TIME (nS) | POWER SUPPLY CURRENT MAX. (mA) | STANDBY V _{DD} CURRENT MAX. (mA) | PACKAGE | CYCLE |
|--------------|------------------|--------------------------------|---|---------------|-------|
| W29C512AP-90 | 90 | 50 | 100 | 32-pin PLCC | 1K |
| W29C512AT-90 | 90 | 50 | 100 | Type one TSOP | 1K |

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

HOW TO READ THE TOP MARKING

Example: The top marking of 32-pin TSOP W29C512AT-90



1st line: winbond logo

2nd line: the part number: W29C512AT-90

3rd line: the lot number

4th line: the tracking code: 149 O B RA

149: Packages made in '01, week 49

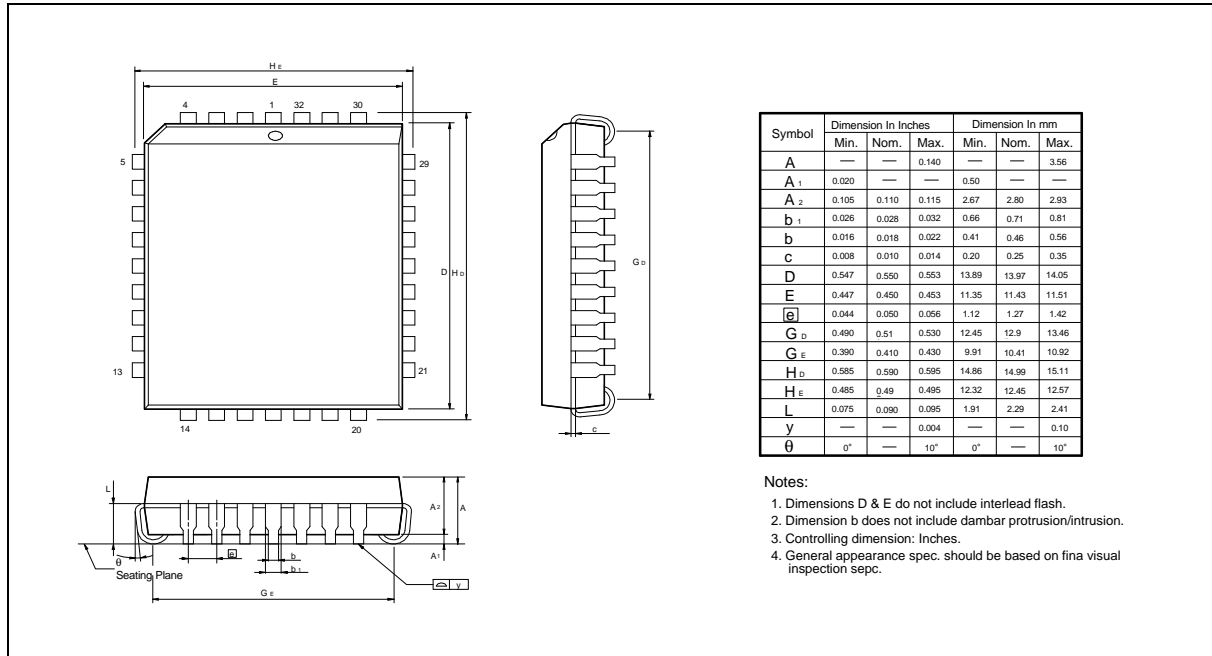
O: Assembly house ID: A means ASE, O means OSE, ... etc.

B: IC revision; A means version A, B means version B, ... etc.

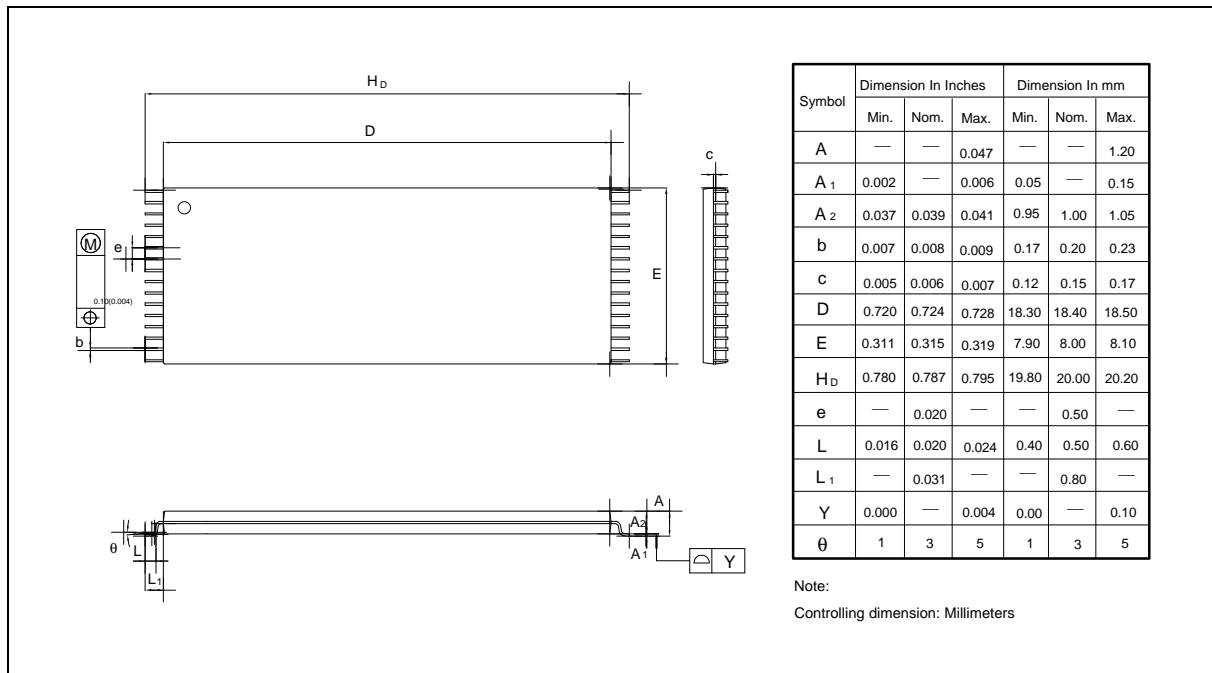
RA: Process code

PACKAGE DIMENSIONS

32-pin PLCC



32-pin TSOP





VERSION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---------|--------------|------|--|
| A1 | 9/7/2001 | - | Initial Issued |
| A2 | Feb. 5, 2002 | 18 | Add HOW TO READ THE TOP MARKING |
| | | 4 | Modify VDD Power Up/Down Detection in Hardware Data Protection |



Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
<http://www.winbond.com.tw/>

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu Chiu, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

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