

## Clock Generator for Intel PCI Express Mobile Chipset

### Features

- 14.318 MHz Crystal Input
- Selectable of 100, 133, 166, 200, 266, 333, and 400 MHz CPU Output Frequencies
- SMBus: Power Management Control
- Spread Spectrum support (-0.5% down spread)
- Packaging (Pb-free & Green available):  
— 56-Pin TSSOP

### Output Features

- Two Pairs of Differential CPU Clocks
- One selectable of CPU/SRC Clock
- Seven Pairs of SRC Clocks
- Six PCI Clocks
- One 48 MHz USB clock
- One REF clock
- One 96 MHz Differential clock

### Description

PI6C410M is a high-speed, low-noise clock generator designed to work with the Intel Mobile PCI Express Chipset. This Spread Spectrum PLL based clock generator reduces EMI emission and supports a wide range of frequencies.

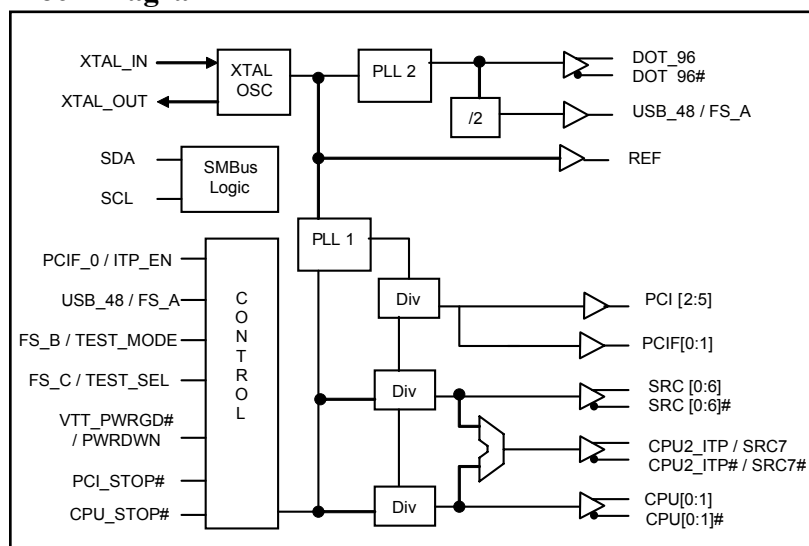
### Jitter Performance

- < 85ps Cycle-to-Cycle CPU 0/1 clock jitter
- < 125ps Cycle-to-Cycle CPU 2 clock jitter
- < 350ps Cycle-to-Cycle 48 MHz clock jitter
- < 500ps Cycle-to-Cycle PCI clock jitter
- < 125ps Cycle-to-Cycle SRC clock jitter
- < 1000ps Cycle-to-Cycle REF clock jitter

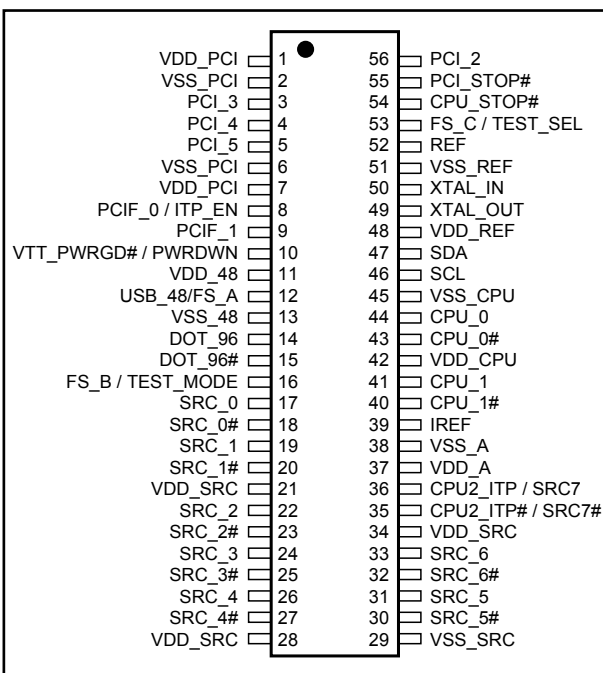
### Skew Performance

- < 100ps Output-to-output CPU 0/1 clock skew
- < 150ps Output-to-output CPU 2 clock skew
- < 500ps Output-to-output PCI clock skew
- < 250ps Output-to-output SRC clock skew

### Block Diagram



### Pin Configuration



**Pin Description**

| Pin Name                                 | Type              | Pin Number                                                      | Descriptions                                                                                                                                                                                       |
|------------------------------------------|-------------------|-----------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REF                                      | Output            | 52                                                              | 3.3V 14.31818 MHz output                                                                                                                                                                           |
| XTAL_IN                                  | Input             | 50                                                              | 14.31818 MHz crystal input                                                                                                                                                                         |
| XTAL_OUT                                 | Output            | 49                                                              | 14.31818 MHz crystal output                                                                                                                                                                        |
| CPU[0:1] & CPU[0:1]#                     | Output            | 40, 41, 43, 44                                                  | Differential CPU outputs                                                                                                                                                                           |
| SRC[0:6] & SRC[0:6]#                     | Output            | 17, 18, 19, 20,<br>22, 23, 24, 25,<br>26, 27, 30, 31,<br>32, 33 | Differential Serial Reference Clock outputs                                                                                                                                                        |
| CPU2_ITP / SRC_7 &<br>CPU2_ITP# / SRC_7# | Output            | 35, 36                                                          | Selectable Differential CPU or SRC clock output<br>ITP_EN = 0 @ Vtt_Pwrgd# assertion = SRC<br>ITP_EN = 1 @ Vtt_Pwrgd# assertion = CPU                                                              |
| PCIF_0 / ITP_EN                          | Input /<br>Output | 8                                                               | 33 MHz clock output / CPU2 select when HIGH                                                                                                                                                        |
| PCIF_1                                   | Output            | 9                                                               | 33 MHz clocks outputs (free running)                                                                                                                                                               |
| PCI[2:5]                                 | Output            | 3, 4, 5, 56                                                     | 33 MHz clocks outputs                                                                                                                                                                              |
| USB_48 / FS_A                            | Input /<br>Output | 12                                                              | 48 MHz clock output / 3.3V LVTTL inputs for CPU frequency selection                                                                                                                                |
| DOT_96 & DOT_96#                         | Output            | 14, 15                                                          | 96 MHz differential clock output                                                                                                                                                                   |
| PCI_STOP#                                | Input             | 55                                                              | 3.3V LVTTL active low input for PCI Stop operation.<br>(150k-ohm internal pull-up resistor)                                                                                                        |
| CPU_STOP#                                | Input             | 54                                                              | 3.3V LVTTL active low input for CPU Stop operation.<br>(150k-ohm internal pull-up resistor)                                                                                                        |
| FS_B / TEST_MODE                         | Input             | 16                                                              | 3.3V LVTTL inputs for CPU frequency selection / Test Mode select: 0 = Hi-Z, 1 = Ref/N                                                                                                              |
| FS_C / TEST_SEL                          | Input             | 53                                                              | 3.3V LVTTL inputs for CPU frequency selection / Test Mode select if pulled to 3.3V when Vtt_Pwrgd# is asserted LOW                                                                                 |
| IREF                                     | Input             | 39                                                              | External resistor connection for internal current reference                                                                                                                                        |
| VTT_PWRGD# /<br>PWRDWN                   | Input             | 10                                                              | 3.3V LVTTL Level sensitive strobe used to determine to latch the FS_A, FS_B/TEST_MODE, FS_C/TEST_SEL and PCIF0/ITP_EN inputs (active low) / 3.3V LVTTL active high input for Power Down operation. |
| SDA                                      | I/O               | 47                                                              | SMBus compatible SDATA                                                                                                                                                                             |
| SCL                                      | Input             | 46                                                              | SMBus compatible SCLOCK                                                                                                                                                                            |
| VDD_PCI                                  | Power             | 1, 7                                                            | 3.3V Power Supply for Outputs                                                                                                                                                                      |
| VDD_48                                   | Power             | 11                                                              | 3.3V Power Supply for Outputs                                                                                                                                                                      |
| VDD_SRC                                  | Power             | 21, 28, 34                                                      | 3.3V Power Supply for Outputs                                                                                                                                                                      |
| VDD_CPU                                  | Power             | 42                                                              | 3.3V Power Supply for Outputs                                                                                                                                                                      |
| VDD_REF                                  | Power             | 48                                                              | 3.3V Power Supply for Outputs                                                                                                                                                                      |
| VSS_PCI                                  | Ground            | 2, 6                                                            | Ground for Outputs                                                                                                                                                                                 |
| VSS_48                                   | Ground            | 13                                                              | Ground for Outputs                                                                                                                                                                                 |
| VSS_SRC                                  | Ground            | 29                                                              | Ground for Outputs                                                                                                                                                                                 |
| VSS_CPU                                  | Ground            | 45                                                              | Ground for Outputs                                                                                                                                                                                 |
| VSS_REF                                  | Ground            | 51                                                              | Ground for Outputs                                                                                                                                                                                 |
| VDD_A                                    | Power             | 37                                                              | 3.3V Power Supply for PLL                                                                                                                                                                          |
| VSS_A                                    | Ground            | 38                                                              | Ground for PLL                                                                                                                                                                                     |

## Functionality

### Frequency Selection<sup>(1)</sup>

| FS_C | FS_B | FS_A | CPU      | SRC     | PCIF / PCI | REF        | DOT_96 | USB_48 |
|------|------|------|----------|---------|------------|------------|--------|--------|
| 1    | 0    | 1    | 100 MHz  | 100 MHz | 33 MHz     | 14.318 MHz | 96 MHz | 48 MHz |
| 0    | 0    | 1    | 133 MHz  | 100 MHz | 33 MHz     | 14.318 MHz | 96 MHz | 48 MHz |
| 0    | 1    | 1    | 166 MHz  | 100 MHz | 33 MHz     | 14.318 MHz | 96 MHz | 48 MHz |
| 0    | 1    | 0    | 200 MHz  | 100 MHz | 33 MHz     | 14.318 MHz | 96 MHz | 48 MHz |
| 0    | 0    | 0    | 266 MHz  | 100 MHz | 33 MHz     | 14.318 MHz | 96 MHz | 48 MHz |
| 1    | 0    | 0    | 333 MHz  | 100 MHz | 33 MHz     | 14.318 MHz | 96 MHz | 48 MHz |
| 1    | 1    | 0    | 400 MHz  | 100 MHz | 33 MHz     | 14.318 MHz | 96 MHz | 48 MHz |
| 1    | 1    | 1    | Reserved | 100 MHz | 33 MHz     | 14.318 MHz | 96 MHz | 48 MHz |

**Note:**

1. Refer to DC Electrical Characteristics for FS\_A, FS\_B and FS\_C (Vih\_FS, Vil\_FS) threshold levels.

### Test Mode Selection<sup>(2)</sup>

| TEST_MODE | CPU   | SRC   | PCIF / PCI | REF  | DOT_96 | USB_48 |
|-----------|-------|-------|------------|------|--------|--------|
| 1         | REF/N | REF/N | REF/N      | REF  | REF/N  | REF/N  |
| 0         | Hi-Z  | Hi-Z  | Hi-Z       | Hi-Z | Hi-Z   | Hi-Z   |

**Note:**

2. Test mode will occur where the SMBus Bit 6 of Byte 6 = 1, or FS\_C/TEST\_SEL is set to logic high level.

### PWRDWN Functionality

| PWRDWN | CPU               | CPU#   | SRC               | SRC#   | PCIF / PCI | REF        | DOT_96            | DOT_96# | USB_48 |
|--------|-------------------|--------|-------------------|--------|------------|------------|-------------------|---------|--------|
| 0      | Normal            | Normal | Normal            | Normal | 33 MHz     | 14.318 MHz | Normal            | Normal  | 48 MHz |
| 1      | Iref × 2 or Float | Float  | Iref × 2 or Float | Float  | Low        | Low        | Iref × 2 or Float | Float   | Low    |

### PCI\_STOP# Functionality

| PCI_STOP# | CPU    | CPU#   | SRC               | SRC#   | PCIF / PCI | REF        | DOT_96 | DOT_96# | USB_48 |
|-----------|--------|--------|-------------------|--------|------------|------------|--------|---------|--------|
| 1         | Normal | Normal | Normal            | Normal | 33 MHz     | 14.318 MHz | Normal | Normal  | 48 MHz |
| 0         | Normal | Normal | Iref × 6 or Float | Low    | Low        | 14.318 MHz | Normal | Normal  | 48 MHz |

### CPU\_STOP# Functionality

| CPU_STOP# | CPU               | CPU#   | SRC    | SRC#   | PCIF / PCI | REF        | DOT_96 | DOT_96# | USB_48 |
|-----------|-------------------|--------|--------|--------|------------|------------|--------|---------|--------|
| 1         | Normal            | Normal | Normal | Normal | 33 MHz     | 14.318 MHz | Normal | Normal  | 48 MHz |
| 0         | Iref × 6 or Float | Low    | Normal | Normal | 33 MHz     | 14.318 MHz | Normal | Normal  | 48 MHz |

### Serial Data Interface (SMBus)

PI6C410M is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

### Address Assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|----|----|----|----|----|----|----|-----|
| 1  | 1  | 0  | 1  | 0  | 0  | 1  | I/O |

### Data Protocol<sup>(1)</sup>

|           |            |     |     |                 |     |                |     |             |     |  |                 |     |          |
|-----------|------------|-----|-----|-----------------|-----|----------------|-----|-------------|-----|--|-----------------|-----|----------|
| 1 bit     | 7 bits     | 1   | 1   | 8 bits          | 1   | 8 bits         | 1   | 8 bits      | 1   |  | 8 bits          | 1   | 1 bit    |
| Start bit | Slave Addr | R/W | Ack | Register offset | Ack | Byte Count = N | Ack | Data Byte 0 | Ack |  | Data Byte N - 1 | Ack | Stop bit |

#### Note:

1 Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

### Data Byte 0: Control Register

| Bit | Descriptions                                                    | Type | Power Up Condition | Output(s) Affected | Pin    | Source Pin |
|-----|-----------------------------------------------------------------|------|--------------------|--------------------|--------|------------|
| 0   | SRC_0 Output Enable<br>1 = Enabled, 0 = Disabled (Hi-Z)         | RW   | 1 = Enabled        | SRC_0              | 17, 18 | NA         |
| 1   | SRC_1 Output Enable<br>1 = Enabled, 0 = Disabled (Hi-Z)         | RW   | 1 = Enabled        | SRC_1              | 19, 20 | NA         |
| 2   | SRC_2 Output Enable<br>1 = Enabled, 0 = Disabled (Hi-Z)         | RW   | 1 = Enabled        | SRC_2              | 22, 23 | NA         |
| 3   | SRC_3 Output Enable<br>1 = Enabled, 0 = Disabled (Hi-Z)         | RW   | 1 = Enabled        | SRC_3              | 24, 25 | NA         |
| 4   | SRC_4 Output Enable<br>1 = Enabled, 0 = Disabled (Hi-Z)         | RW   | 1 = Enabled        | SRC_4              | 26, 27 | NA         |
| 5   | SRC_5 Output Enable<br>1 = Enabled, 0 = Disabled (Hi-Z)         | RW   | 1 = Enabled        | SRC_5              | 30, 31 | NA         |
| 6   | SRC_6 Output Enable<br>1 = Enabled, 0 = Disabled (Hi-Z)         | RW   | 1 = Enabled        | SRC_6              | 32, 33 | NA         |
| 7   | CPU_2 / SRC_7 Output Enable<br>1 = Enabled, 0 = Disabled (Hi-Z) | RW   | 1 = Enabled        | CPU_2 / SRC_7      | 35, 36 | NA         |

**Data Byte 1: Control Register**

| Bit | Descriptions                                             | Type | Power Up Condition | Output(s) Affected                         | Pin                                                                                                           | Source Pin |
|-----|----------------------------------------------------------|------|--------------------|--------------------------------------------|---------------------------------------------------------------------------------------------------------------|------------|
| 0   | Spread Spectrum<br>1 = Enable, 0 = Disable               | RW   | 0 = Spread off     | CPU[0:2], SRC[0:7],<br>PCI[2:5], PCIF[0:1] | 3, 4, 5, 8, 9, 17,<br>18, 19, 20, 22, 23,<br>24, 25, 26, 27, 30,<br>31, 32, 33, 35, 36,<br>40, 41, 43, 44, 56 | NA         |
| 1   | CPU_0 output enable<br>1 = Enabled, 0 = Disabled (Hi-Z)  | RW   | 1 = Enabled        | CPU_0, CPU_0#                              | 43, 44                                                                                                        | NA         |
| 2   | CPU_1 output enable<br>1 = Enabled, 0 = Disabled (Hi-Z)  | RW   | 1 = Enabled        | CPU_1, CPU_1#                              | 40, 41                                                                                                        | NA         |
| 3   | Reserved                                                 | RW   |                    |                                            |                                                                                                               |            |
| 4   | REF Output Enable<br>1 = Enabled, 0 = Disabled           | RW   | 1 = Enabled        | REF                                        | 52                                                                                                            | NA         |
| 5   | USB_48 Output Enable<br>1 = Enabled, 0 = Disabled        | RW   | 1 = Enabled        | USB_48                                     | 12                                                                                                            | NA         |
| 6   | DOT_96 Output Enable<br>1 = Enabled, 0 = Disabled (Hi-Z) | RW   | 1 = Enabled        | DOT_96 & DOT96#                            | 14, 15                                                                                                        | NA         |
| 7   | PCIF_0 Output Enable<br>1 = Enabled, 0 = Disabled        | RW   | 1 = Enabled        | PCIF_O                                     | 8                                                                                                             | NA         |

**Data Byte 2: Control Register**

| Bit | Descriptions                                      | Type | Power Up Condition | Output(s) Affected | Pin | Source Pin |
|-----|---------------------------------------------------|------|--------------------|--------------------|-----|------------|
| 0   | PCIF_1 Output Enable<br>1 = Enabled, 0 = Disabled | RW   | 1 = Enabled        | PCIF_1             | 9   | NA         |
| 1   | Reserved                                          | RW   |                    |                    |     | NA         |
| 2   | Reserved                                          | RW   |                    |                    |     |            |
| 3   | Reserved                                          | RW   |                    |                    |     |            |
| 4   | PCI_2 Output Enable<br>1 = Enabled, 0 = Disabled  | RW   | 1 = Enabled        | PCI_2              | 56  | NA         |
| 5   | PCI_3 Output Enable<br>1 = Enabled, 0 = Disabled  | RW   | 1 = Enabled        | PCI_3              | 3   | NA         |
| 6   | PCI_4 Output Enable<br>1 = Enabled, 0 = Disabled  | RW   | 1 = Enabled        | PCI_4              | 4   | NA         |
| 7   | PCI_5 Output Enable<br>1 = Enabled, 0 = Disabled  | RW   | 1 = Enabled        | PCI_5              | 5   | NA         |

**Data Byte 3: Control Register**

| Bit | Descriptions                                                            | Type | Power Up Condition                                | Output(s) Affected | Pin    | Source Pin |
|-----|-------------------------------------------------------------------------|------|---------------------------------------------------|--------------------|--------|------------|
| 0   | SRC_0 Output Control<br>0 = Free Running,<br>1 = Stopped with PCI_STOP# | RW   | 0 = Free running,<br>not affected by<br>PCI_STOP# | SRC_0              | 17, 18 | NA         |
| 1   | SRC_1 Output Control<br>0 = Free Running,<br>1 = Stopped with PCI_STOP# | RW   | 0 = Free running,<br>not affected by<br>PCI_STOP# | SRC_1              | 19, 20 | NA         |
| 2   | SRC_2 Output Control<br>0 = Free Running,<br>1 = Stopped with PCI_STOP# | RW   | 0 = Free running,<br>not affected by<br>PCI_STOP# | SRC_2              | 22, 23 | NA         |
| 3   | SRC_3 Output Control<br>0 = Free Running,<br>1 = Stopped with PCI_STOP# | RW   | 0 = Free running,<br>not affected by<br>PCI_STOP# | SRC_3              | 24, 25 | NA         |
| 4   | SRC_4 Output Control<br>0 = Free Running,<br>1 = Stopped with PCI_STOP# | RW   | 0 = Free running,<br>not affected by<br>PCI_STOP# | SRC_4              | 26, 27 | NA         |
| 5   | SRC_5 Output Control<br>0 = Free Running,<br>1 = Stopped with PCI_STOP# | RW   | 0 = Free running,<br>not affected by<br>PCI_STOP# | SRC_5              | 30, 31 | NA         |
| 6   | SRC_6 Output Control<br>0 = Free Running,<br>1 = Stopped with PCI_STOP# | RW   | 0 = Free running,<br>not affected by<br>PCI_STOP# | SRC_6              | 32, 33 | NA         |
| 7   | SRC_7 Output Control<br>0 = Free Running,<br>1 = Stopped with PCI_STOP# | RW   | 0 = Free running,<br>not affected by<br>PCI_STOP# | SRC_7              | 35, 36 | NA         |

**Data Byte 4: Control Register**

| Bit | Descriptions                                                             | Type | Power Up Condition                             | Output(s) Affected | Pin    | Source Pin |
|-----|--------------------------------------------------------------------------|------|------------------------------------------------|--------------------|--------|------------|
| 0   | CPU_0 Output Control<br>0 = Free Running,<br>1 = Stopped with CPU_STOP#  | RW   | 1 = Stopped with CPU_STOP# assertion           | CPU_0              | 43, 44 | NA         |
| 1   | CPU_1 Output Control<br>0 = Free Running,<br>1 = Stopped with CPU_STOP#  | RW   | 1 = Stopped with CPU_STOP# assertion           | CPU_1              | 40, 41 | NA         |
| 2   | CPU_2 Output Control<br>0 = Free Running,<br>1 = Stopped with CPU_STOP#  | RW   | 1 = Stopped with CPU_STOP# assertion           | CPU_2              | 35, 36 | NA         |
| 3   | PCIF_0 Output Control<br>0 = Free Running,<br>1 = Stopped with PCI_STOP# | RW   | 0 = Free running,<br>not affected by PCI_STOP# | PCIF_0             | 8      | NA         |
| 4   | PCIF_1 Output Control<br>0 = Free Running,<br>1 = Stopped with PCI_STOP# | RW   | 0 = Free running,<br>not affected by PCI_STOP# | PCIF_1             | 9      | NA         |
| 5   | Reserved                                                                 | RW   |                                                |                    |        |            |
| 6   | DOT_Pwrdown drive mode<br>1 = Hi-Z, 0 = Driven in Pwrdown                | RW   | 0 = Driven in power down                       | DOT_96 & DOT_96#   | 14, 15 | NA         |
| 7   | Reserved                                                                 | RW   |                                                |                    |        |            |

**Data Byte 5: Control Register**

| Bit | Descriptions                                                | Type | Power Up Condition       | Output(s) Affected   | Pin                                                            | Source Pin |
|-----|-------------------------------------------------------------|------|--------------------------|----------------------|----------------------------------------------------------------|------------|
| 0   | CPU_0 Pwrdown drive mode<br>1 = Hi-Z, 0 = Driven in Pwrdown | RW   | 0 = Driven in power down | CPU_0 & CPU_0#       | 43, 44                                                         | NA         |
| 1   | CPU_1 Pwrdown drive mode<br>1 = Hi-Z, 0 = Driven in Pwrdown | RW   | 0 = Driven in power down | CPU_1 & CPU_1#       | 40, 41                                                         | NA         |
| 2   | CPU_2 Pwrdown drive mode<br>1 = Hi-Z, 0 = Driven in Pwrdown | RW   | 0 = Driven in power down | CPU_2 & CPU_2#       | 35, 36                                                         | NA         |
| 3   | SRC_Pwrdown drive mode<br>1 = Hi-Z, 0 = Driven in Pwrdown   | RW   | 0 = Driven in power down | SRC[0:7] & SRC[0:7]# | 17, 18, 19, 20, 22, 23, 24, 25, 26, 27, 30, 31, 32, 35, 36     | NA         |
| 4   | CPU_0 Stop drive mode<br>1 = Hi-Z, 0 = Driven in CPU Stop   | RW   | 0 = Driven in CPU_STOP   | CPU_0 & CPU_0#       | 43, 44                                                         | NA         |
| 5   | CPU_1 Stop drive mode<br>1 = Hi-Z, 0 = Driven in CPU Stop   | RW   | 0 = Driven in CPU_STOP   | CPU_1 & CPU_1#       | 40, 41                                                         | NA         |
| 6   | CPU_2 Stop drive mode<br>1 = Hi-Z, 0 = Driven in CPU Stop   | RW   | 0 = Driven in CPU_STOP   | CPU_2 & CPU_2#       | 35, 36                                                         | NA         |
| 7   | SRC_Stop drive mode<br>1 = Hi-Z, 0 = Driven in PCI Stop     | RW   | 0 = Driven in PCI_STOP   | SRC[0:7] & SRC[0:7]# | 17, 18, 19, 20, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 35, 36 | NA         |

**Data Byte 6: Control Register**

| Bit | Descriptions                                                                                                | Type | Power Up Condition  | Output(s) Affected                                                  | Pin                                                                                                               | Source Pin |
|-----|-------------------------------------------------------------------------------------------------------------|------|---------------------|---------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|------------|
| 0   | FS_A Reflects the value of the FS_A pin sampled on power up<br>0 = FS_A was low during Vtt_Pwrgd# assertion | R    | Externally Selected | CPU[0:2]                                                            | 35, 36, 40, 41, 43, 44                                                                                            | NA         |
| 1   | FS_B Reflects the value of the FS_B pin sampled on power up<br>0 = FS_B was low during Vtt_Pwrgd# assertion | R    | Externally Selected | CPU[0:2]                                                            | 35, 36, 40, 41, 43, 44                                                                                            | NA         |
| 2   | FS_C Reflects the value of the FS_C pin sampled on power up<br>0 = FS_C was low during Vtt_Pwrgd# assertion | R    | Externally Selected | CPU[0:2]                                                            | 35, 36, 40, 41, 43, 44                                                                                            | NA         |
| 3   | PCI_Stop control<br>1 = Disabled,<br>0 = Enabled, Stopped SRC and PCI clocks                                | RW   | 1 = Disabled        | All PCI & SRC clocks except PCIF and SRC clocks set to free-running | 3, 4, 5, 17, 18, 19, 20, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 35, 36, 56                                       | NA         |
| 4   | REF Output Drive Strength<br>0 = 1x, 1 = 2x                                                                 | RW   | 1 = 2X              | REF                                                                 | 52                                                                                                                | NA         |
| 5   | Reserved                                                                                                    | RW   |                     |                                                                     |                                                                                                                   |            |
| 6   | Test Clock Mode Entry Control<br>0 = Disabled, 1 = REF/N or Hi-Z                                            | RW   | 0 = Disabled        |                                                                     |                                                                                                                   |            |
| 7   | Test Clock Mode<br>0 = Hi-Z, 1 = REF/N                                                                      | RW   | 0 = Hi-Z            | CPU[0:2], SRC[0:7], PCI[2:5], PCIF[0:1], REF, USB_48, DOT_96        | 3, 4, 5, 8, 9, 12, 14, 15, 17, 18, 19, 20, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 35, 36, 40, 41, 43, 44, 52, 56 | NA         |

**DataByte 7: Control Register**

| Bit | Descriptions  | Type | Power Up Condition | Output(s) Affected | Pin |
|-----|---------------|------|--------------------|--------------------|-----|
| 0   | Vendor ID     | R    | 0                  | NA                 | NA  |
| 1   |               | R    | 0                  | NA                 | NA  |
| 2   |               | R    | 0                  | NA                 | NA  |
| 3   |               | R    | 0                  | NA                 | NA  |
| 4   | Revision Code | R    | 1                  | NA                 | NA  |
| 5   |               | R    | 0                  | NA                 | NA  |
| 6   |               | R    | 1                  | NA                 | NA  |
| 7   |               | R    | 0                  | NA                 | NA  |



### Vtt\_Pwrgd# Timing Diagram

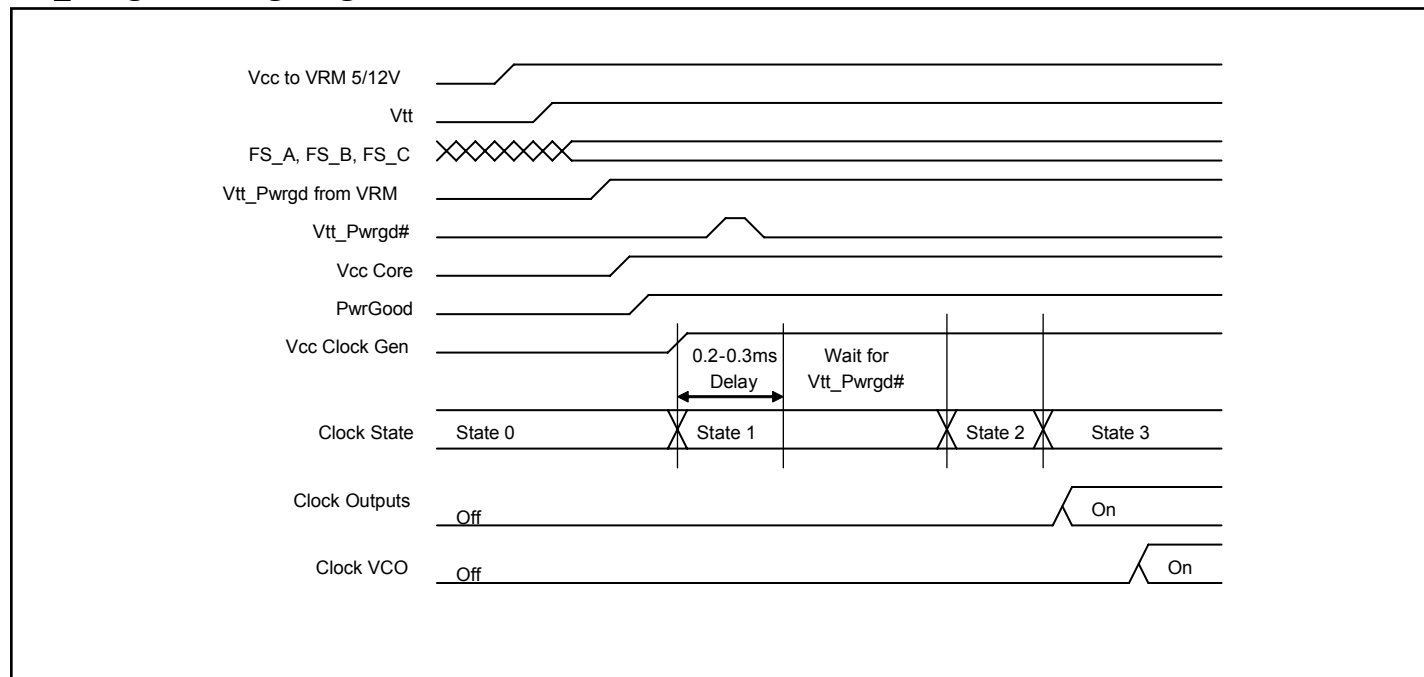


Figure 1. CPU power BEFORE clock power

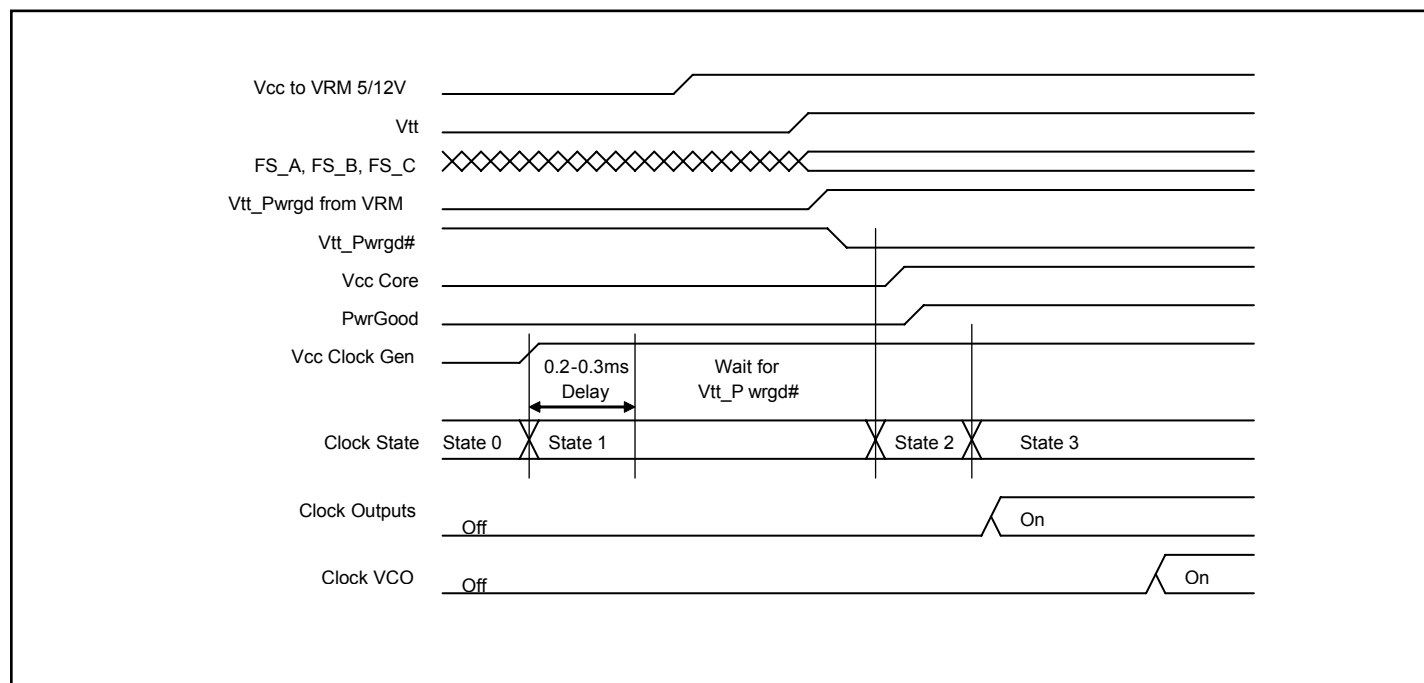


Figure 2. CPU power AFTER clock power

### Clock Power-Up State Machine

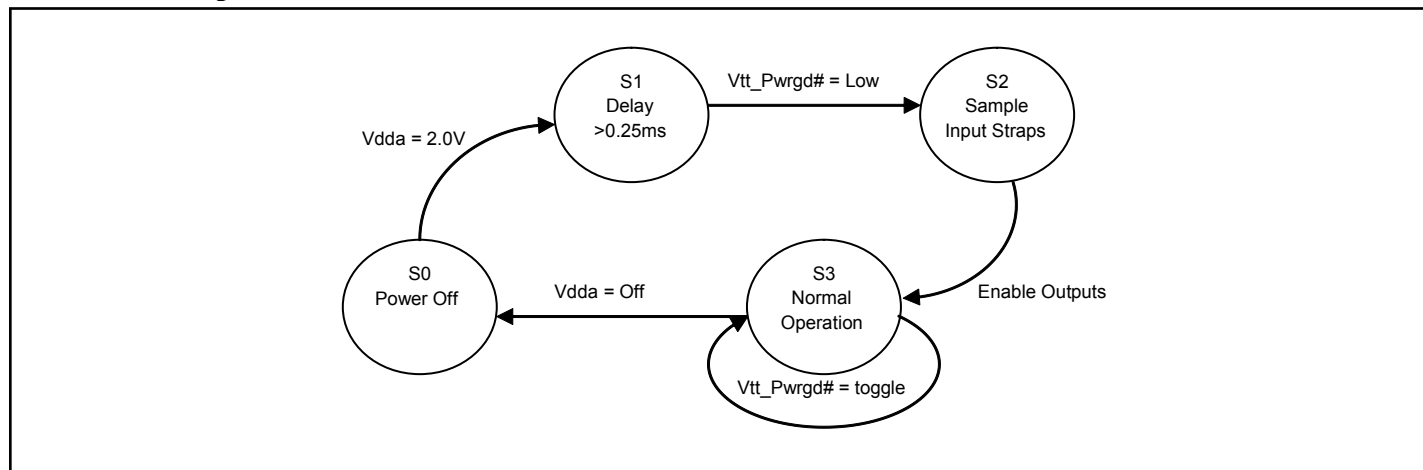


Figure 3. Power-Up State Diagram

### Power Down (PWRDWN assertion)

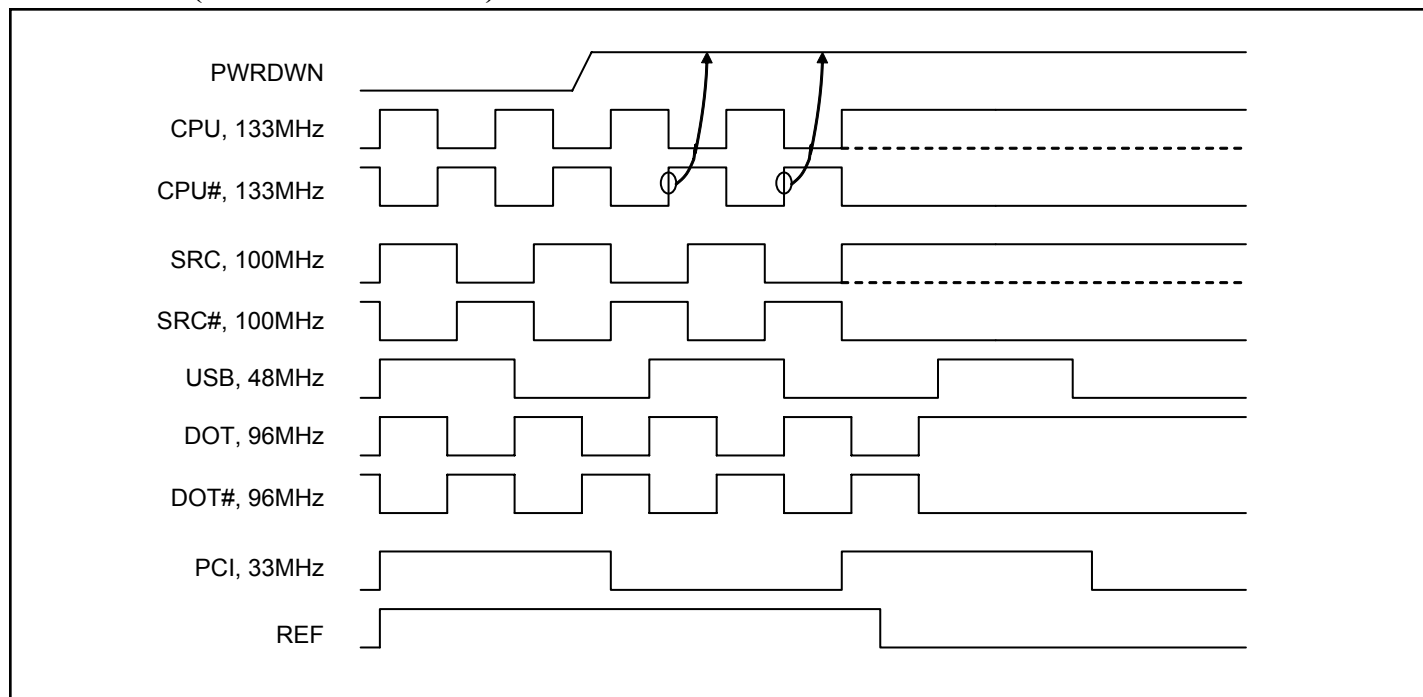


Figure 4. Power down sequence

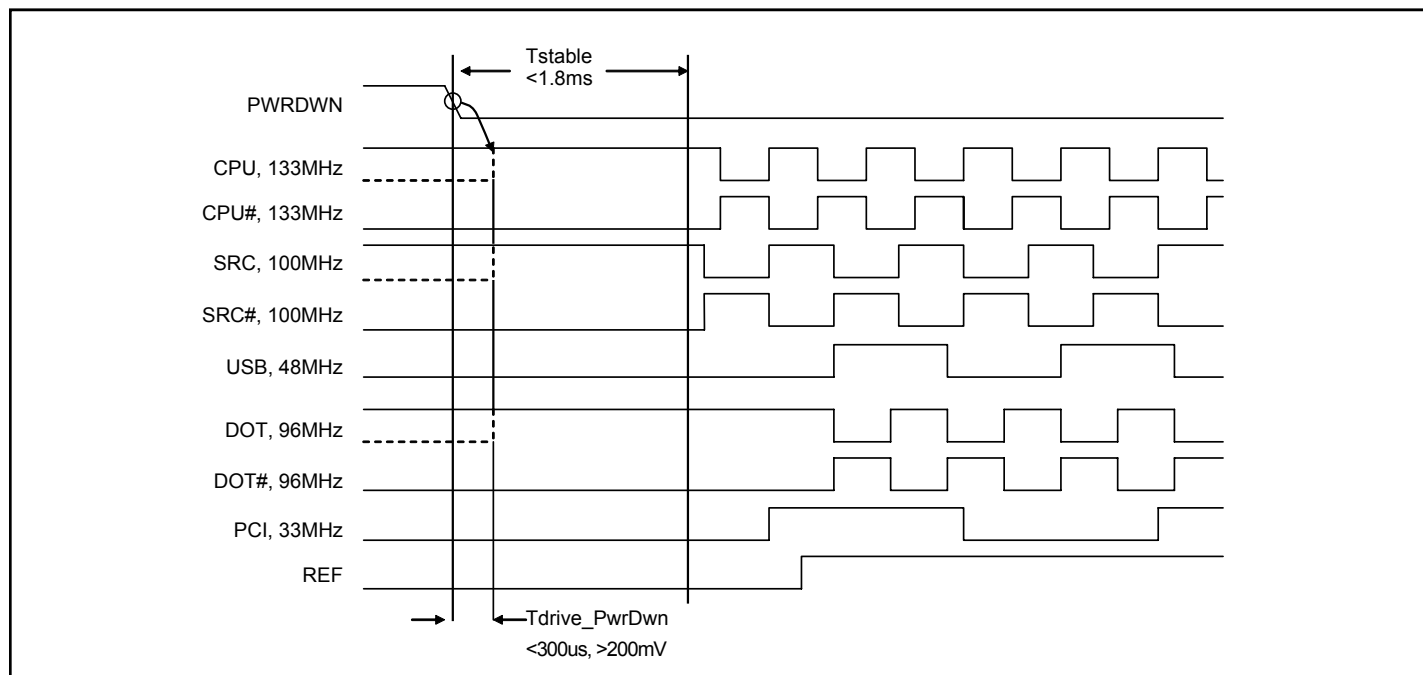
**Power Down (PWRDWN De-assertion)**


Figure 5. Power down de-assertion

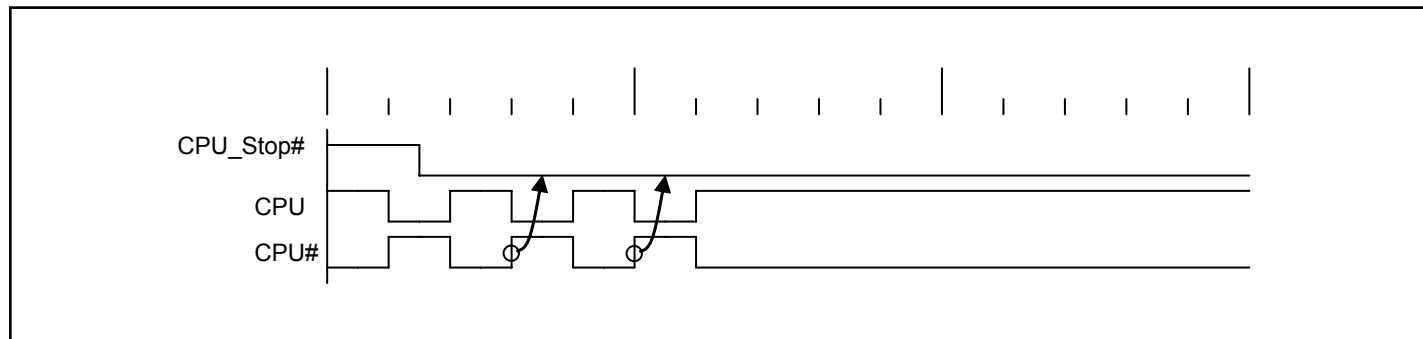
**CPU STOP (CPU\_STOP# assertion)**


Figure 6. Assertion of CPU\_Stop# Waveforms

### CPU STOP (CPU\_STOP# De-assertion)

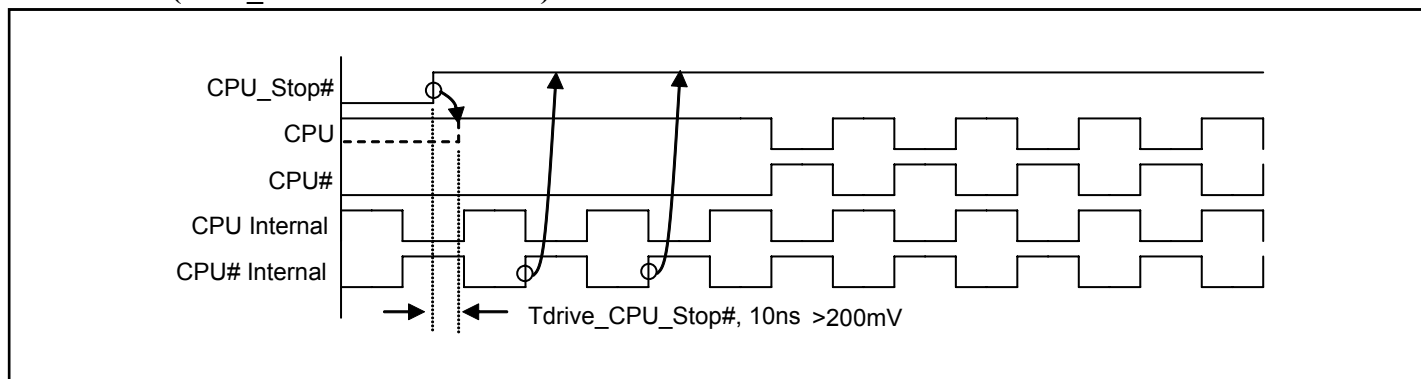


Figure 7. CPU\_STOP# De-assertion Waveform

### PCI STOP (PCI\_STOP# assertion)

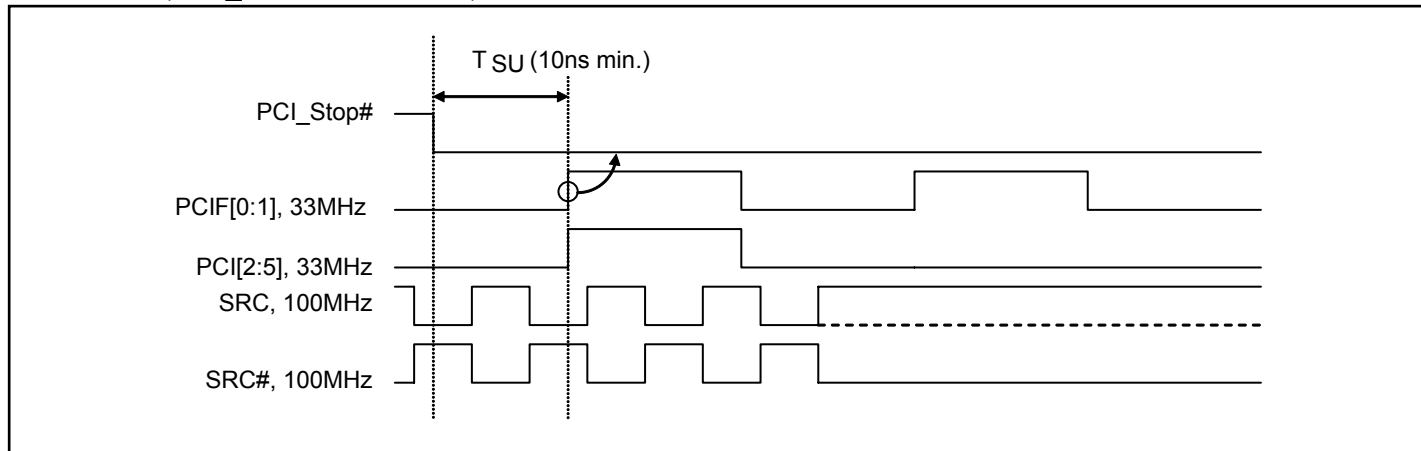


Figure 8. Assertion of PCI\_STOP# Waveform

### PCI STOP (PCI\_STOP# De-assertion)

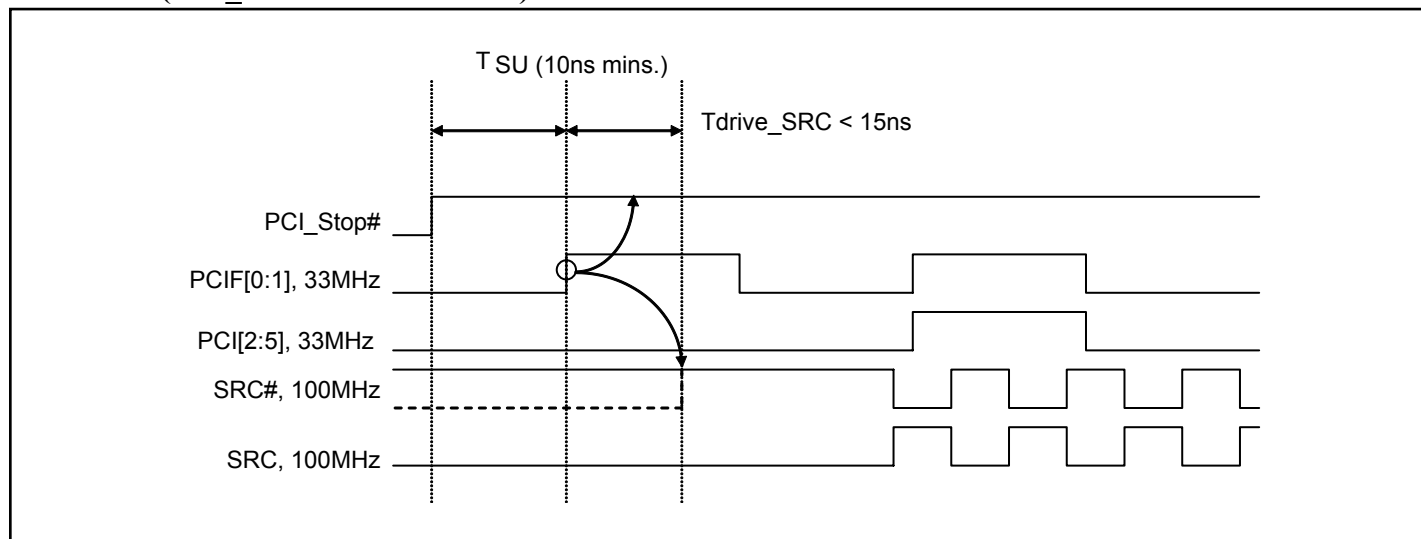


Figure 8. De-assertion of PCI\_STOP# Waveform

## Tristate Specifications

### CPU Tristate clock truth table

| Signal   | Pwrdsn | CPU_STOP# | CPU_Stop<br>Tristate Bit | Pwrdsn<br>Tristate Bit | Non-stop          | Stoppable         |
|----------|--------|-----------|--------------------------|------------------------|-------------------|-------------------|
|          | pin    | pin       |                          |                        | Outputs           | Outputs           |
| CPU[0:2] | 0      | 1         | X                        | X                      | Running           | Running           |
|          | 0      | 0         | 0                        | X                      | Running           | Driven @ Iref x 6 |
|          | 0      | 0         | 1                        | X                      | Running           | Tristate          |
|          | 1      | X         | X                        | 0                      | Driven @ Iref x 2 | Driven @ Iref x 2 |
|          | 1      | X         | X                        | 1                      | Tristate          | Tristate          |

### SRC Tristate clock truth table

| Signal   | Pwrdsn | PCI_STOP# | PCI_Stop<br>Tristate Bit | Pwrdsn<br>Tristate Bit | Non-stop          | Stoppable         |
|----------|--------|-----------|--------------------------|------------------------|-------------------|-------------------|
|          | pin    | pin       |                          |                        | Outputs           | Outputs           |
| SRC[0:7] | 0      | 1         | X                        | X                      | Running           | Running           |
|          | 0      | 0         | 0                        | X                      | Running           | Driven @ Iref x 6 |
|          | 0      | 0         | 1                        | X                      | Running           | Tristate          |
|          | 1      | X         | X                        | 0                      | Driven @ Iref x 2 | Driven @ Iref x 2 |
|          | 1      | X         | X                        | 1                      | Tristate          | Tristate          |

### DOT Tristate clock truth table

| Signal | Pwrdsn | Pwrdsn Tristate Bit | Stoppable         |
|--------|--------|---------------------|-------------------|
|        | pin    |                     | Outputs           |
| DOT96  | 0      | X                   | Running           |
|        | 1      | 0                   | Driven @ Iref x 2 |
|        | 1      | 1                   | Tristate          |

### CPU Clock Tristate Timing

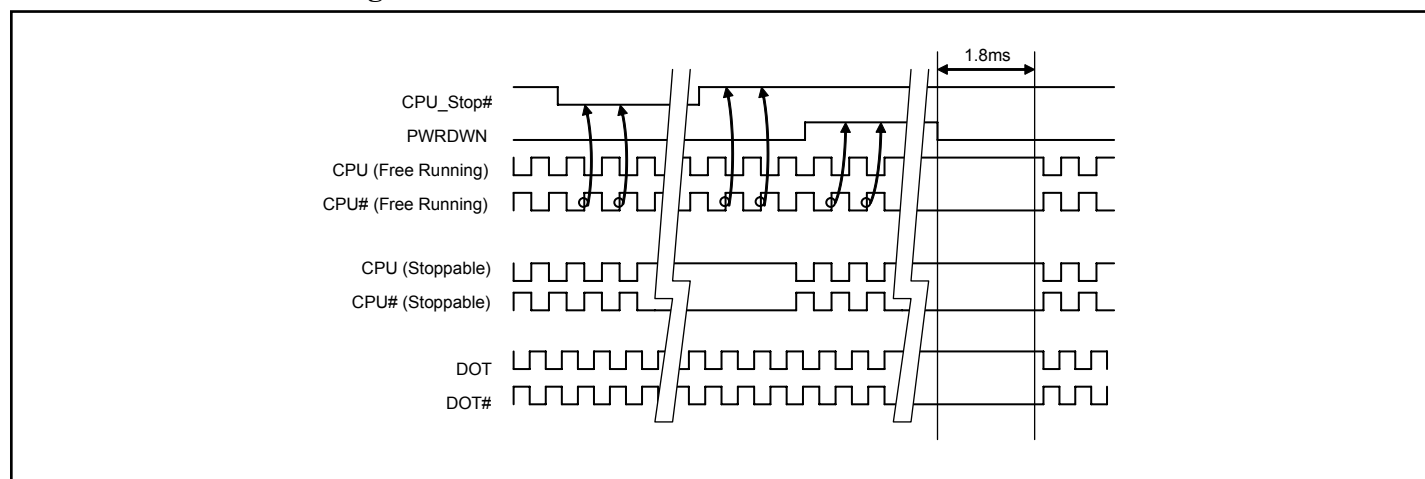


Figure 10. CPU\_STOP = Driven, CPU\_PWRDWN = Driven, DOT\_PWRDWN = Driven

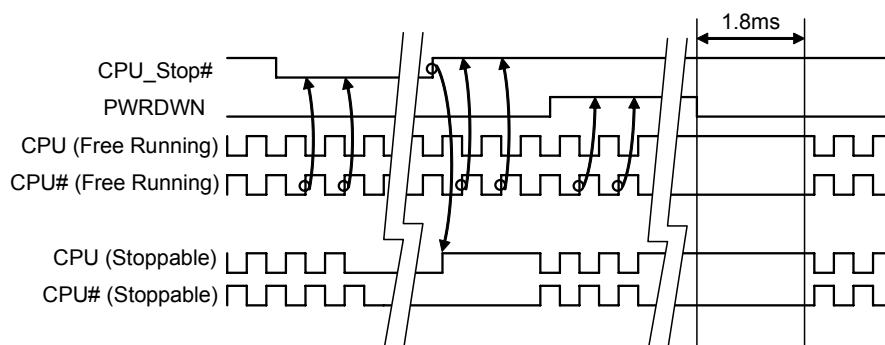


Figure 11. CPU\_Stop = Tristate, CPU\_PWRDWN = Driven

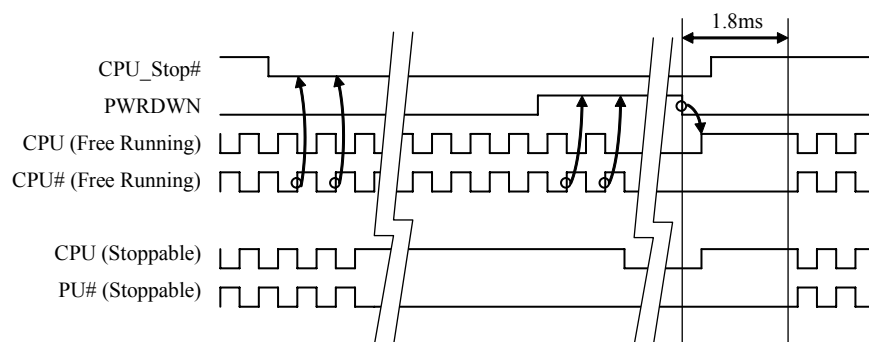


Figure 12. CPU\_Stop = Driven, CPU\_PWRDWN = Tristate

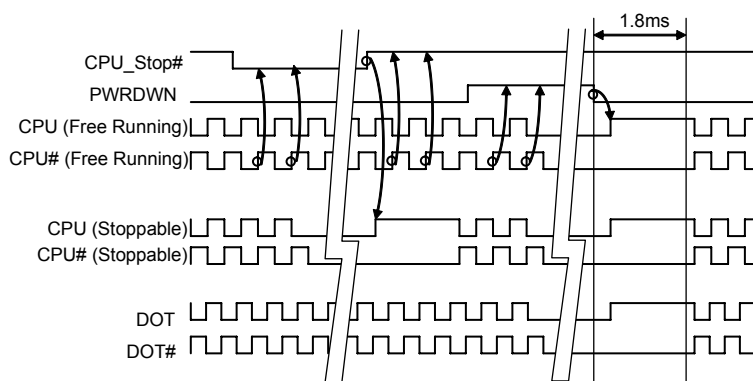


Figure 13. CPU\_STOP = Tristate, CPU\_PWRDWN = Tristate, DOT\_PWRDWN = Tristate

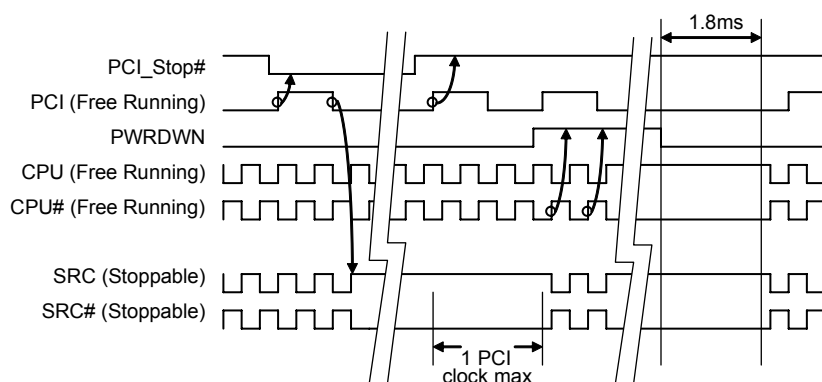


Figure 14. SRC\_Stop = Driven, SRC\_PWRDWN = Driven

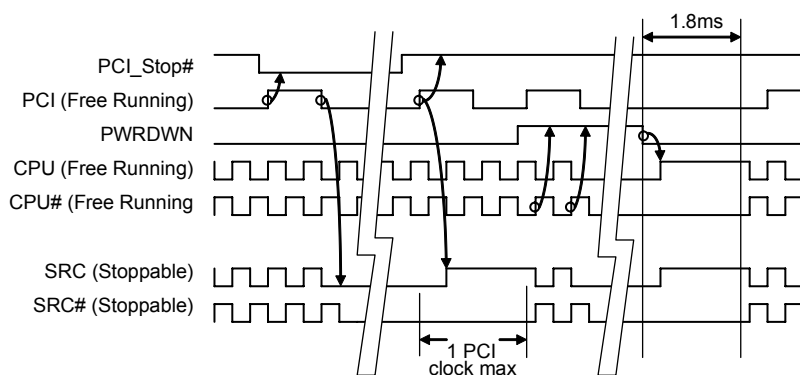


Figure 15. SRC\_Stop = Tristate, SRC\_PWRDWN = Tristate

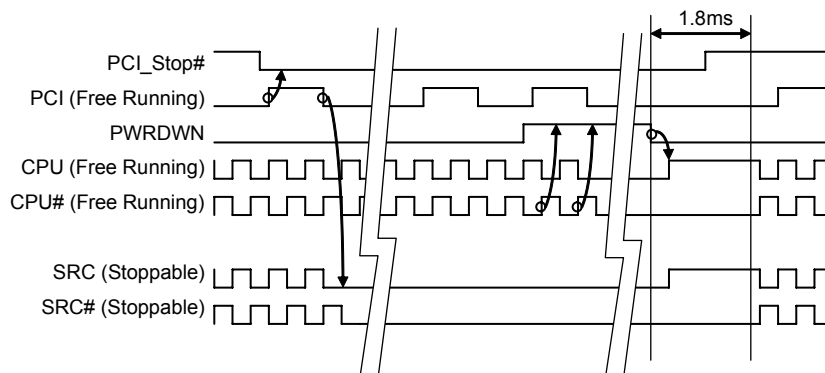


Figure 16. SRC\_STOP = Tristate, SRC\_PWRDWN = Tristate, PCI\_STOP# = Asserted

### Spread Spectrum Specifications

PI6C410M supports Spread Spectrum clocking and can be enabled and disabled via SMBus control. The maximum Spread Spectrum Modulation is  $-0.5\%$  down spread with frequency from 30KHz to 33KHz.

| SSC ON                  | Tperiod |         | SSC OFF                 | Tperiod |        | Unit |
|-------------------------|---------|---------|-------------------------|---------|--------|------|
|                         | Min     | Max     |                         | Min     | Max    |      |
| CPU @ 399.000 MHz       | 2.4993  | 2.5133  | CPU @ 400.000 MHz       | 2.4993  | 2.5008 | ns   |
| CPU @ 332.500 MHz       | 2.9991  | 3.016   | CPU @ 333.333 MHz       | 2.9991  | 3.0009 |      |
| CPU @ 266.000 MHz       | 3.7489  | 3.77    | CPU @ 266.666 MHz       | 3.7489  | 3.7511 |      |
| CPU @ 199.500 MHz       | 4.9985  | 5.0266  | CPU @ 200.000 MHz       | 4.9985  | 5.0015 |      |
| CPU @ 166.250 MHz       | 5.9982  | 6.032   | CPU @ 166.666 MHz       | 5.9982  | 6.0018 |      |
| CPU @ 133.000 MHz       | 7.4978  | 7.54    | CPU @ 133.333 MHz       | 7.4978  | 7.5023 |      |
| CPU @ 99.750 MHz        | 9.997   | 10.0533 | CPU @ 100.000 MHz       | 9.997   | 10.003 |      |
|                         |         |         |                         |         |        |      |
| SRC @ 99.750 MHz        | 9.997   | 10.0533 | SRC @ 100.000 MHz       | 9.997   | 10.003 |      |
|                         |         |         |                         |         |        |      |
| PCIF / PCI @ 33.250 MHz | 29.991  | 30.1598 | PCIF / PCI @ 33.333 MHz | 29.991  | 30.009 |      |

### Current-mode output buffer characteristics of CPU, SRC, and DOT

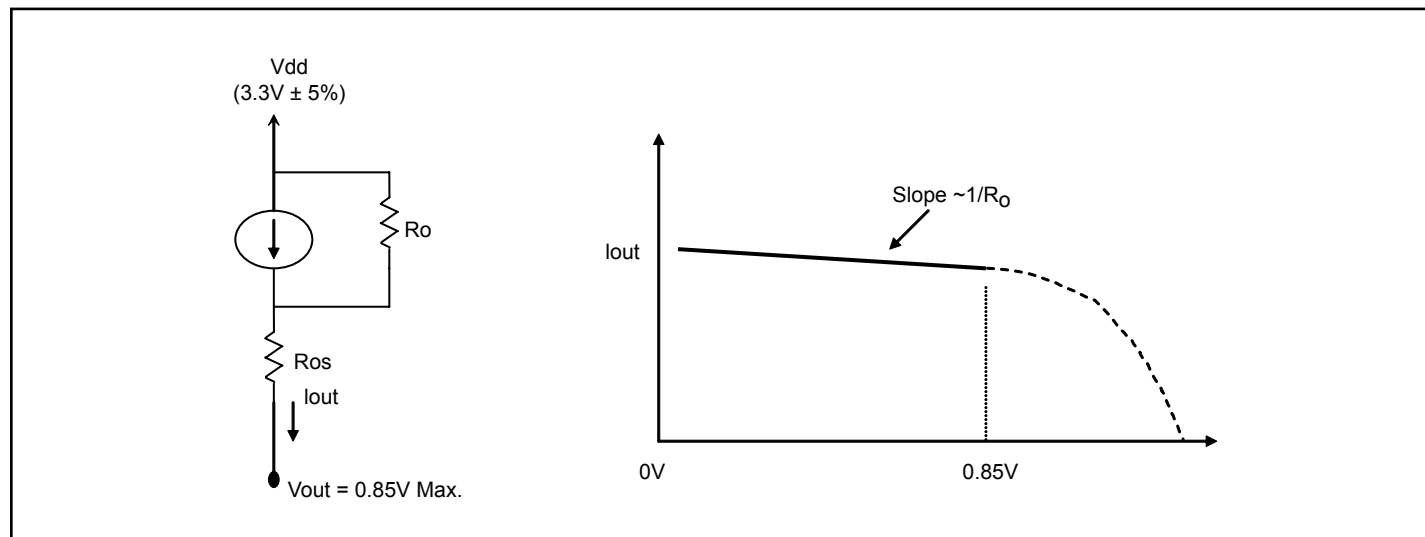


Figure 17. Simplified diagram of a current-mode output buffer

### Host Clock Buffer Characteristics

|           | Min           | Max         |
|-----------|---------------|-------------|
| $R_O$     | 3000 $\Omega$ | N/A         |
| $R_{OS}$  | unspecified   | unspecified |
| $V_{OUT}$ | N/A           | 850mV       |



**Cueernt Accuracy**

|                  | Conditions                 | Configuration | Load                                      | Min.                        | Max.                        |
|------------------|----------------------------|---------------|-------------------------------------------|-----------------------------|-----------------------------|
| I <sub>OUT</sub> | V <sub>DD</sub> = 3.30 ±5% | Rref = 475Ω   | Nominal test load for given configuration | -12% x I <sub>NOMINAL</sub> | +12% x I <sub>NOMINAL</sub> |
|                  |                            | Iref = 2.32mA |                                           |                             |                             |

**Host Clock Output Current**

| Board Target Trace/Term Z                       | Reference R, Iref = V <sub>DD</sub> /(3xRr) | Output Current | Voh @ Z   |
|-------------------------------------------------|---------------------------------------------|----------------|-----------|
| 100Ω<br>(100Ω differential ≈ 8% coupling ratio) | Rref = 475 Ω<br>Iref = 2.32mA               | Ioh = 6 x Iref | 0.7V @ 50 |

**Crystal Recommendations<sup>(1)</sup>**

| Frequency    | Cut | Loading  | Load Cap | Drive Max. | Shunt Cap Max. | Motional Cap Max. | Tolerance Max. | Stability Max. | Aging Max. |
|--------------|-----|----------|----------|------------|----------------|-------------------|----------------|----------------|------------|
| 14.31818 MHz | AT  | Parallel | 20pF     | 0.1mW      | 5pF            | 0.016pF           | 35ppm          | 30ppm          | 5ppm       |

**Note:**

- External trim capacitors (Ce) are required.  $C_e = 2 \cdot CL - (C_s + C_i)$ . Typical Ce = 33pF when Crystal-load = 20pF, Ctrace (Cs) = 2.8pF and CXTAL = 4.5pF.

**Absolute Maximum Ratings<sup>(1)</sup>** (Over operating free-air temperature range)

| Symbol            | Parameters               | Min. | Max. | Units |
|-------------------|--------------------------|------|------|-------|
| V <sub>DD_A</sub> | 3.3V Core Supply Voltage | -0.5 | 4.6  | V     |
| V <sub>DD</sub>   | 3.3V I/O Supply Voltage  | -0.5 | 4.6  |       |
| V <sub>IH</sub>   | Input High Voltage       |      | 4.6  |       |
| V <sub>IL</sub>   | Input Low Voltage        | -0.5 |      |       |
| Ts                | Storage Temperature      | -65  | 150  | °C    |
| V <sub>ESD</sub>  | ESD Protection           | 2000 |      | V     |

**Note:**

- Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

**DC Electrical Characteristics** ( $V_{DD} = 3.3 \pm 5\%$ ,  $V_{DD\_A} = 3.3 \pm 5\%$ )

| Symbol             | Parameters               | Condition                                                                            | Min.                     | Max.                  | Units |
|--------------------|--------------------------|--------------------------------------------------------------------------------------|--------------------------|-----------------------|-------|
| VDD_A              | 3.3V Core Supply Voltage |                                                                                      | 3.135                    | 3.465                 | V     |
| VDD                | 3.3V I/O Supply Voltage  |                                                                                      | 3.135                    | 3.465                 |       |
| V <sub>IH</sub>    | 3.3V Input High Voltage  | V <sub>DD</sub>                                                                      | 2.0                      | V <sub>DD</sub> + 0.3 |       |
| V <sub>IL</sub>    | 3.3V Input Low Voltage   |                                                                                      | V <sub>SS</sub> - 0.3    | 0.8                   |       |
| I <sub>IK</sub>    | Input Leakage Current    | 0 < V <sub>IN</sub> < V <sub>DD</sub>                                                | -5                       | +5                    | μA    |
| V <sub>IH_FS</sub> | 3.3V Input High Voltage  |                                                                                      | 0.7                      | V <sub>DD</sub> + 0.3 | V     |
| V <sub>IL_FS</sub> | 3.3V Input Low Voltage   |                                                                                      | V <sub>SS</sub> - 0.3    | 0.35                  |       |
| V <sub>OH</sub>    | 3.3V Output High Voltage | I <sub>OH</sub> = -1mA                                                               | 2.4                      |                       |       |
| V <sub>OL</sub>    | 3.3V Output Low Voltage  | I <sub>OL</sub> = 1mA                                                                |                          | 0.4                   |       |
| I <sub>OH</sub>    | Output High Current      | CPU, SRC, DOT: I <sub>OH</sub> = 6 x I <sub>ref</sub> ,<br>I <sub>ref</sub> = 2.32mA | 12.2                     |                       | mA    |
|                    |                          |                                                                                      |                          | 15.6                  |       |
|                    |                          | USB                                                                                  | V <sub>OH</sub> = 1.0V   | -29                   |       |
|                    |                          |                                                                                      | V <sub>OH</sub> = 3.135V | -23                   |       |
|                    |                          | REF, PCI                                                                             | V <sub>OH</sub> = 1.0V   | -33                   |       |
|                    |                          |                                                                                      | V <sub>OH</sub> = 3.135V | -33                   |       |
| I <sub>OL</sub>    | Output Low Current       | USB                                                                                  | V <sub>OL</sub> = 1.95V  | 29                    |       |
|                    |                          |                                                                                      | V <sub>OL</sub> = 0.4V   | 27                    |       |
|                    |                          | REF, PCI                                                                             | V <sub>OL</sub> = 1.95V  | 30                    |       |
|                    |                          |                                                                                      | V <sub>OL</sub> = 0.4V   | 38                    |       |
| C <sub>in</sub>    | Input Pin Capacitance    |                                                                                      | 3                        | 5                     | pF    |
| C <sub>xtal</sub>  | Xtal Pin Capacitance     |                                                                                      | 3                        | 6                     |       |
| C <sub>out</sub>   | Output Pin Capacitance   |                                                                                      |                          | 6                     |       |
| L <sub>pin</sub>   | Pin Inductance           |                                                                                      |                          | 7                     | nH    |
| I <sub>DD</sub>    | Power Supply Current     | V <sub>DD</sub> = 3.465V, F <sub>CPU</sub> = 400 MHz                                 |                          | 500                   | mA    |
| I <sub>SS</sub>    | Power Down Current       | Driven outputs                                                                       |                          | 100                   |       |
| I <sub>SS</sub>    | Power Down Current       | Tristate outputs                                                                     |                          | 12                    |       |
| T <sub>a</sub>     | Ambient Temperature      |                                                                                      | 0                        | 70                    | °C    |

**AC Electrical Characteristics** ( $V_{DD} = 3.3 \pm 5\%$ ,  $V_{DD\_A} = 3.3 \pm 5\%$ )

| Symbol                                  | Outputs            | Parameters                                                | Min. | Max. | Units | Notes |   |
|-----------------------------------------|--------------------|-----------------------------------------------------------|------|------|-------|-------|---|
| T <sub>rise</sub> / T <sub>fall</sub>   | CPU, SRC, DOT      | Rise and fall Time<br>(measured between 0.175V to 0.525V) | 175  | 700  | ps    | 1,2   |   |
| T <sub>rise</sub> / T <sub>fall</sub>   | PCI/PCIF, REF      | Rise and fall Time<br>(measured between 0.8V to 2.0V)     | 0.5  | 2.0  | ns    | 4     |   |
| T <sub>rise</sub> / T <sub>fall</sub>   | USB                | Rise and fall Time<br>(measured between 0.8V to 2.0V)     | 1.0  | 2.0  |       | 5     |   |
| ΔT <sub>rise</sub> / ΔT <sub>fall</sub> | CPU, SRC, DOT      | Rise and fall Time Variation                              |      | 125  | ps    | 1, 2  |   |
| T <sub>skew</sub>                       | CPU0, CPU1         | CPU – CPU Skew                                            |      | 100  | ps    | 1,3,6 |   |
| T <sub>skew</sub>                       | CPU2               | CPU – CPU Skew                                            |      | 200  |       |       |   |
| T <sub>skew</sub>                       | SRC                | SRC – SRC Skew                                            |      | 250  |       |       |   |
| T <sub>skew</sub>                       | PCI/PCIF, REF      | PCI – PCI Skew / REF - REF Skew (measured at 1.5V)        |      | 500  |       | 4     |   |
| T <sub>jitter</sub>                     | CPU0, CPU1         | Cycle – Cycle Jitter                                      |      | 85   |       | 1, 3  |   |
| T <sub>jitter</sub>                     | CPU2               | Cycle – Cycle Jitter                                      |      | 125  |       |       |   |
| T <sub>jitter</sub>                     | SRC                | Cycle – Cycle Jitter                                      |      | 125  |       |       |   |
| T <sub>jitter</sub>                     | DOT                | Cycle – Cycle Jitter                                      |      | 250  |       |       |   |
| T <sub>jitter</sub>                     | PCI/PCIF           | Cycle – Cycle Jitter (measured at 1.5V)                   |      | 500  |       |       | 4 |
| T <sub>jitter</sub>                     | USB                | Cycle – Cycle Jitter (measured at 1.5V)                   |      | 350  |       |       | 5 |
| T <sub>jitter</sub>                     | REF                | Cycle – Cycle Jitter (measured at 1.5V)                   |      | 1000 |       | 4     |   |
| V <sub>HIGH</sub>                       | CPU, SRC, DOT      | Voltage HIGH including overshoot                          | 660  | 1150 | mV    | 1, 2  |   |
| V <sub>LOW</sub>                        | CPU, SRC, DOT      | Voltage LOW including undershoot                          | -300 |      |       |       |   |
| V <sub>cross</sub>                      | CPU, SRC, DOT      | Absolute crossing poing voltages                          | 250  | 550  |       |       |   |
| ΔV <sub>cross</sub>                     | CPU, SRC, DOT      | Total variation of Vcross over all edges                  |      | 140  |       |       |   |
| T <sub>DC</sub>                         | CPU, SRC, DOT      | Duty-Cycle                                                | 45   | 55   | %     | 1,3,6 |   |
| T <sub>DC</sub>                         | REF, USB, PCI/PCIF | Duty-Cycle (measured at 1.5V)                             | 45   | 55   | %     | 4, 5  |   |
| T <sub>stable</sub>                     |                    | All clock stabilization from power-up                     |      | <1.8 | ms    | Fig 2 |   |
| T <sub>drive</sub>                      |                    | Differential output enable after PwrDwn de-assertion      |      | 300  | μs    |       |   |
| Pwrdwn                                  |                    |                                                           |      |      |       |       |   |
| T <sub>rise</sub> / T <sub>fall</sub>   |                    | Power down rise and fall time                             |      | 5.0  | ns    |       |   |
| Pwrdwn                                  |                    |                                                           |      |      |       |       |   |

**Notes:**

1. Test configuration is  $R_s = 33.2\Omega$ ,  $R_p = 49.9\Omega$ , and  $C_L = 2pF$ .
2. Single-Ended measurement.
3. Differential measurement.
4. PCI, PCIF, and REF  $C_L(\min) = 10pF$ ,  $C_L(\max) = 30pF$ .
5. USB  $C_L(\min) = 10pF$ ,  $C_L(\max) = 20pF$ .
6. CPU measured at 133 MHz.

### Configuration Test Load Board Termination

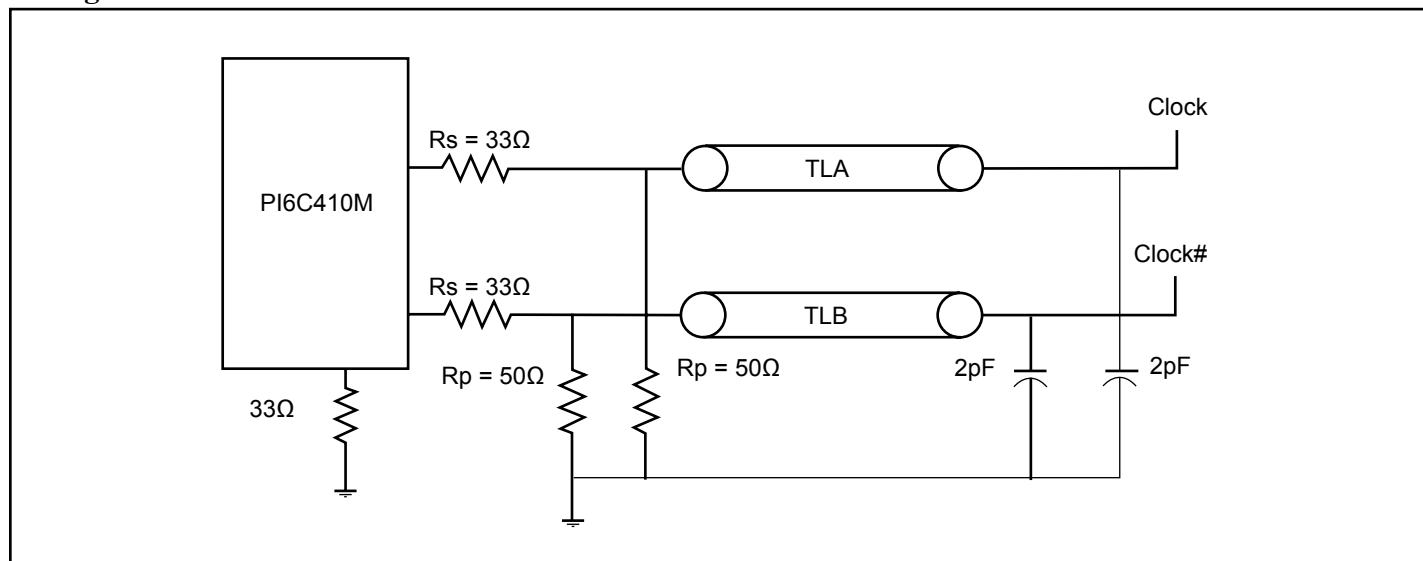
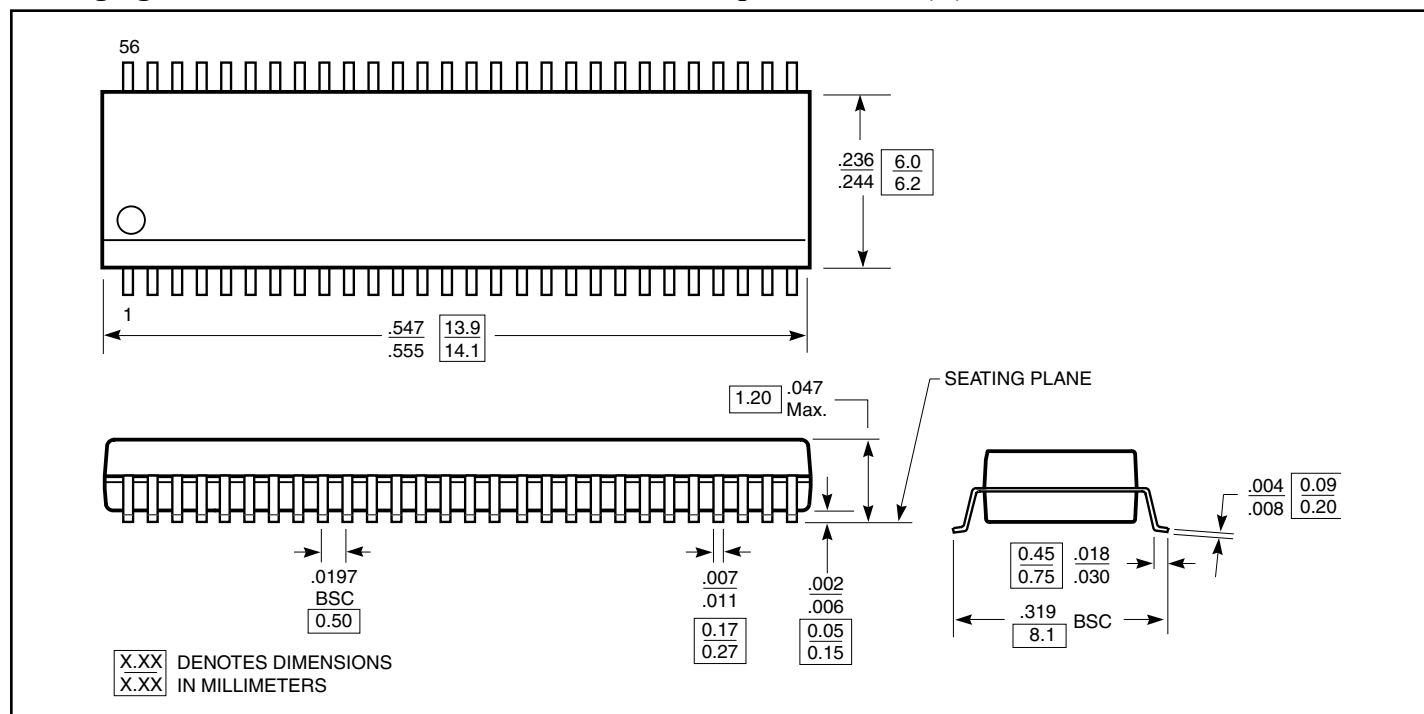


Figure 18. Configuration test load board termination

**Note:**

1. Maximum 10" trace length for CPU @ 200 MHz, 16" trace for SRC @ 100 MHz.

**Packaging Mechanical: 56-Pin, 240mil wide, 0.5mm pitch TSSOP (A)**

**Ordering Information<sup>(1,2,3)</sup>**

| Ordering Code | Package Code | Package Description                                                    |
|---------------|--------------|------------------------------------------------------------------------|
| PI6C410MA     | A            | 56-Pin, 240mil wide, 0.5mm pitch TSSOP                                 |
| PI6C410MAE    | A            | Pb-free & Green 56-Pin, 240mil wide, 0.5mm pitch TSSOP                 |
| PI6C410MAAE   | A            | Pb-free & Green 56-Pin, 240mil wide, 0.5mm pitch TSSOP                 |
| PI6C410MAAEX  | A            | Pb-free & Green 56-Pin, 240mil wide, 0.5mm pitch TSSOP , Tape and Reel |

**Notes:**

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
2. E = Pb-free and Green
3. X Suffix = Tape/Reel