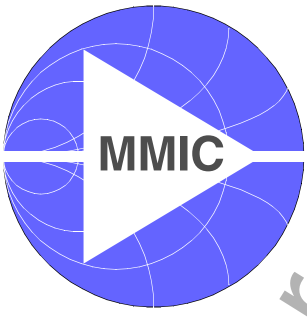
BGB550

Mirror Biased Transistor



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Silicon Discretes

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BGB550
Preliminary data sheet
Revision History: **2001-07-31** Preliminary

Previous Version:	2001-01-19
Page	Subjects (major changes since last revision)
all pages	Change from word to FrameMaker - complete reworked

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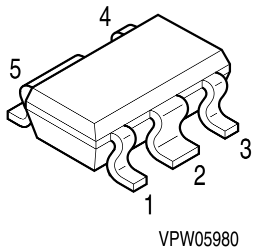
Preliminary

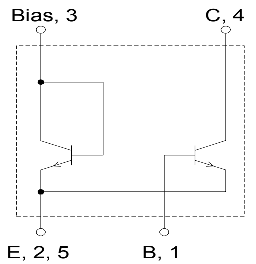
Mirror Biased Transistor

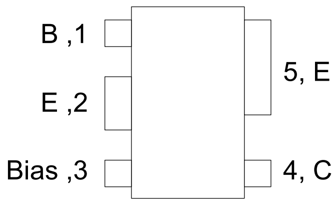
BGB550

Features

- Ideal for driver appliciations
- Small SCT595 package
- Open collector output
- Typical supply voltage: 1.4-4.3V
- Current easy adjustable by an external resistor
- SIEGET®-45 technology







Description

The BGB 550 is a silicon mirror biased RF transistor. The RF transistor is biased simply by adding an external resistor to the bias pin and an inductor as RF choke. There is no voltage drop at the collector. The mirror transistors are matched with a ratio of 1:14. If a higher degree of current stabilisation over supply voltage is needed a current source can be added without voltage drop at the collector.

ESD: Electrostatic discharge sensitive device, observe handling precaution!

Type	Package	Marking	Chip
BGB550	SCT595	MDs	T0529

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Maximum Ratings

Parameter	Symbol	Value	Unit
Maximum collector-emitter voltage	V_{CE}	4.5	V
Maximum collector current	I_C	350	mA
Maximum bias current	I_{Bias}	25	mA
Maximum emitter-base voltage	V_{EB}	1.5	V
Maximum base current	I_B	40	mA
Total power dissipation, T_S < 75 °C[1)]	P_{tot}	1000	mW
Junction temperature	T_j	150	°C
Operating temperature range	T_{OP}	-65 ... +150	°C
Storage temperature range	T_{STG}	-65 ... +150	°C
Thermal resistance: junction-soldering point	$R_{th\ JS}$	75	K/W

Notes:
For detailed symbol description refer to figure 1.
[1)] T_S is measured on the emitter lead at the soldering point to the PCB

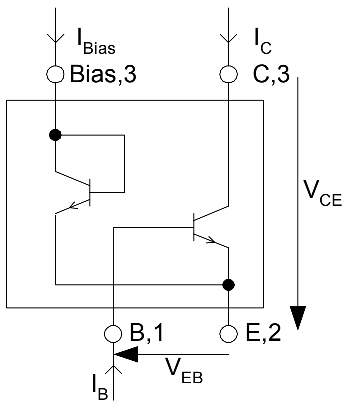

Fig. 1: Symbol definition

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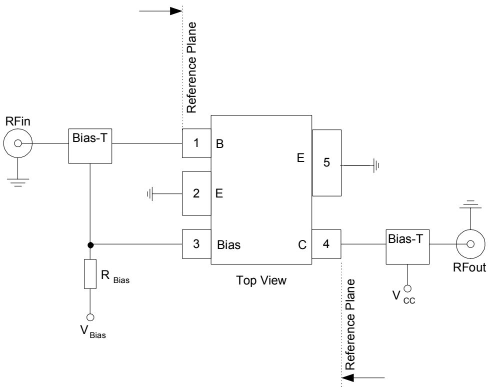


Fig. 2: Test circuit for electrical characteristics and S-parameter

Electrical Characteristics at T_A=25°C (measured in test circuit specified in fig. 2)

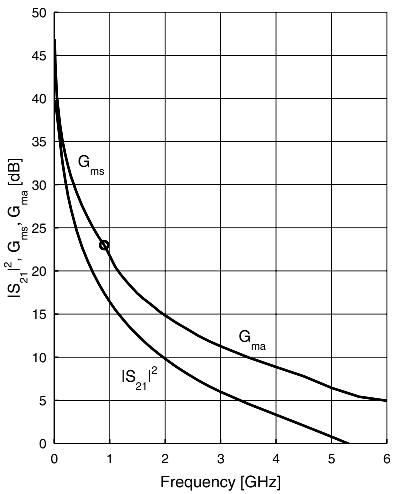
Parameter		Symbol	min.	typ.	max.	Unit
Maximum stable power gain V_{CC}=2V, I_c=100mA	f=0.9GHz f=1.8GHz	G_{ms}		22 16		dB
Insertion power gain V_{CC}=2V, I_c=100mA	f=0.9GHz f=1.8GHz	$\|S_{21}\|^2$		17 11		dB
Insertion loss V_{CC}=2V, I_c=0mA	f=0.9GHz f=1.8GHz	IL		-12.5 -13		dB
Noise figure (Z_S=Z_{Sopt}) V_{CC}=2V, f=1.8GHz	I_c=10mA I_c=50mA	F_{opt}		1.2 1.5		dB
Output power at 1dB gain compression V_{CC}=2V, I_c=100mA, f=1.8GHz	Z_L=Z_{LOPT} Z_L=50Ω	P_{-1dB}		19 15		dBm
Output third order intercept point V_{CC}=2V, I_c=100mA, f=1.8GHz	$Z_{L/S}$=$Z_{L/SOPT}$ $Z_{L/S}$=50Ω	OIP_3		28 25		dBm
Collector-base capacitance V_{CB}=2V, f=1MHz		C_{CB}		0.6		pF
Current Ratio $I_C/(I_{Bias} + I_B)$ I_{Bias}+ I_B=5mA, V_{CC}=2V		CR	10	14	17	

Preliminary

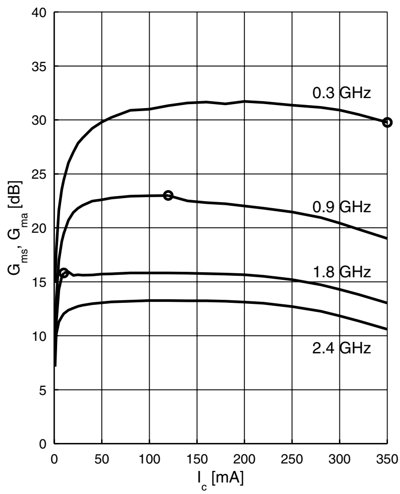
S-Parameter T_A=25°C,V_{CE}=2V, I_C=100mA (measured in test circuit specified in fig. 2)

f [GHz]	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.1	0.6217	-150.7	57.9230	123.0	0.0112	50.7	0.6959	-97.7
0.2	0.7181	-166.6	33.3990	104.4	0.0150	48.1	0.6248	-134.5
0.4	0.7497	-179.3	17.2680	89.4	0.0210	52.6	0.5988	-161.2
0.6	0.7630	173.3	11.4480	81.0	0.0272	55.7	0.6018	-173.1
0.8	0.7682	167.3	8.4390	74.4	0.0342	56.3	0.6070	179.0
1.0	0.7747	162.3	6.6270	69.1	0.0410	55.4	0.6171	172.8
1.2	0.7807	157.9	5.4350	64.3	0.0473	54.6	0.6223	167.7
1.4	0.7874	153.7	4.5780	59.9	0.0545	52.6	0.6323	163.0
1.6	0.7912	150.0	3.9570	55.7	0.0613	50.3	0.6383	159.0
1.8	0.7985	146.2	3.4780	51.6	0.0682	47.9	0.6482	155.0
2.0	0.8017	142.8	3.0980	47.6	0.0747	45.7	0.6523	151.6
2.4	0.8079	136.3	2.5350	40.0	0.0875	40.5	0.6638	145.0
3.0	0.8117	126.7	1.9930	28.9	0.1081	32.3	0.6738	135.2
4.0	0.8124	109.0	1.4660	8.8	0.1440	14.8	0.6947	118.2
5.0	0.8059	90.9	1.0920	-11.8	0.1708	-7.0	0.6902	99.5
6.0	0.8087	79.2	0.7820	-31.9	0.1750	-37.8	0.6612	89.0

Power Gain $|S_{21}|^2$, G_{ms}, G_{ma} = f(f)
V_{CC} = 2.0V; I_c = 0.10A



Power Gain G_{ms}, G_{ma} = f(I_c)
V_{CC} = 2.0V



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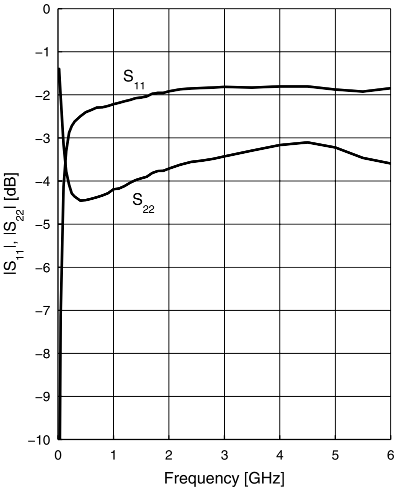
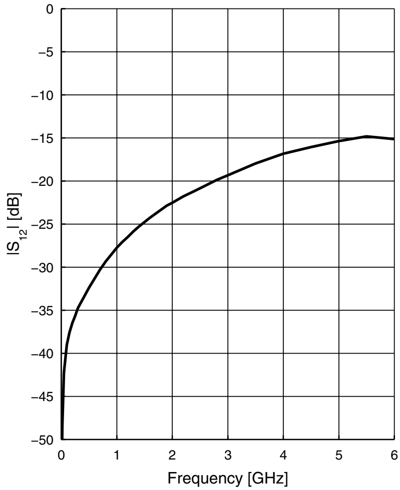
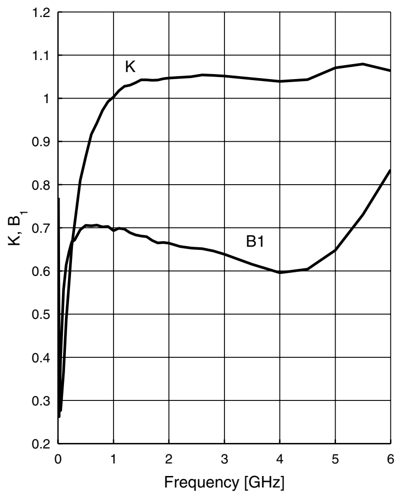
Matching $|S_{11}|, |S_{22}| = f(f)$
$V_{CC} = 2.0V$; $I_c = 0.10A$



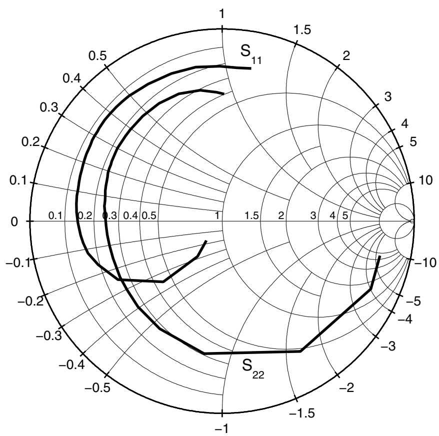
Reverse Isolation $|S_{12}| = f(f)$
$V_{CC} = 2.0V$; $I_c = 0.10A$



Stability K, $B_1 = f(f)$
$V_{CC} = 2.0V$; $I_c = 0.10A$



Matching $|S_{11}|, |S_{22}| = f(f)$
$V_{CC} = 2.0V$; $I_c = 0.10A$
f = 0.01GHz – 6GHz



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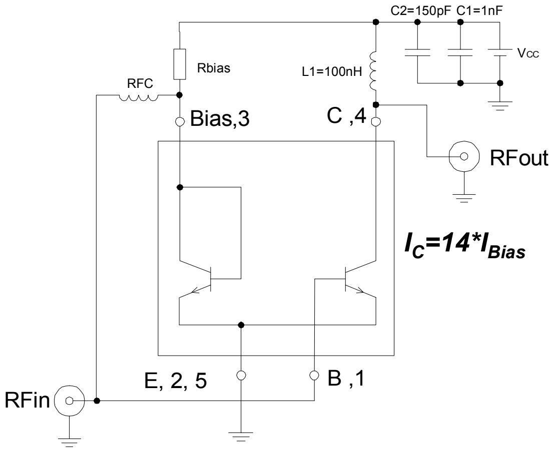
Typical Application

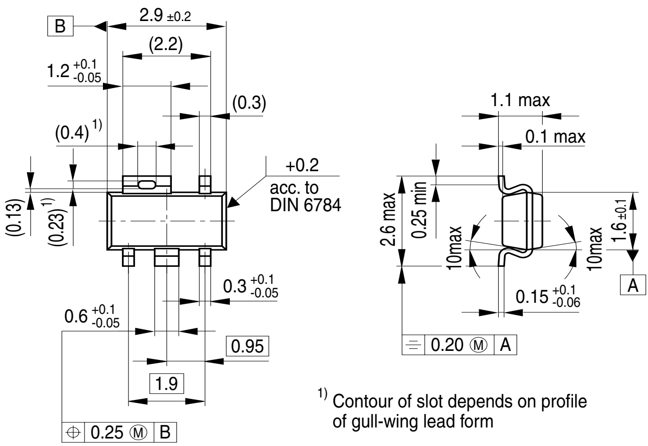


This proposal demonstrates how to use the BGB550 as a self-biased transistor. As for a discrete transistor matching circuits have to be applied.

The RFC circuit (e.g. an inductor) can be used to improve the input match.

Fig. 3: Typical application circuit

Package Outline



[1]) Contour of slot depends on profile of gull-wing lead form