

Dual P-Channel 20 V (D-S) MOSFET

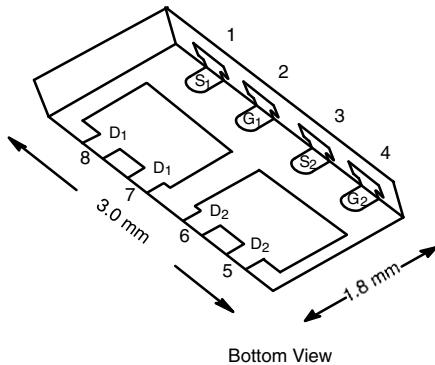
| PRODUCT SUMMARY | | | |
|-----------------|-----------------------------|------------------|--------------|
| V_{DS} (V) | $R_{DS(on)}$ (Ω) | I_D (A) | Q_g (Typ.) |
| - 20 | 0.059 at $V_{GS} = - 4.5$ V | - 6 ^a | 6.9 nC |
| | 0.096 at $V_{GS} = - 2.5$ V | - 6 ^a | |

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® ChipFET® Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8 mm Profile
- Typical ESD Performance 1500 V in HBM
- Compliant to RoHS Directive 2002/95/EC



PowerPAK ChipFET Dual



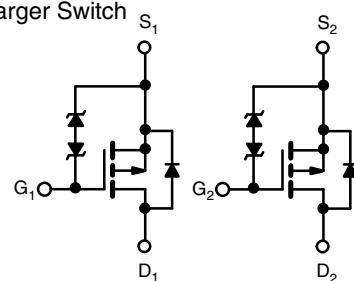
Marking Code

| | |
|----|-----|
| OA | XXX |
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 Lot Traceability and Date Code
 Part # Code

APPLICATIONS

- Load Switch and Charger Switch for Portable Devices
- DC/DC Converters



Ordering Information: Si5999EDU-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|--|----------------|-----------------------|------|
| Drain-Source Voltage | V_{DS} | - 20 | V |
| Gate-Source Voltage | V_{GS} | ± 12 | |
| Continuous Drain Current ($T_J = 150$ °C) | I_D | - 6 ^a | A |
| | | - 6 ^a | |
| | | - 5 ^{b, c} | |
| | | - 4 ^{b, c} | |
| Pulsed Drain Current ($t = 300$ μ s) | I_{DM} | - 20 | |
| Continuous Source-Drain Diode Current | I_S | - 6 ^a | |
| | | - 1.9 ^{b, c} | |
| Maximum Power Dissipation | P_D | 10.4 | W |
| | | 6.7 | |
| | | 2.3 ^{b, c} | |
| | | 1.5 ^{b, c} | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to 150 | °C |
| Soldering Recommendations (Peak Temperature) ^{d, e} | | 260 | |

THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Typical | Maximum | Unit |
|---|------------|---------|---------|------|
| Maximum Junction-to-Ambient ^{b, f} | R_{thJA} | 43 | 55 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | 9.5 | 12 | |

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$ s.
- See solder profile (www.vishay.com/ppg?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 105 °C/W.

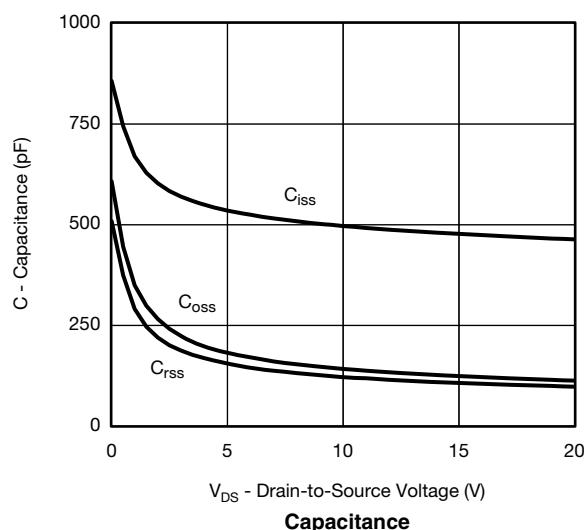
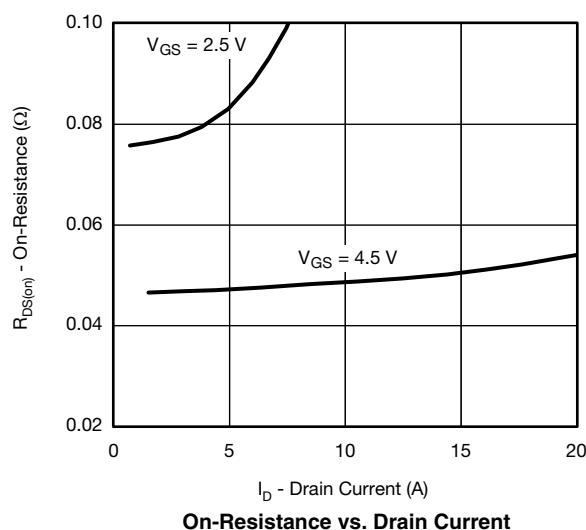
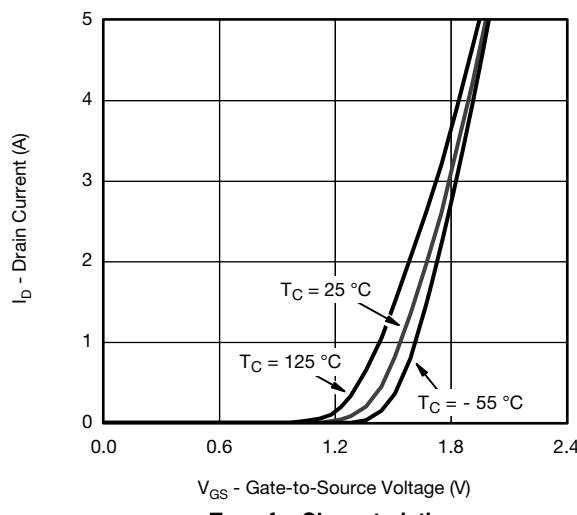
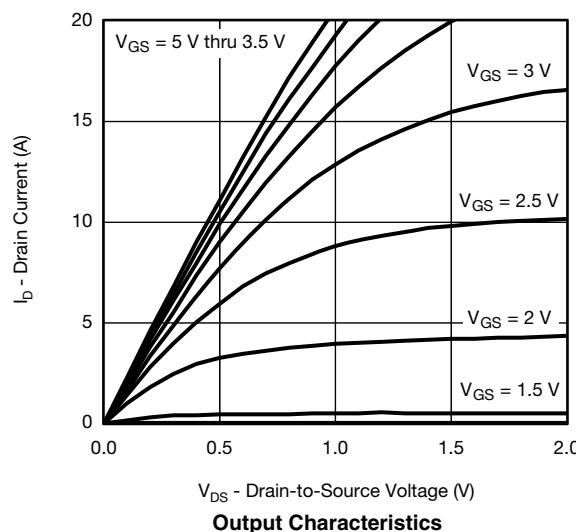
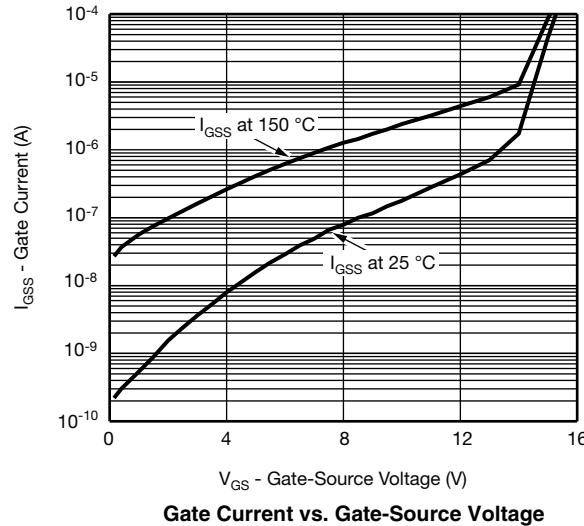
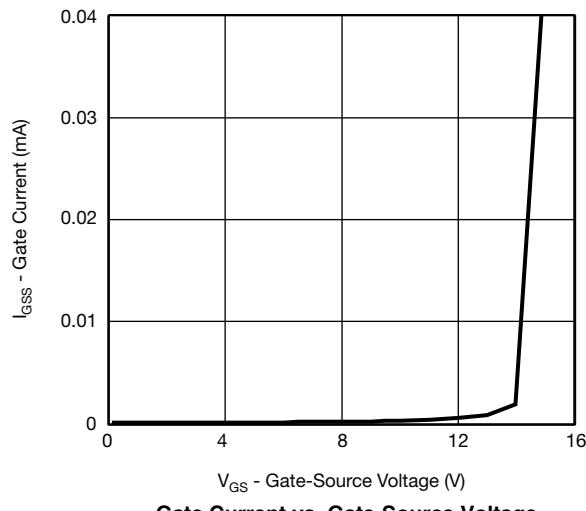
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|--|--------------------------------|---|------|-------|----------|-------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0 \text{ V}$, $I_D = -250 \mu\text{A}$ | -20 | | | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D = -250 \mu\text{A}$ | | -16 | | mV/°C |
| $V_{GS(\text{th})}$ Temperature Coefficient | $\Delta V_{GS(\text{th})}/T_J$ | | | 3 | | |
| Gate-Source Threshold Voltage | $V_{GS(\text{th})}$ | $V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$ | -0.6 | | -1.5 | V |
| Gate-Source Leakage | I_{GSS} | $V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 12 \text{ V}$ | | | ± 10 | μA |
| | | $V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 4.5 \text{ V}$ | | | ± 1 | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -20 \text{ V}$, $V_{GS} = 0 \text{ V}$ | | | -1 | |
| | | $V_{DS} = -20 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$ | | | -10 | |
| On-State Drain Current ^a | $I_{D(\text{on})}$ | $V_{DS} \leq -5 \text{ V}$, $V_{GS} = -4.5 \text{ V}$ | -20 | | | A |
| Drain-Source On-State Resistance ^a | $R_{DS(\text{on})}$ | $V_{GS} = -4.5 \text{ V}$, $I_D = -3.5 \text{ A}$ | | 0.047 | 0.059 | Ω |
| | | $V_{GS} = -2.5 \text{ V}$, $I_D = -1.5 \text{ A}$ | | 0.077 | 0.096 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = -10 \text{ V}$, $I_D = -3.5 \text{ A}$ | | 11 | | S |
| Dynamic^b | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = -10 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$ | | 496 | | pF |
| Output Capacitance | C_{oss} | | | 141 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 121 | | |
| Total Gate Charge | Q_g | $V_{DS} = -10 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -5 \text{ A}$ | | 13.2 | 20 | nC |
| | | | | 6.9 | 10.5 | |
| Gate-Source Charge | Q_{gs} | $V_{DS} = -10 \text{ V}$, $V_{GS} = -4.5 \text{ V}$, $I_D = -5 \text{ A}$ | | 1.6 | | |
| Gate-Drain Charge | Q_{gd} | | | 1.8 | | |
| Gate Resistance | R_g | $f = 1 \text{ MHz}$ | 2 | 8 | 16 | Ω |
| Turn-On Delay Time | $t_{d(\text{on})}$ | $V_{DD} = -10 \text{ V}$, $R_L = 2.5 \Omega$ $I_D \cong -4 \text{ A}$, $V_{GEN} = -4.5 \text{ V}$, $R_g = 1 \Omega$ | | 17 | 26 | ns |
| Rise Time | t_r | | | 21 | 32 | |
| Turn-Off Delay Time | $t_{d(\text{off})}$ | | | 26 | 40 | |
| Fall Time | t_f | | | 13 | 20 | |
| Turn-On Delay Time | $t_{d(\text{on})}$ | $V_{DD} = -10 \text{ V}$, $R_L = 2.5 \Omega$ $I_D \cong -4 \text{ A}$, $V_{GEN} = -10 \text{ V}$, $R_g = 1 \Omega$ | | 6 | 12 | |
| Rise Time | t_r | | | 11 | 22 | |
| Turn-Off Delay Time | $t_{d(\text{off})}$ | | | 23 | 35 | |
| Fall Time | t_f | | | 11 | 22 | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I_S | $T_C = 25^\circ\text{C}$ | | | -6 | A |
| Pulse Diode Forward Current | I_{SM} | | | | -20 | |
| Body Diode Voltage | V_{SD} | $I_S = -4 \text{ A}$, $V_{GS} = 0 \text{ V}$ | | -0.85 | -1.2 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $I_F = -4 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$ | | 24 | 48 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | 10 | 20 | nC |
| Reverse Recovery Fall Time | t_a | | | 14 | | ns |
| Reverse Recovery Rise Time | t_b | | | 10 | | |

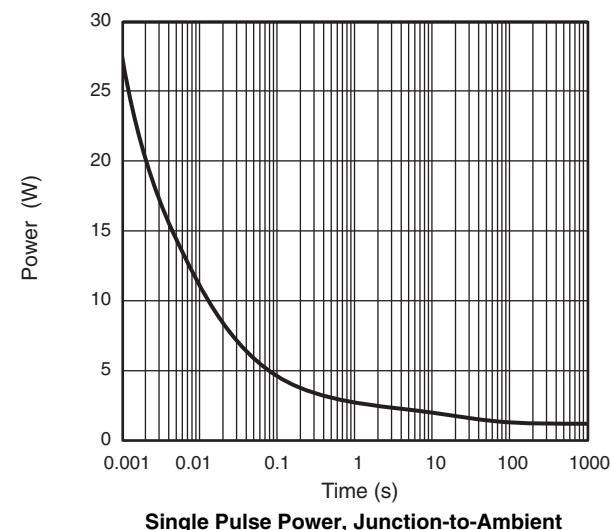
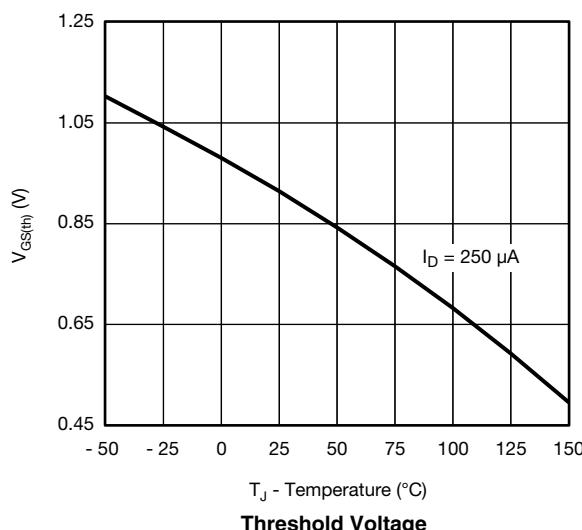
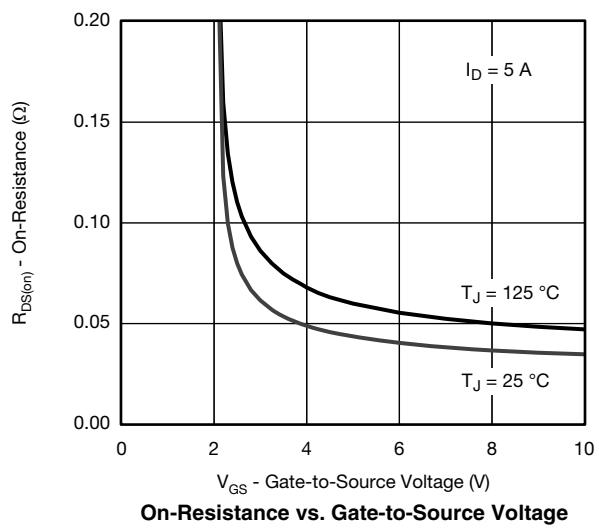
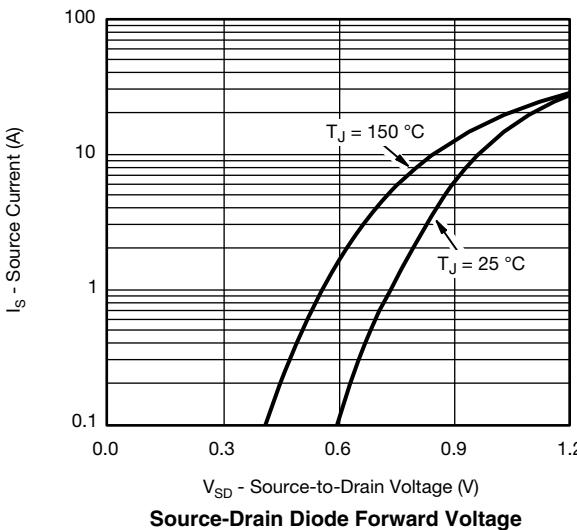
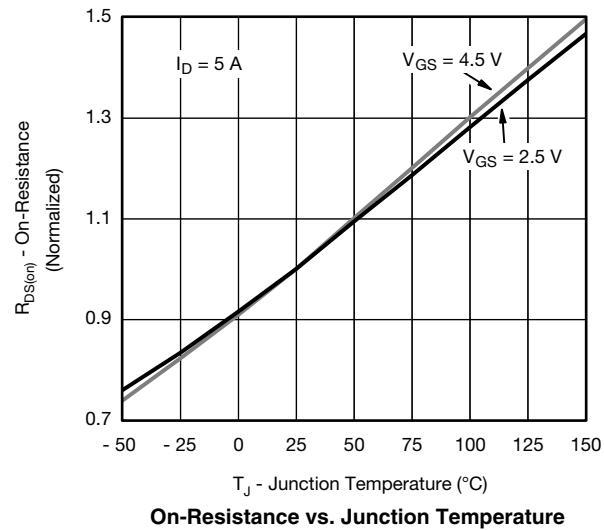
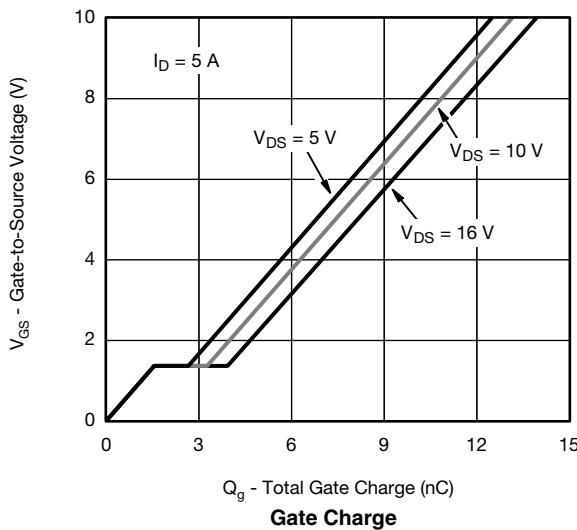
Notes:

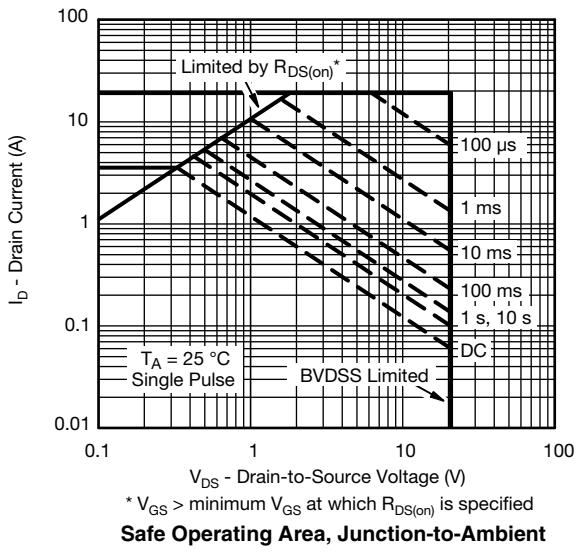
a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

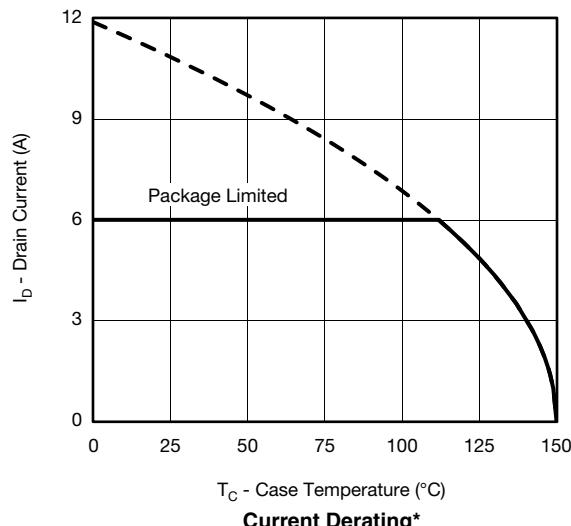
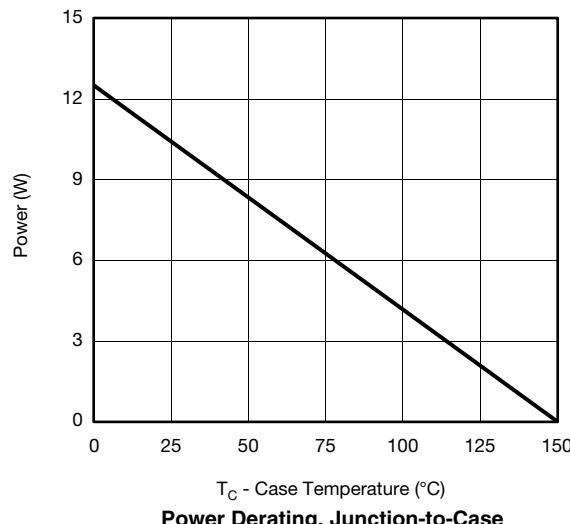
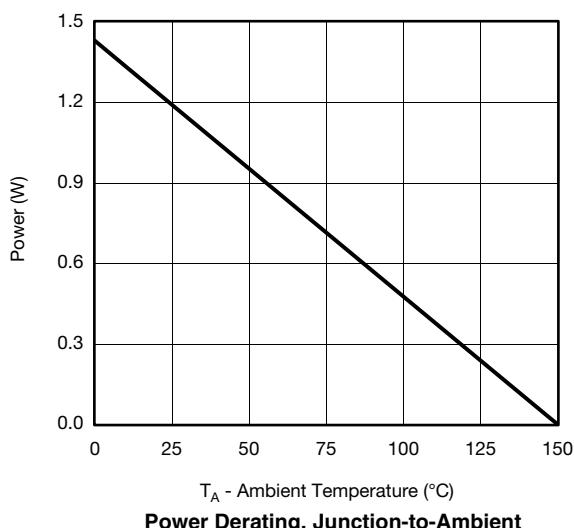
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


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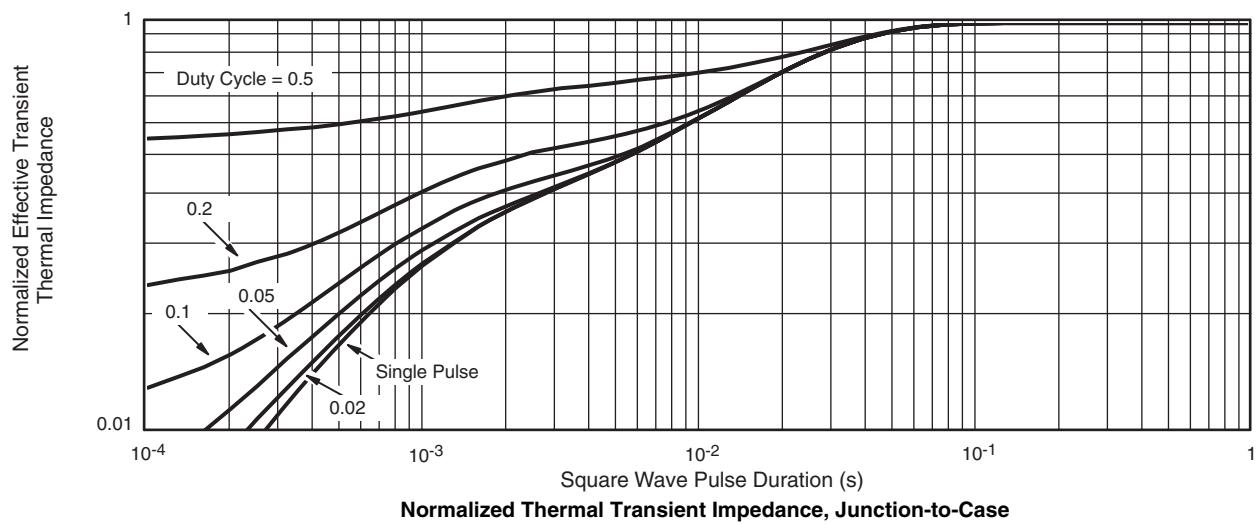
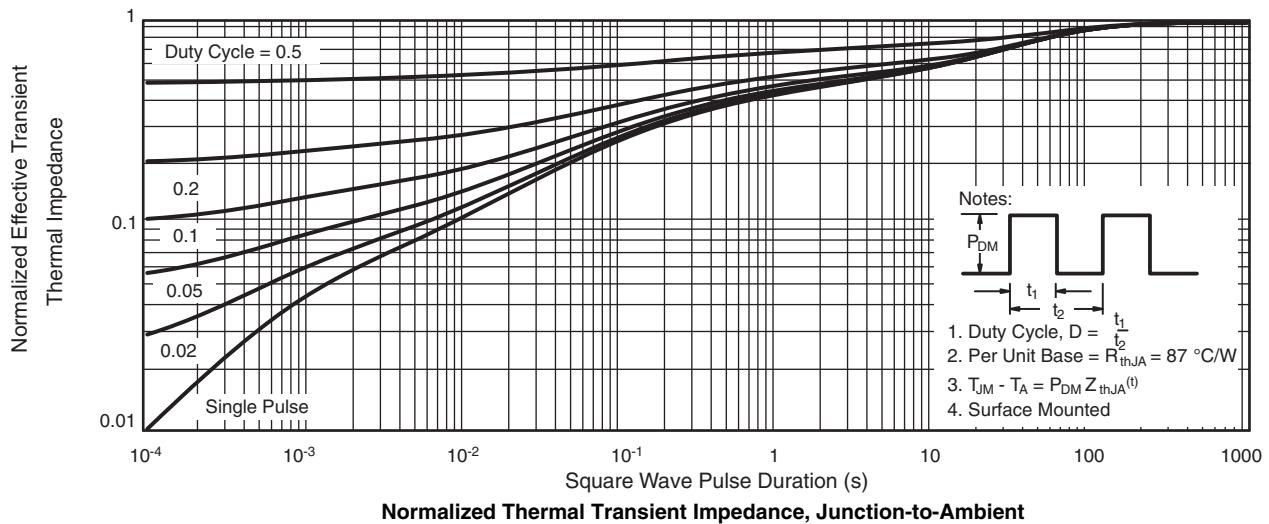
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

Current Derating*

Power Derating, Junction-to-Case

Power Derating, Junction-to-Ambient

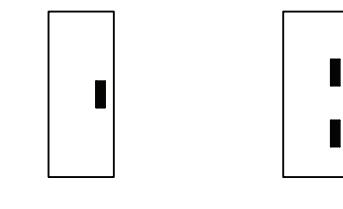
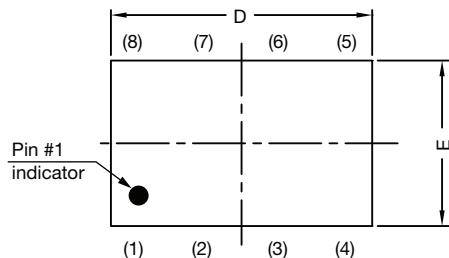
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

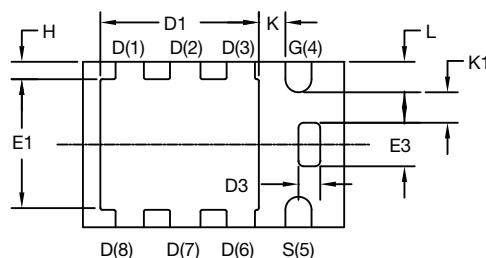
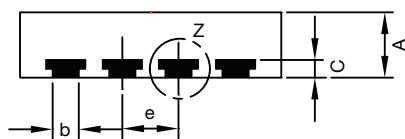


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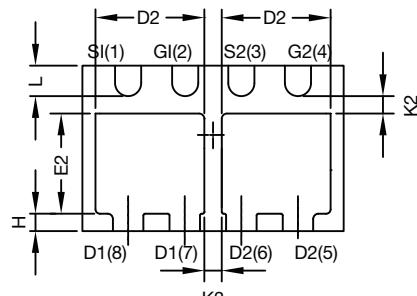
PowerPAK® ChipFET® Case Outline



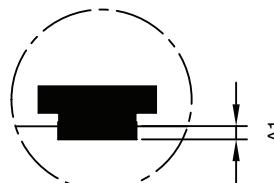
Side view of single Side view of dual



Backside view of single pad



Backside view of dual pad



Detail Z

| DIM. | MILLIMETERS | | | INCHES | | |
|------|-------------|------|------|-----------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.85 | 0.028 | 0.030 | 0.033 |
| A1 | 0 | - | 0.05 | 0 | - | 0.002 |
| b | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| C | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 2.92 | 3.00 | 3.08 | 0.115 | 0.118 | 0.121 |
| D1 | 1.75 | 1.87 | 2.00 | 0.069 | 0.074 | 0.079 |
| D2 | 1.07 | 1.20 | 1.32 | 0.042 | 0.047 | 0.052 |
| D3 | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| E | 1.82 | 1.90 | 1.98 | 0.072 | 0.075 | 0.078 |
| E1 | 1.38 | 1.50 | 1.63 | 0.054 | 0.059 | 0.064 |
| E2 | 0.92 | 1.05 | 1.17 | 0.036 | 0.041 | 0.046 |
| E3 | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| H | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| K | 0.25 | - | - | 0.010 | - | - |
| K1 | 0.30 | - | - | 0.012 | - | - |
| K2 | 0.20 | - | - | 0.008 | - | - |
| K3 | 0.20 | - | - | 0.008 | - | - |
| L | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |

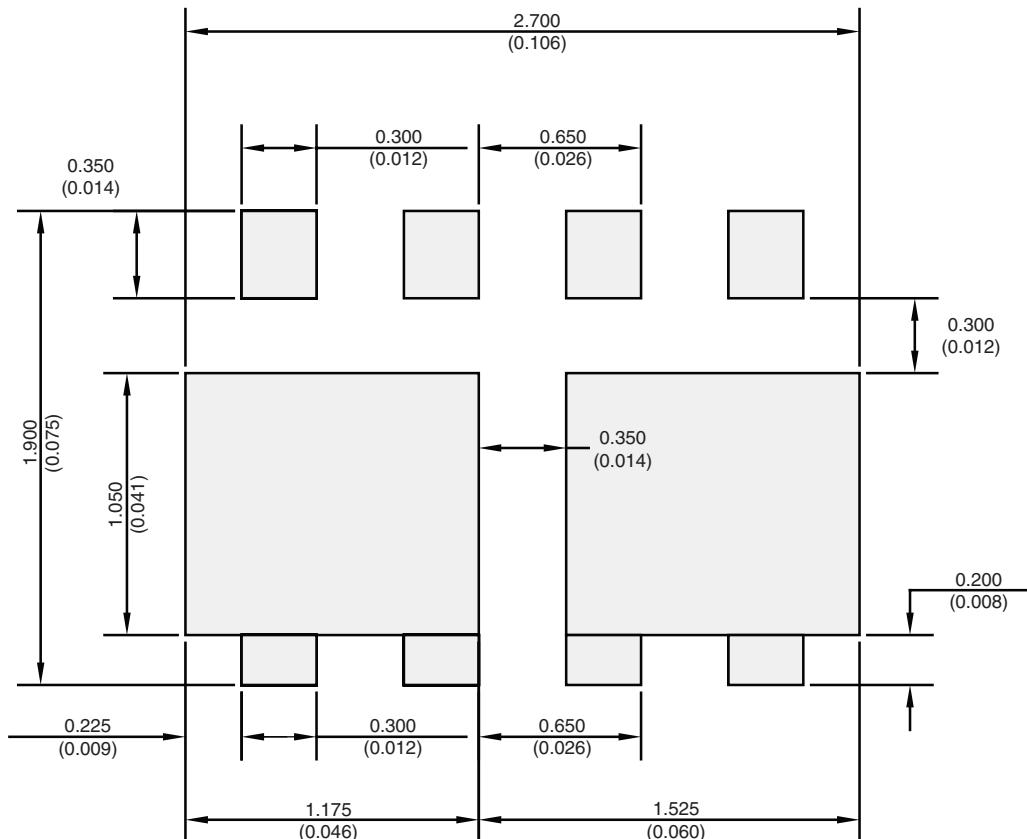
C14-0630-Rev. E, 21-Jul-14

DWG: 5940

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Dual



Recommended Minimum Pads
Dimensions in mm/Inches

Note: This is Flipped Mirror Image
Pin #1 Location is Top Left Corner

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