Dual Low Power Frequency Synthesizers

ADF4217L/ADF4218L/ADF4219L

FEATURES

Total I_{DD}: 7.1 mA
Bandwidth/RF 3.0 GHz
ADF4217L/ADF4218L, IF 1.1 GHz
ADF4219L, IF 1.0 GHz
2.6 V to 3.3 V Power Supply
1.8 V Logic Compatibility
Separate V_P Allows Extended Tuning Voltage
Selectable Dual Modulus Prescaler
Selectable Charge Pump Currents
Charge Pump Current Matching of 1%
3-Wire Serial Interface
Power-Down Mode

APPLICATIONS

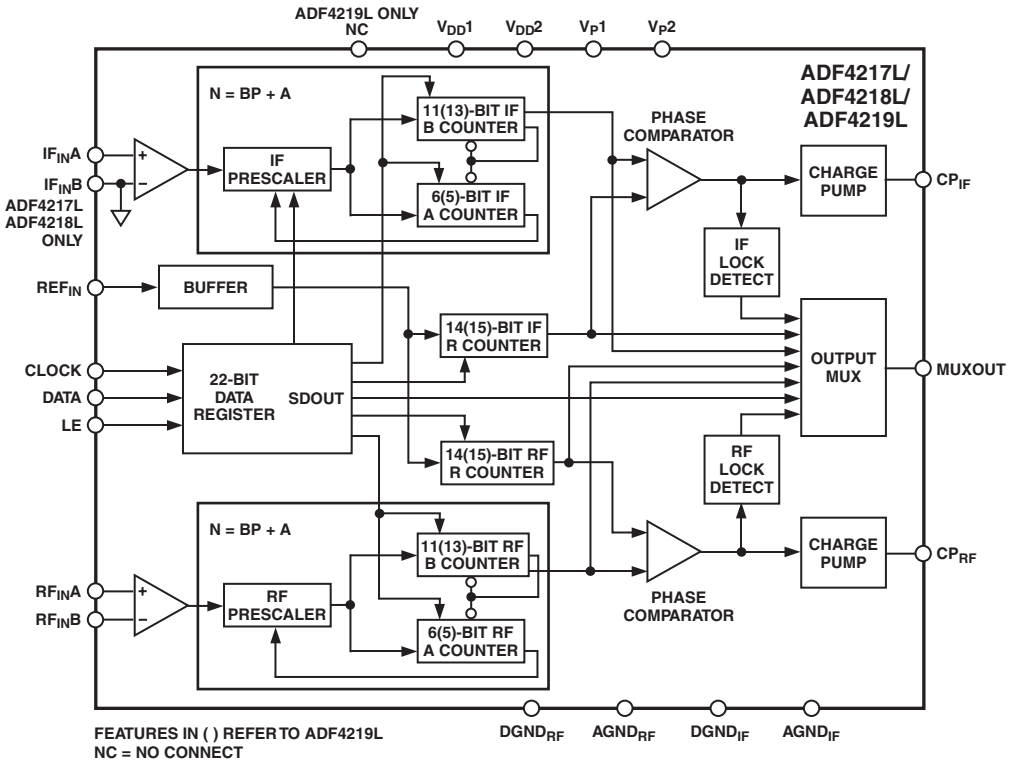
Wireless Handsets (GSM, PCS, DCS, CDMA, WCDMA)
Base Stations for Wireless Radio (GSM, PCS, DCS, WCDMA)
Wireless LANs
Communications Test Equipment
Cable TV Tuners (CATV)

GENERAL DESCRIPTION

The ADF4217L/ADF4218L/ADF4219L are low power dual frequency synthesizers that can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. They can provide the LO for both the RF and IF sections. They consist of a low noise digital PFD (phase frequency detector), a precision charge pump, a programmable reference divider, programmable A and B counters, and a dual modulus prescaler (P/P + 1). The A and B counters, in conjunction with the dual modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R Counter) allows selectable REFIN frequencies at the PFD input. A complete PLL (phase-locked loop) can be implemented if the synthesizers are used with an external loop filter and VCOs (voltage controlled oscillators).

Control of all the on-chip registers is via a simple 3-wire interface with 1.8 V compatibility. The devices operate with a power supply ranging from 2.6 V to 3.3 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM



REV. C

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ADF4217L/ADF4218L/ADF4219L–SPECIFICATIONS[1]

($V_{DD}1 = V_{DD}2 = 2.6$ V to 3.3 V; V_P1, $V_P2 = V_{DD}$ to 5.5 V; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1]	BChips[2] (Typical)	Unit	Test Conditions/Comments
RF CHARACTERISTICS				Use a square wave for operation below minimum frequency spec.
RF Input Frequency (RF_{IN})				
ADF4217L, ADF4218L	0.15/3.0	0.15/3.0	GHz min/max	–10 dBm minimum input signal
ADF4217L, ADF4218L	0.15/2.5	0.15/2.5	GHz min/max	–15 dBm minimum input signal
ADF4219L	0.8/2.2	0.8/2.2	GHz min/max	–20 dBm minimum input signal
RF Input Sensitivity				
ADF4217L, ADF4218L	–15/0	–15/0	dBm min/max	
ADF4219L	–20/0	–20/0	dBm min/max	
IF Input Frequency (IF_{IN})				
ADF4217L/ADF4218L	0.045/1.1	0.045/1.1	GHz min/max	–15 dBm minimum input signal
ADF4219L P = 16/17	0.045/1.0	0.045/1.0	GHz min/max	–10 dBm minimum input signal
ADF4219L P = 8/9	0.045/0.55	0.045/0.55	GHz min/max	–10 dBm minimum input signal
IF Input Sensitivity	–15/0	–15/0	dBm min/max	
Maximum Allowable Prescaler Output Frequency[3]	188	188	MHz max	
REFIN CHARACTERISTICS				
Reference Input Frequency	10/110	10/110	MHz min/max	For f < 10 MHz, use dc-coupled square wave, (0 to V_{DD}).
Reference Input Sensitivity	0.5	0.5	V p-p min	AC-coupled. When dc-coupled, 0 to V_{DD} max.
REFIN Input Capacitance	10	10	pF max	(CMOS compatible)
REFIN Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency[4]	56	56	MHz max	
CHARGE PUMP				
I_{CP} Sink/Source				
High Value	4	4	mA typ	
Low Value	1	1	mA typ	
Absolute Accuracy	1	1	% typ	
I_{CP} Three-State Leakage Current	1	1	nA typ	
Sink and Source Current Matching	6	6	% max	$0.5\ V < V_{CP} < V_P - 0.5$, 1% typ
I_{CP} vs. V_{CP}	5	5	% max	$0.5\ V < V_{CP} < V_P - 0.5$, 0.1% typ
I_{CP} vs. Temperature	2	2	% typ	$V_{CP} = V_P/2$
LOGIC INPUTS				
V_{INH}, Input High Voltage	1.4	1.4	V min	
V_{INL}, Input Low Voltage	0.6	0.6	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
Reference Input Current	±100	±100	µA max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	$V_{DD} - 0.4$	$V_{DD} - 0.4$	V min	$I_{OH} = 1$ mA
V_{OL}, Output Low Voltage	0.4	0.4	V max	$I_{OL} = 1$ mA
POWER SUPPLIES				
$V_{DD}1$	2.6/3.3	2.6/3.3	V min/V max	
$V_{DD}2$	$V_{DD}1$	$V_{DD}1$		
V_P1, V_P2	$V_{DD}1$/5.5 V	$V_{DD}1$/5.5 V	V min/V max	
I_{DD} (RF + IF)[5]	10	10	mA max	7.1 mA typ
(RF only)[5]	7	7	mA	4.7 mA typ
(IF only)[5]	5	5	mA	3.4 mA typ
I_P (I_P1 + I_P2)	0.6	0.6	mA typ	$T_A = 25°C$
Low Power Sleep Mode	1	1	µA typ	

Parameter	B Version[1]	BChips[2] (Typical)	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS[6]				
RF Phase Noise Floor[7]	–171	–171	dBc/Hz typ	@ 30 kHz PFD Frequency
	–163	–163	dBc/Hz typ	@ 200 kHz PFD Frequency
IF Phase Noise Floor[7]	–167	–167	dBc/Hz typ	@ 30 kHz PFD Frequency
	–159	–159	dBc/Hz typ	@ 200 kHz PFD Frequency
Phase Noise Performance[8]				@ VCO Output
RF[9]	–75	–75	dBc/Hz typ	1.95 GHz Output; 30 kHz PFD
RF[10]	–90	–90	dBc/Hz typ	900 MHz Output; 200 kHz PFD
IF[11]	–77	–77	dBc/Hz typ	900 MHz Output; 30 kHz PFD
IF[12]	–86	–86	dBc/Hz typ	900 MHz Output; 200 kHz PFD
Spurious Signals				Measured at Offset of $f_{PFD}/2f_{PFD}$
RF[9]	–78/–85	–78/–85	dBc typ	
RF[10]	–80/–84	–80/–84	dBc typ	
IF[11]	–79/–86	–79/–86	dBc typ	
IF[12]	–80/–84	–80/–84	dBc typ	

NOTES
[1]Operating temperature range is as follows: B Version: –40°C to +85°C.
[2]The BChip specifications are given as typical values.
[3]This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.
[4]Guaranteed by design. Sample tested to ensure compliance.
[5]This includes relevant I_P.
[6]V_{DD} = 3 V; P = 16/32; IF_{IN}/RF_{IN} for ADF4218L, ADF4219L = 540 MHz/900 MHz.
[7]The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value).
[8]The phase noise is measured with the EVAL-ADF421xEB1 Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer. (f_{REFOUT} = 10 MHz @ 0 dBm.)
[9]f_{REFIN} = 10 MHz; f_{PFD} = 30 kHz; Offset frequency = 1 kHz; f_{RF} = 1.95 GHz; N = 65000; Loop B/W = 3 kHz
[10]f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 900 MHz; N = 4500; Loop B/W = 20 kHz
[11]f_{REFIN} = 10 MHz; f_{PFD} = 30 kHz; Offset frequency = 1 kHz; f_{IF} = 900 MHz; N = 30000; Loop B/W = 3 kHz
[12]f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{IF} = 900 MHz; N = 4500; Loop B/W = 20 kHz

Specifications subject to change without notice.

TIMING CHARACTERISTICS ($V_{DD}1 = V_{DD}2 = 3$ V ± 10%, 5 V ± 10%; $V_{DD}1$, $V_{DD}2 \le V_P1$, $V_P2 \le 6.0$ V; $AGND_{RF1} = DGND_{RF1} = AGND_{RF2} = DGND_{RF2} = 0$ V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Setup Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Setup Time
t_6	50	ns min	LE Pulsewidth

Guaranteed by design but not production tested.

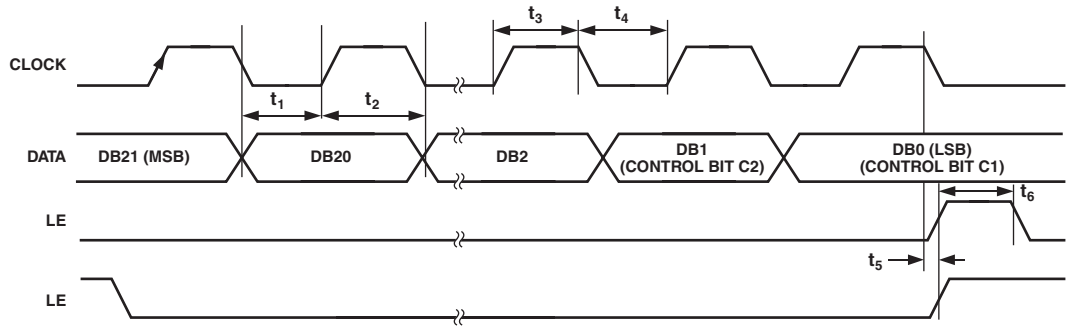


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = 25°C, unless otherwise noted.)

$V_{DD}1$ to GND[3] . . . . . –0.3 V to +3.6 V
$V_{DD}1$ to $V_{DD}2$ . . . . . –0.3 V to +0.3 V
V_P1, V_P2 to GND . . . . . –0.3 V to +5.8 V
V_P1, V_P2 to $V_{DD}1$ . . . . . –0.3 V to +5.5 V
Digital I/O Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND . . . . . –0.3 V to V_P + 0.3 V
REF_{IN}, $RF1_{IN}$ (A, B), IF_{IN} (A, B)
to GND . . . . . –0.3 V to V_{DD} + 0.3 V
$RF_{IN}A$ to $RF_{IN}B$ . . . . . ±320 mV
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C
TSSOP θ_{JA} Thermal Impedance . . . . . 150.4°C/W
LGA θ_{JA} . . . . . 112°C/W
Lead Temperature, Soldering
TSSOP, Vapor Phase (60 sec) . . . . . 215°C
TSSOP, Infrared (15 sec) . . . . . 220°C
LGA, Vapor Phase (60 sec) . . . . . 240°C
LGA, Infrared (20 sec) . . . . . 240°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]This device is a high performance RF integrated circuit with an ESD rating of < 2 kV and is ESD sensitive. Proper precautions should be taken for handling and assembly.

[3]GND = AGND = DGND = 0 V.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
ADF4217L/ADF4218L/ADF4219LBRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-20
ADF4217L/ADF4218L/ADF4219LBCC	–40°C to +85°C	Chip Array CASON (LGA)	CC-24

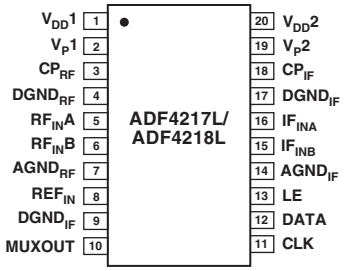
*Contact the factory for chip availability.

CAUTION

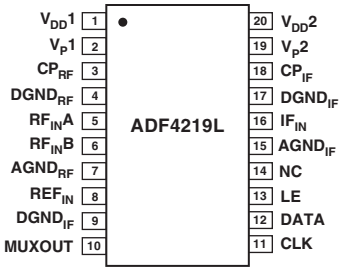
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADF4217L/ADF4218L/ADF4219L feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

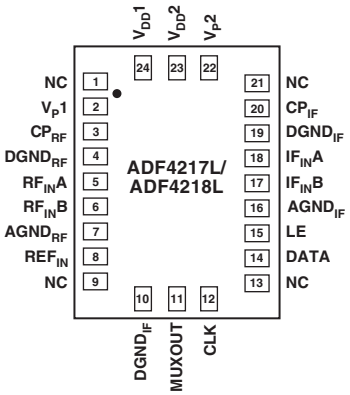
TSSOP



TSSOP

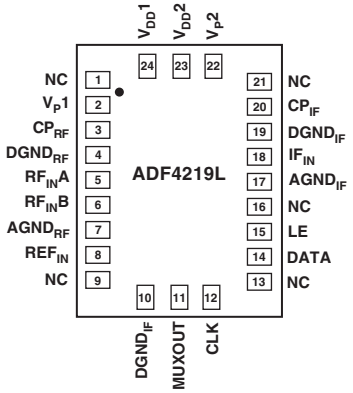


CHIP SCALE



NC = NO INTERNAL CONNECT

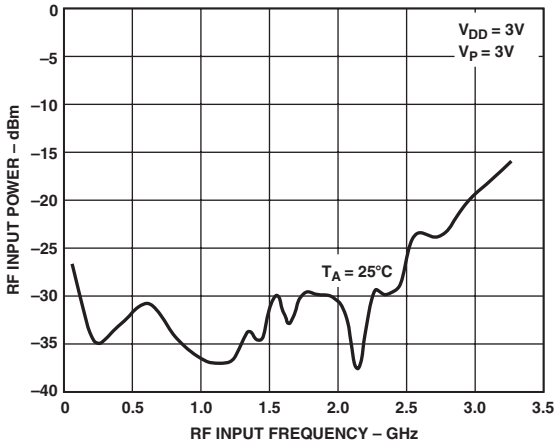
CHIP SCALE



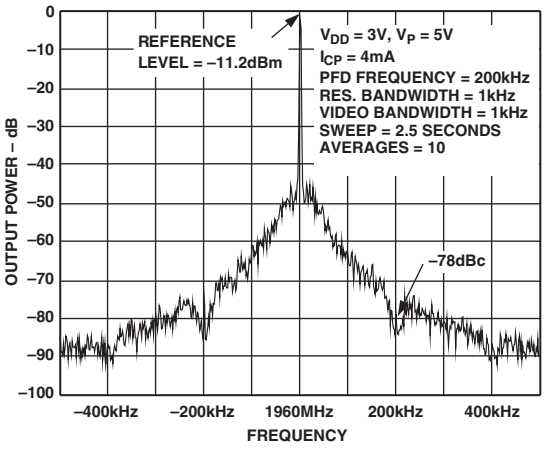
NC = NO INTERNAL CONNECT

PIN FUNCTION DESCRIPTIONS

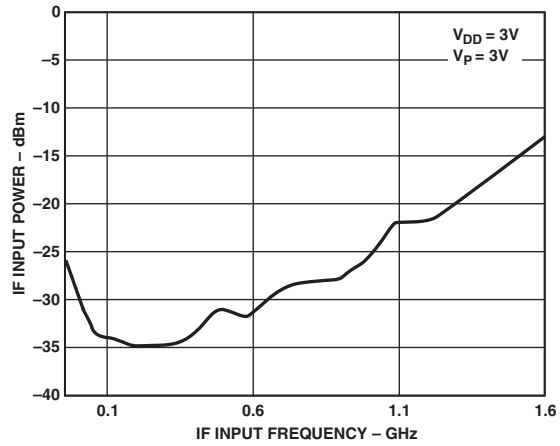
Mnemonic	Function
$V_{DD}1$	Positive Power Supply for the RF Section. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. $V_{DD}1$ should have a value of between 2.6 V and 3.3 V. $V_{DD}1$ must have the same potential as $V_{DD}2$.
V_P1	Power Supply for the RF Charge Pump. This should be greater than or equal to V_{DD}.
CP_{RF}	Output from the RF Charge Pump. When enabled, this provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.
$DGND_{RF}$	Ground Pin for the RF Digital Circuitry
$RF_{IN}A$	Input to the RF Prescaler. This low level input signal is normally ac-coupled to the external VCO.
$RF_{IN}B$	Complementary Input to the RF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
$AGND_{RF}$	Ground Pin for the RF Analog Circuitry
REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator, or can be ac-coupled.
$DGND_{IF}$	Ground Pin for the IF Digital, Interface, and Control Circuitry
MUXOUT	This multiplexer output allows either the IF/RF Lock Detect, the scaled RF, or the scaled Reference Frequency to be accessed externally (Table V).
CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 22-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches; the latch is selected using the control bits.
$AGND_{IF}$	Ground Pin for the IF Analog Circuitry
NC	This pin is not connected internally (ADF4219L only).
$IF_{IN}B$	Complementary Input to the IF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor, typically 100 pF (ADF4217L/ADF4218L only).
$IF_{IN}A$	Input to the IF Prescaler. This low level input signal is normally ac-coupled to the external VCO.
$DGND_{IF}$	Ground Pin for the IF Digital, Interface, and Control Circuitry
CP_{IF}	Output from the IF Charge Pump. When enabled, this provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.
V_P2	Power Supply for the IF Charge Pump. This should be greater than or equal to V_{DD}.
$V_{DD}2$	Positive Power Supply for the IF Interface and Oscillator Sections. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. $V_{DD}2$ should have a value of between 2.6 V and 3.3 V. $V_{DD}2$ must have the same potential as $V_{DD}1$.



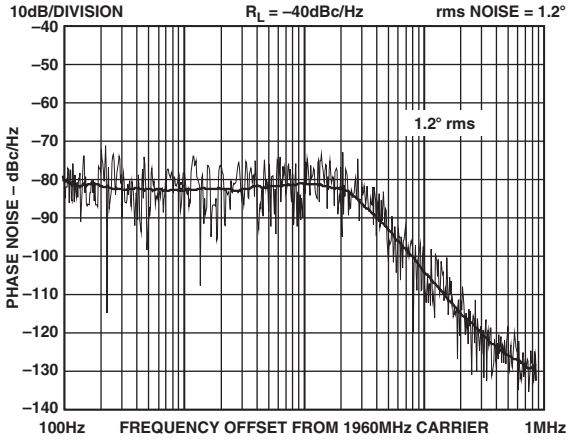
TPC 1. Input Sensitivity, RF Input



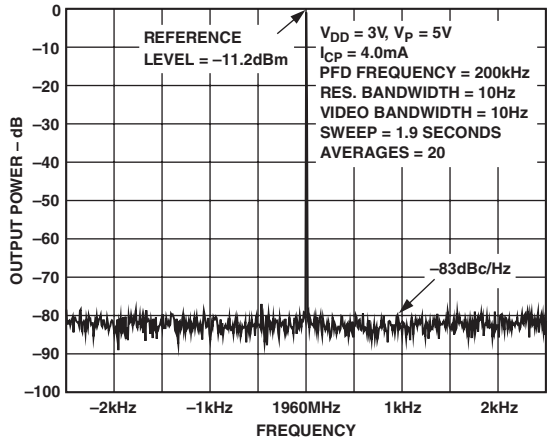
TPC 4. Reference Spurs, RF Side (1960 MHz, 200 kHz, 20 kHz)



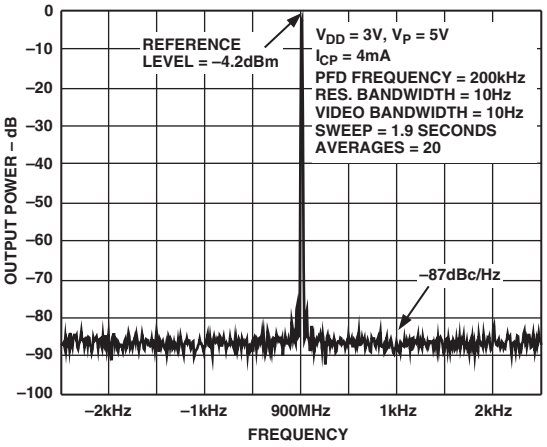
TPC 2. Input Sensitivity, IF Input



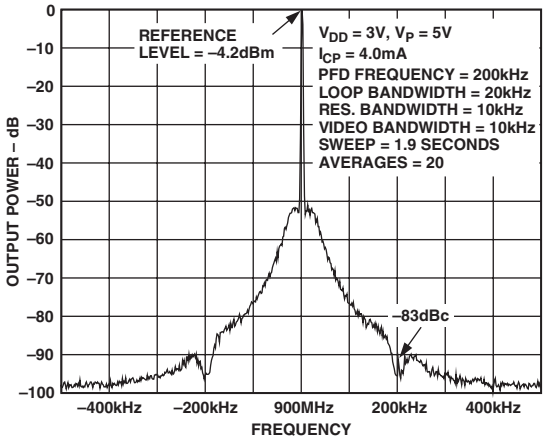
TPC 5. Integrated Phase Noise, RF Side (1960 MHz, 200 kHz, 20 kHz)



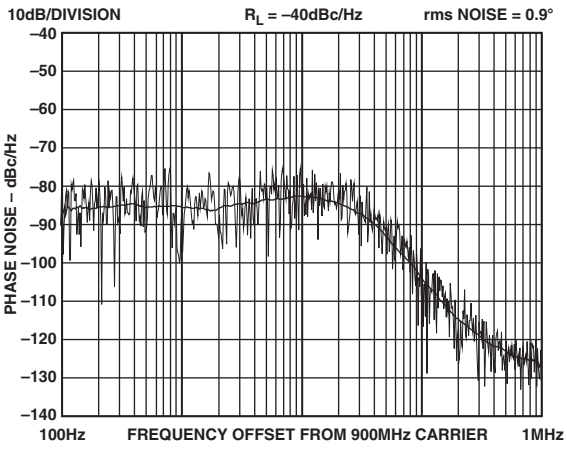
TPC 3. Phase Noise, RF Side (1960 MHz, 200 kHz, 20 kHz)



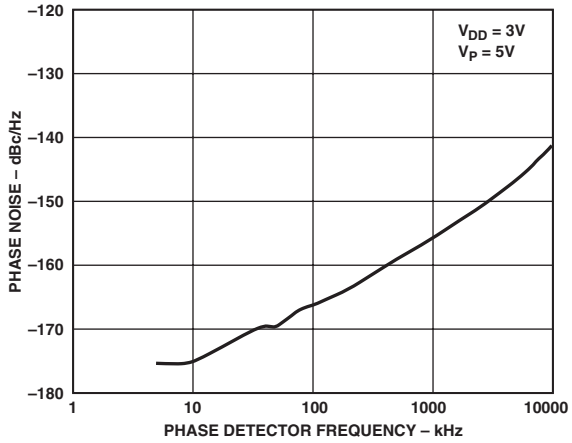
TPC 6. Phase Noise, IF Side (900 MHz, 200 kHz, 20 kHz)



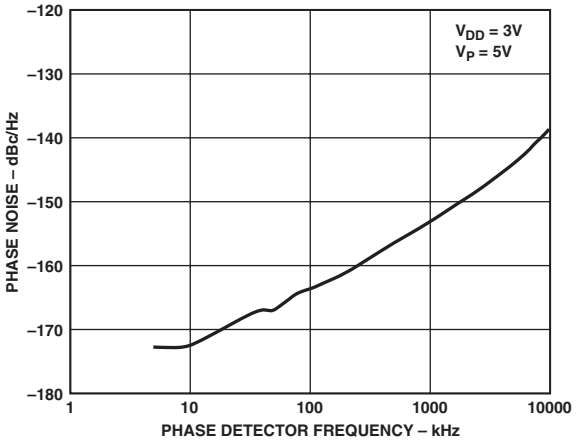
TPC 7. Reference Spurs, IF Side (900 MHz, 200 kHz, 20 kHz)



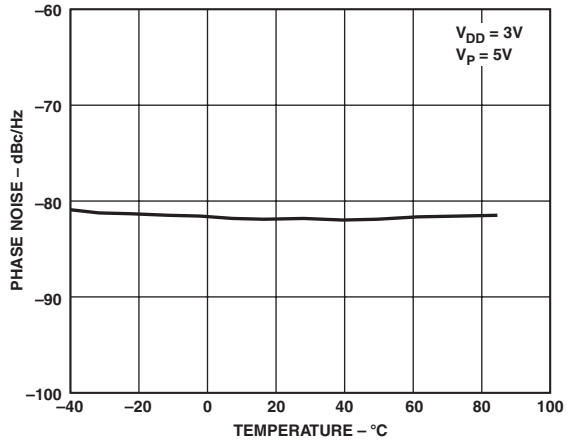
TPC 8. Integrated Phase Noise, IF Side (900 MHz, 200 kHz, 20 kHz)



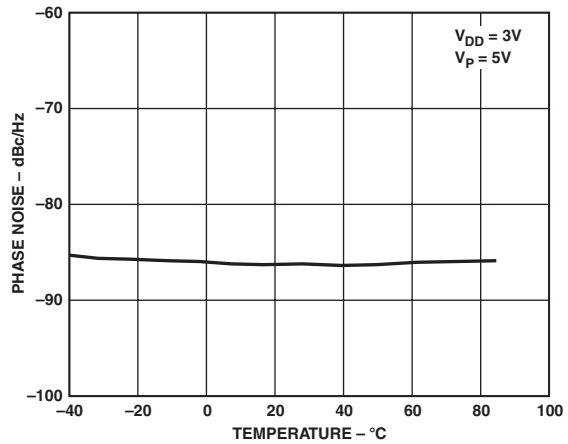
TPC 9. Phase Noise Referred to CP Output vs. PFD Frequency, RF Side



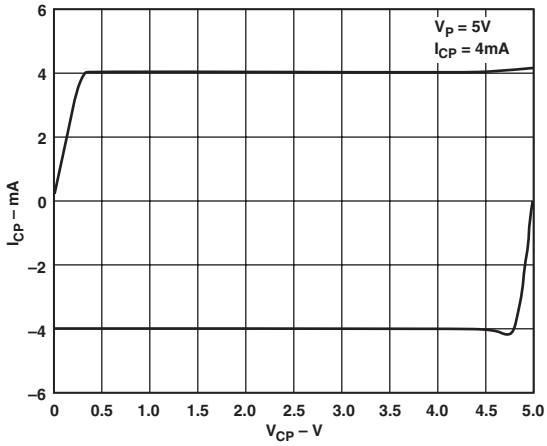
TPC 10. Phase Noise Referred to CP Output vs. PFD Frequency, IF Side



TPC 11. Phase Noise vs. Temperature, RF Side (1960 MHz, 200 kHz, 20 kHz)



TPC 12. Phase Noise vs. Temperature, IF Side (900 MHz, 200 kHz, 20 kHz)



TPC 13. Charge Pump Output Characteristics

CIRCUIT DESCRIPTION

Reference Input Section

The reference input stage is shown in Figure 2. SW1 and SW2 are normally closed switches; SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

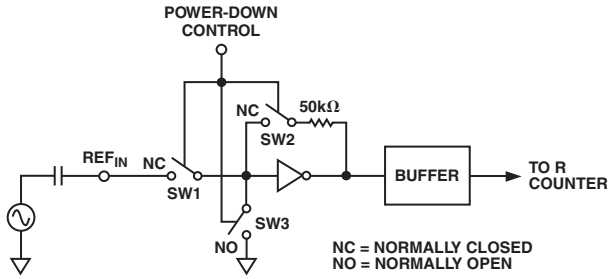


Figure 2. Reference Input Stage

IF/RF Input Stage

The IF/RF input stage is shown in Figure 3. It is followed by a two-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

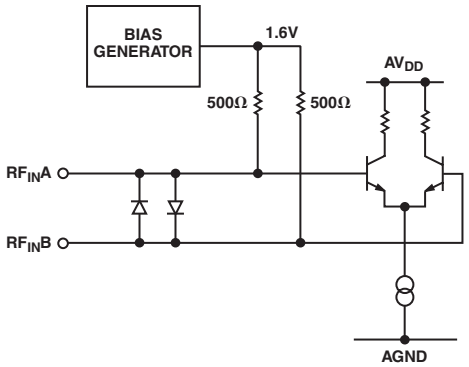


Figure 3. IF/RF Input Stage

Prescaler

The dual modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = BP + A). This prescaler, operating at CML levels, takes the clock from the IF/RF input stage and divides it down to a manageable frequency for the CMOS A and B counters. It is based on a synchronous 4/5 core.

The prescaler is selectable. On the IF side, it can be set to either 8/9 (DB20 of the IF AB Counter Latch set to 0) or 16/17 (DB20 set to 1). On the RF side of the ADF4217L/ADF4218L, it can be set to 64/65 or 32/33. On the ADF4219L, the RF prescaler can be set to 16/17 or 32/33. See Tables V, VI, VIII, and IX.

A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The devices are guaranteed to work when the prescaler output is 188 MHz or less. Typically they will work with 250 MHz output from the prescaler.

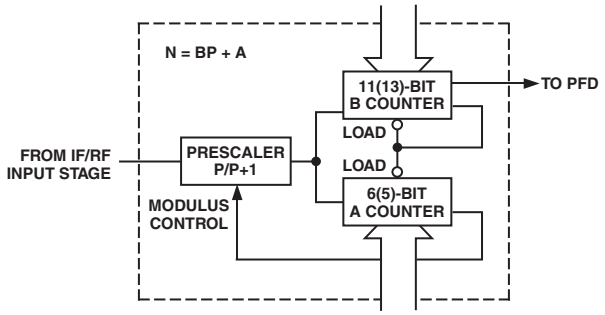


Figure 4. Reference Input Stage, A and B Counters

The A and B counters, in conjunction with the dual modulus prescaler, make it possible to generate output frequencies that are spaced only by the Reference Frequency divided by *R*. The equation for the VCO frequency is as follows:

$$f_{VCO} = \left[(P \times B) + A\right] \times f_{REF_{IN}} / R$$

f_{VCO} = Output frequency of external voltage controlled oscillator (VCO).

P = Preset modulus of dual modulus prescaler (8/9, 16/17, and so on).

B = Preset divide ratio of binary 11-bit counter (ADF4217L/ ADF4218L), binary 13-bit counter (ADF4219L).

A = Preset divide ratio of binary 6-bit A counter (ADF4217L/ ADF4218L), binary 5-bit counter (ADF4219L).

$f_{REF_{IN}}$ = Output frequency of the external reference frequency oscillator.

R = Preset divide ratio of binary 14-bit programmable reference counter (1 to 16383). The ADF4219L has an R divide of 15 bits.

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed. The extra R15 bit on the ADF4219L allows ratios from 1 to 32767.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 5 is a simplified schematic.

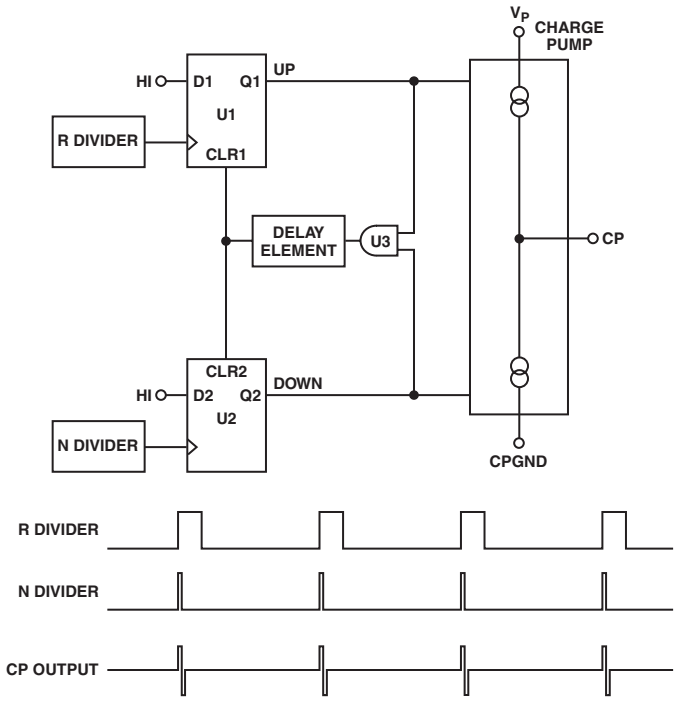


Figure 5. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4217L family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by P3, P4, P11, and P12. See Tables IV and VII. Figure 6 shows the MUXOUT section in block diagram form.

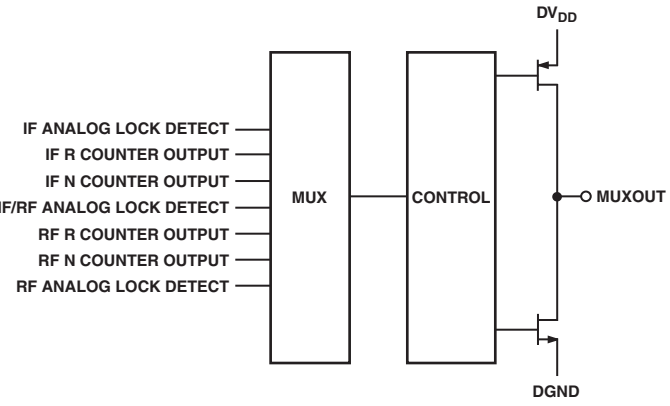


Figure 6. MUXOUT Circuit

Lock Detect

MUXOUT can be programmed for analog lock detect. The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, it is high with narrow low going pulses.

INPUT SHIFT REGISTER

The functional block diagram for the ADF4217L family is shown on page 1. The main blocks include a 22-bit input shift register, a 14-bit R counter, and an N counter. The N counter is comprised of a 6-bit A counter and an 11-bit B counter for the ADF4217L and the ADF4218L. The 18-bit N counter on the ADF4219L is comprised of a 13-bit B counter and a 5-bit A counter. Data is clocked into the 22-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table I.

Table I. C2, C1 Truth Table

Control Bits C2	C1	Data Latch
0	0	IF R Counter
0	1	IF AB Counter (and Prescaler Select)
1	0	RF R Counter
1	1	RF AB Counter (and Prescaler Select)

Table II. ADF4217L/ADF4218L Family Latch Summary

IF REFERENCE COUNTER LATCH

IF F_O	IF LOCK DETECT	THREE-STATE CP_{IF}	IF CP GAIN	IF PD POLARITY	NOT USED	14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

IF AB COUNTER LATCH

IF POWER-DOWN	IF PRESCALER	11-BIT B COUNTER											NOT USED	6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

RF REFERENCE COUNTER LATCH

RF F_O	RF LOCK DETECT	THREE-STATE CP_{IF}	RF CP GAIN	RF PD POLARITY	NOT USED	14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P12	P11	P10	P13	P9		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

RF AB COUNTER LATCH

RF POWER-DOWN	RF PRESCALER	11-BIT B COUNTER											NOT USED	6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P14	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

Table III. ADF4219L Family Latch Summary

IF REFERENCE COUNTER LATCH

IF F_O	IF LOCK DETECT	THREE-STATE CP_{IF}	IF CP GAIN	IF PD POLARITY	15-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

IF AB COUNTER LATCH

IF POWER-DOWN	IF PRESCALER	13-BIT B COUNTER													5-BIT A COUNTER					CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

RF REFERENCE COUNTER LATCH

RF F_O	RF LOCK DETECT	THREE-STATE CP_{IF}	RF CP GAIN	RF PD POLARITY	15-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P12	P11	P10	P13	P9	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

RF AB COUNTER LATCH

RF POWER-DOWN	RF PRESCALER	13-BIT B COUNTER													5-BIT A COUNTER					CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

Table IV. ADF4217L/ADF4218L/ADF4219L IF Reference Counter Latch Map

IF REFERENCE COUNTER LATCH

IF F_O	IF LOCK DETECT	THREE-STATE CP_{IF}	IF CP GAIN	IF PD POLARITY	ADF4219L ONLY	14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P4	P3	P2	P5	P1	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

R15	R14	R13	R12	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	0	.....	0	0	1	1
0	0	0	0	.....	0	1	0	2
0	0	0	0	.....	0	1	1	3
0	0	0	0	.....	1	0	0	4
.	.	.	.	.....	.	.	.	.
.	.	.	.	.....	.	.	.	.
.	.	.	.	.....	.	.	.	.
0	1	1	1	.....	1	0	0	16380
0	1	1	1	.....	1	0	1	16381
0	1	1	1	.....	1	1	0	16382
0	1	1	1	.....	1	1	1	16383
.	.	.	.	.....	.	.	.	.
1	1	1	1	.....	1	1	1	32767

P1	PD POLARITY
0	NEGATIVE
1	POSITIVE

P5	I_{CP}
0	1.0mA
1	4.0mA

P2	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

P12 FROM RF R LATCH	P11	P4	P3	MUXOUT
0	0	0	0	LOGIC LOW STATE
0	0	0	1	IF ANALOG LOCK DETECT
0	X	1	0	IF REFERENCE DIVIDER OUTPUT
0	X	1	1	IF N DIVIDER OUTPUT
0	1	0	0	RF ANALOG LOCK DETECT
0	1	0	1	RF/IF ANALOG LOCK DETECT
1	X	0	0	RF REFERENCE DIVIDER
1	X	0	1	RF N DIVIDER
1	0	1	0	FAST LOCK OUTPUT SWITCH ON AND CONNECTED TO MUXOUT
1	0	1	1	IF COUNTER RESET
1	1	1	0	RF COUNTER RESET
1	1	1	1	IF AND RF COUNTER RESET

Table V. ADF4217L/ADF4218L IF AB Counter Latch Map

IF AB COUNTER LATCH

IF POWER-DOWN	IF PRESCALER	11-BIT B COUNTER											NOT USED	6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

A6	A5	A4	A3	A2	A1	A COUNTER DIVIDE RATIO
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	62
1	1	1	1	1	1	63

B11	B10	B9	.....	B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	0	1	NOT ALLOWED
0	0	0	.....	0	1	0	NOT ALLOWED
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	2044
1	1	1	.....	1	0	1	2045
1	1	1	.....	1	1	0	2046
1	1	1	.....	1	1	1	2047

P6	IF PRESCALER
0	8/9
1	16/17

P7	IF SECTION
0	NORMAL OPERATION
1	POWER-DOWN

N = BP + A, P IS PRESCALER VALUE SET BY P6. B MUST BE GREATER THAN OR EQUAL TO A. TO ENSURE CONTINUOUSLY ADJACENT VALUES OF N, N_{MIN} IS ($P^2 - P$).

Table VI. ADF4219L IF AB Counter Latch Map

IF AB COUNTER LATCH

IF POWER-DOWN	IF PRESCALER	13-BIT B COUNTER													5-BIT A COUNTER					CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P7	P6	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

A5	A4	A3	A2	A1	A COUNTER DIVIDE RATIO
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
.	.	.	.	.	.
1	1	1	1	0	30
1	1	1	1	1	31

B13	B12	B11	.....	B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	0	1	NOT ALLOWED
0	0	0	.....	0	1	0	NOT ALLOWED
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	8188
1	1	1	.....	1	0	1	8189
1	1	1	.....	1	1	0	8190
1	1	1	.....	1	1	1	8191

P6	IF PRESCALER
0	8/9
1	16/17

P7	IF SECTION
0	NORMAL OPERATION
1	POWER-DOWN

N = BP + A, P IS PRESCALER VALUE SET BY P6.
B MUST BE GREATER THAN OR EQUAL TO A.
FOR CONTIGUOUS VALUES OF N, N_{MIN} IS (P^2 – P).

Table VII. RF Reference Counter Latch Map

RF REFERENCE COUNTER LATCH

RF F_O	RF LOCK DETECT	THREE-STATE CP_{IF}	RF CP GAIN	RF PD POLARITY	ADF4129L ONLY	14-BIT REFERENCE COUNTER, R												CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P12	P11	P10	P13	P9	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

R15	R14	R13	R12	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	0	.....	0	0	1	1
0	0	0	0	.....	0	1	0	2
0	0	0	0	.....	0	1	1	3
0	0	0	0	.....	1	0	0	4
.	.	.	.	.....	.	.	.	.
.	.	.	.	.....	.	.	.	.
.	.	.	.	.....	.	.	.	.
0	1	1	1	.....	1	0	0	16380
0	1	1	1	.....	1	0	1	16381
0	1	1	1	.....	1	1	0	16382
0	1	1	1	.....	1	1	1	16383
.	.	.	.	.....	.	.	.	.
1	1	1	1	.....	1	1	1	32767

P9	PD POLARITY
0	NEGATIVE
1	POSITIVE

P13	I_{CP}
0	1.0mA
1	4.0mA

P10	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

P12	P11	P4 FROM RF R LATCH	P3	MUXOUT
0	0	0	0	LOGIC LOW STATE
0	0	0	1	IF ANALOG LOCK DETECT
0	X	1	0	IF REFERENCE DIVIDER OUTPUT
0	X	1	1	IF N DIVIDER OUTPUT
0	1	0	0	RF ANALOG LOCK DETECT
0	1	0	1	RF/IF ANALOG LOCK DETECT
1	X	0	0	RF REFERENCE DIVIDER
1	X	0	1	RF N DIVIDER
1	0	1	0	FAST LOCK OUTPUT SWITCH ON AND CONNECTED TO MUXOUT
1	0	1	1	IF COUNTER RESET
1	1	1	0	RF COUNTER RESET
1	1	1	1	IF AND RF COUNTER RESET

Table VIII. ADF4217L/ADF4218L RF AB Counter Latch Map

RF AB COUNTER LATCH

RF POWER-DOWN	RF PRESCALER	11-BIT B COUNTER											NOT USED	6-BIT A COUNTER						CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P14	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

A6	A5	A4	A3	A2	A1	A COUNTER DIVIDE RATIO
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	62
1	1	1	1	1	1	63

B11	B10	B9	.....	B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	0	1	NOT ALLOWED
0	0	0	.....	0	1	0	NOT ALLOWED
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	2044
1	1	1	.....	1	0	1	2045
1	1	1	.....	1	1	0	2046
1	1	1	.....	1	1	1	2047

P14	RF PRESCALER ADF4217L	RF PRESCALER ADF4218L
0	64/65	32/33
1	32/33	64/65

P16	RF SECTION
0	NORMAL OPERATION
1	POWER-DOWN

N = BP + A, P IS PRESCALER VALUE SET BY P6, B MUST BE GREATER THAN OR EQUAL TO A. TO ENSURE CONTINUOUSLY ADJACENT VALUES OF $N \times F_{REF}$, N_{MIN} IS $(P^2 - P)$.

Table IX. ADF4219L RF AB Counter Latch Map

RF AB COUNTER LATCH

RF POWER-DOWN	RF PRESCALER	13-BIT B COUNTER													5-BIT A COUNTER					CONTROL BITS	
DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

A5	A4	A3	A2	A1	A COUNTER DIVIDE RATIO
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
.	.	.	.	.	.
1	1	1	1	0	30
1	1	1	1	1	31

B13	B12	B11	.....	B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	0	1	NOT ALLOWED
0	0	0	.....	0	1	0	NOT ALLOWED
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	8188
1	1	1	.....	1	0	1	8189
1	1	1	.....	1	1	0	8190
1	1	1	.....	1	1	1	8191

P14	IF PRESCALER
0	16/17
1	32/33

P16	IF SECTION
0	NORMAL OPERATION
1	POWER-DOWN

N = BP + A, P IS PRESCALER VALUE SET BY P14.
B MUST BE GREATER THAN OR EQUAL TO A.
FOR CONTIGUOUS VALUES OF N, N_{MIN} IS (P^2–P).
A MUST BE LESS THAN P.

PROGRAM MODES

Tables IV and VII show how to set up the program modes in the ADF4217L family. The following should be noted:

1. IF and RF Analog Lock Detect indicate when the PLL is in lock. When the loop is locked, and either IF or RF Analog Lock Detect is selected, the MUXOUT pin will show a logic high with narrow low-going pulses. When the IF/RF Analog Lock Detect is chosen, the locked condition is indicated only when both IF and RF loops are locked.
2. The IF Counter Reset Mode resets the R and N counters in the IF section and also puts the IF charge pump into three-state. The RF Counter Reset Mode resets the R and N counters in the RF section and also puts the RF charge pump into three-state. The IF and RF Counter Reset Mode does both of the above.

   Upon removal of the reset bits, the N counter resumes counting in close alignment with the R counter (maximum error is one prescaler output cycle).
3. The Fastlock Mode uses MUXOUT to switch a second loop filter damping resistor to ground during Fastlock operation. Activation of Fastlock occurs whenever RF CP Gain in the RF Reference counter is set to 1.

POWER-DOWN

It is possible to program the ADF4217L family for either synchronous or asynchronous power-down on either the IF or RF side.

Synchronous IF Power-Down
Programming a "1" to P7 of the ADF4217L family will initiate a power-down. If P2 of the ADF4217L family has been set to "0" (normal operation), then a synchronous power-down is conducted. The device will automatically put the charge pump into three-state and then complete the power-down.

Asynchronous IF Power-Down
If P2 of the ADF4217L family has been set to "1" (three-state the IF charge pump) and P7 is subsequently set to "1," an asynchronous power-down is conducted. The device will go into power-down on the rising edge of LE, which latches the "1" to the IF Power-Down Bit (P7).

Synchronous RF Power-Down
Programming a "1" to P16 of the ADF4217L family will initiate a power-down. If P10 of the ADF4217L family has been set to "0" (normal operation), a synchronous power-down is conducted. The device will automatically put the charge pump into three-state and then complete the power-down.

Asynchronous RF Power-Down
If P10 of the ADF4217L family has been set to "1" (three-state the RF charge pump) and P16 is subsequently set to "1," an asynchronous power-down is conducted. The device will go into power-down on the rising edge of LE, which latches the "1" to the RF Power-Down Bit (P16).

Activation of either synchronous or asynchronous power-down forces the IF/RF loop's R and N dividers to their load state conditions, and the IF/RF input section is debiased to a high impedance state.

The REF_{IN} oscillator circuit is only disabled if both the IF and RF power-downs are set.

The input register and latches remain active and are capable of loading and latching data during all the power-down modes.

The IF/RF section of the devices will return to normal powered-up operation immediately upon LE latching a "0" to the appropriate power-down bit.

IF SECTION

Programmable IF Reference (R) Counter
If control bits C2, C1 are 0, 0, then the data is transferred from the input shift register to the 14-bit IF R counter. Table IV shows the input shift register data format for the IF R counter and the possible divide ratios.

IF Phase Detector Polarity
P1 sets the IF phase detector polarity. When the IF VCO characteristics are positive, this should be set to "1." When they are negative, it should be set to "0." See Table IV.

IF Charge Pump Three-State
P2 puts the IF charge pump into three-state mode when programmed to a "1." It should be set to "0" for normal operation. See Table IV.

IF Charge Pump Currents
P5 sets the IF charge pump current. With P5 set to "0," I_{CP} is 1.0 mA. With P5 set to "1," I_{CP} is 4.0 mA. See Table IV.

Programmable IF AB Counter
If control bits C2, C1 are 0, 1, the data in the input register is used to program the IF AB counter. For the ADF4217L/ADF4218L, the AB counter consists of a 6-bit swallow counter (A counter) and 11-bit programmable counter (B counter). Table V shows the input register data format for programming the IF AB counter and the possible divide ratios. The ADF4219L N counter consists of an 13-bit B counter and 5-bit A counter. Table VI shows the input register data format for programming the ADF4219L.

IF Prescaler Value
P6 in the IF AB counter latch sets the IF prescaler value. For the ADF4217L family, 8/9 or 16/17 prescalers are available. See Table V and Table VI.

IF Power-Down
Tables IV, V, and VI show the power-down bits in the ADF4217L family. See the Power-Down section for a functional description.

RF SECTION

Programmable RF Reference (R) Counter
If control bits C2, C1 are 1, 0, the data is transferred from the input shift register to the 14-bit RF R counter. Table VII shows the input shift register data format for the RF R counter and the possible divide ratios.

RF Phase Detector Polarity
P9 sets the RF phase detector polarity. When the RF VCO characteristics are positive, this should be set to "1." When they are negative, it should be set to "0." See Table VII.

RF Charge Pump Three-State
P10 puts the RF charge pump into three-state mode when programmed to a "1." It should be set to "0" for normal operation. See Table VII.

RF Program Modes
Tables IV and VII show how to set up the RF program modes.

RF Charge Pump Currents
P13 sets the RF charge pump current. With P13 set to "0," I_{CP} is 1.0 mA. With P13 set to "1," I_{CP} is 4.0 mA. See Table VII.

Programmable RF AB Counter
If control bits C2, C1 are 1, 1, the data in the input register is used to program the RF AB counter. For the ADF4217L/ADF4218L, the AB counter consists of a 6-bit swallow counter (A counter) and 11-bit programmable counter (B counter). Table VIII shows the input register data format for programming the RF AB counter and the possible divide ratios. The ADF4219L N counter consists of a 13-bit B counter and 5-bit A counter. Table IX shows the input register data format for programming the ADF4219L.

RF Prescaler Value
P14 in the RF AB counter latch sets the RF prescaler value. For the ADF4217L and ADF4218L family, 32/33 or 64/65 prescalers are available. See Table VIII. For the ADF4219L, the prescaler may be 16/17 or 32/33. See Table IX.

RF Power-Down
Tables VII, VIII, and IX show the power-down bits (Charge Pump Bit used for asynchronous in the ADF4217L family). See the Power-Down section for a functional description.

RF Fastlock
The RF CP Gain Bit (P13) of the RF N Register in the ADF4217L family is the Fastlock Enable Bit. The loop filter should be designed for the lower current setting. When Fastlock is enabled, the RF CP current is set to maximum value. Also, an extra loop filter damping resistor to ground is switched in using the MUXOUT pin, thus compensating for the change of loop dynamics when in Fastlock Mode. Since the RF CP Gain Bit is contained in the RF N counter, only one write is needed to program the new frequency and to initiate Fastlock. To come out of Fastlock, the RF CP Gain Bit should be returned to "0" and the extra damping resistor switched out.

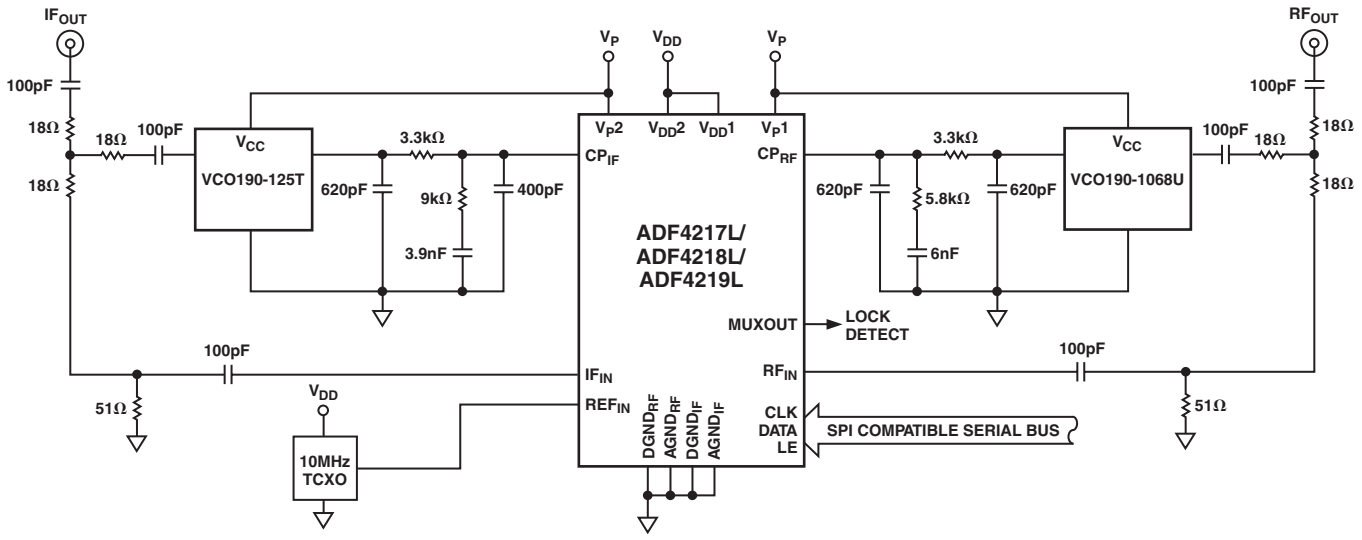
APPLICATIONS SECTION
Local Oscillator for GSM Handset Receiver
The diagram in Figure 7 shows the ADF4217L/ADF4218L/ADF4219L being used in a classic superheterodyne receiver to provide the required LOs (local oscillators). In this circuit, the reference input signal is applied to the circuit at $f_{REF_{IN}}$ and is being generated by a 13 MHz temperature controlled crystal oscillator. In order to have a channel spacing of 200 kHz (the GSM standard), the reference input must be divided by 65, using the on-chip reference counter.

The RF output frequency range is 1050 MHz to 1085 MHz. Loop filter component values are chosen so that the loop bandwidth is 20 kHz. The synthesizer is set up for a charge pump current of 4.0 mA, and the VCO sensitivity is 15.6 MHz/V. The IF output is fixed at 125 MHz. The IF loop bandwidth is chosen to be 20 kHz with a channel spacing of 200 kHz. Loop filter component values are chosen accordingly.

Local Oscillator for WCDMA Receiver
Figure 8 shows the ADF4217L/ADF4218L/ADF4219L being used to generate the local oscillator frequencies in a wideband CDMA (WCDMA) system.

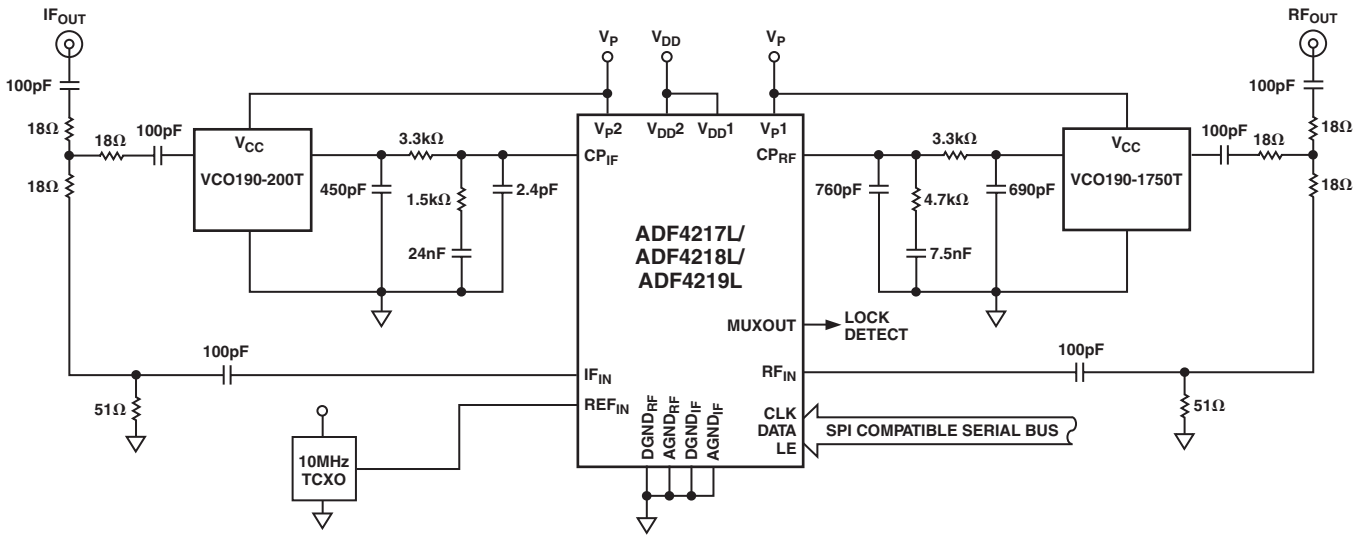
The RF output range needed is 1720 MHz to 1780 MHz. The VCO190-1750T from Varil-L will accomplish that. Channel spacing is 200 kHz, the loop bandwidth of the loop filter is 20 kHz, and the VCO sensitivity is 32 MHz/V. A charge pump current of 4.0 mA is used and the desired phase margin for the loop is 45 degrees.

The IF output is fixed at 200 MHz. The VCO190-200T is used. It has a sensitivity of 11.5 MHz/V. Channel spacing and loop bandwidth are chosen the same as the RF side.



DECOUPLING CAPACITORS (22μF/10pF) ON V_{DD}, V_P OF THE ADF4217L/ADF4218L/ADF4219L.
THE TCXO AND ON V_{CC} OF THE VCOs HAVE BEEN OMITTED FROM THE DIAGRAM TO AID CLARITY.

Figure 7. Local Oscillator Design for GSM Receiver



DECOUPLING CAPACITORS (22μF/10pF) ON V_{DD}, V_P OF THE ADF4217L/ADF4218L/ADF4219L.
THE TCXO AND ON V_{CC} OF THE VCOs HAVE BEEN OMITTED FROM THE DIAGRAM TO AID CLARITY.

Figure 8. Local Oscillator Design for WCDMA System

In this circuit, the reference input signal is applied to the circuit at REF_{IN} by a 10 MHz TCXO (temperature controlled crystal oscillator).

INTERFACING

The ADF4217L/ADF4218L/ADF4219L family has a simple SPI® compatible serial interface for writing to the device. SCLK, SDATA, and LE control the data transfer. When LE (latch enable) goes high, the 22 bits that have been clocked into the input register on each rising edge of SCLK will get transferred to the appropriate latch. See Figure 1 for the timing diagram and Table I for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 909 kHz or one update every 1.1 μs. This is certainly more than adequate for systems that will have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 9 shows the interface to the ADuC812 MicroConverter®. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051 based microcontroller. The MicroConverter is set up for SPI Master Mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF421xL family needs a 22-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

On first applying power to the ADF4217L family, it needs four writes (one each to the R counter latch and the AB counter latch for both RF1 and RF2 side) for the output to become active.

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed will be about 180 kHz.

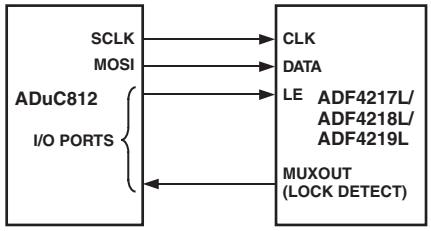


Figure 9. ADuC812 to ADF421xL Interface

ADSP2181 Interface

Figure 10 shows the interface between the ADF4217L family and the ADSP-21xx digital signal processor. As previously discussed, the ADF4217L family needs a 22-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 22-bit word. To program each 22-bit latch, store the three 8-bit bytes, enable the Autobuffered Mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

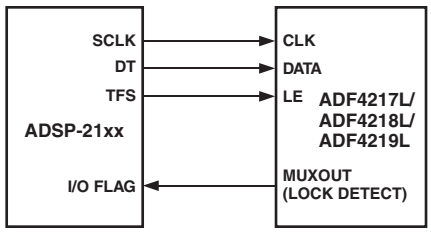
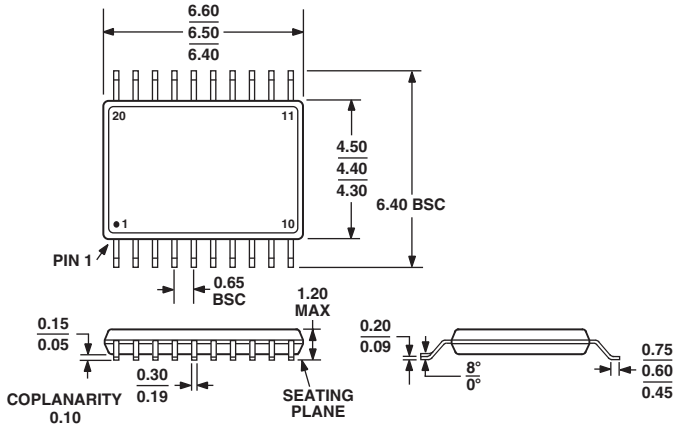


Figure 10. ADSP-21xx to ADF421xL Interface

OUTLINE DIMENSIONS

20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)

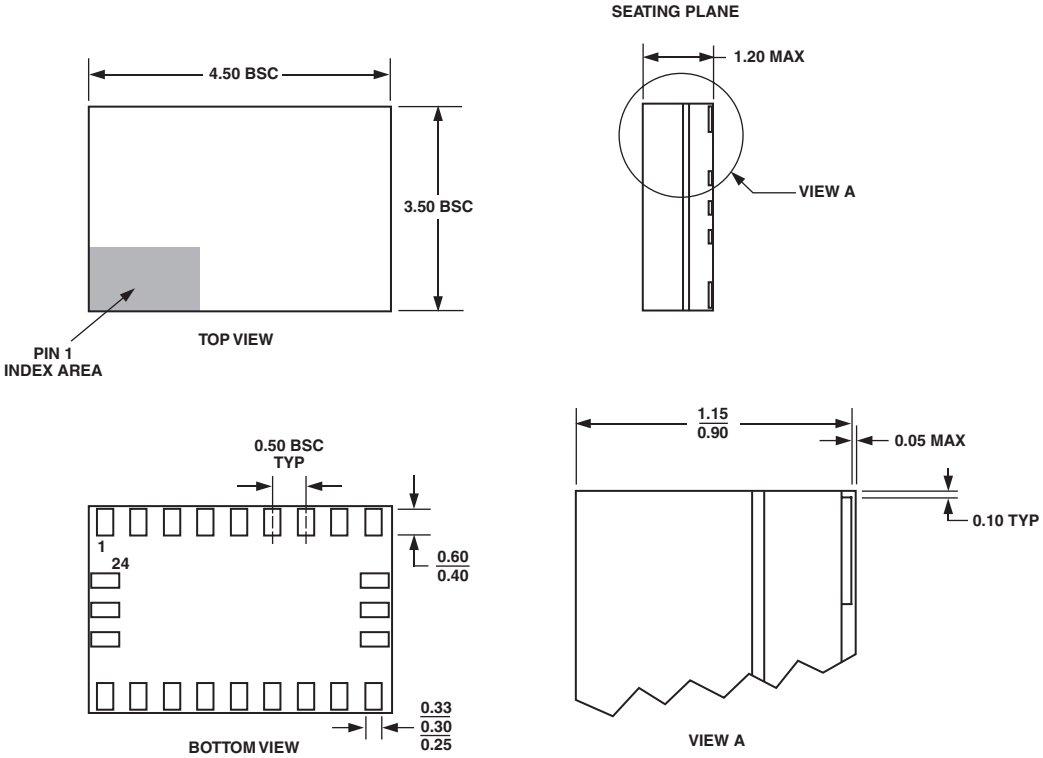
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AC

24-Leadless Chip Array CASON [LGA]
(CC-24)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-208, ECEA-1

Revision History

Location	Page
5/03—Data Sheet changed from REV. B to REV. C.	
Change to SPECIFICATIONS	2
Change to TPC 8	8
Change to OUTLINE DIMENSIONS	22
7/02—Data Sheet changed from REV. A to REV. B.	
Change to ADF4219L SENSITIVITY SPECIFICATION	2
6/02—Data Sheet changed from REV. 0 to REV. A.	
Changes to FUNCTIONAL BLOCK DIAGRAM	1
Changes to SPECIFICATIONS	2
Changes to ABSOLUTE MAXIMUM RATINGS	4
Changes to CASON package drawing	22