

DATA SHEET

74LVC157A

Quad 2-input multiplexer

Product specification
Supercedes data of 1997 Nov 07
IC24 Data Handbook

1998 Jul 29

Quad 2-input multiplexer

74LVC157A

FEATURES

- Wide supply voltage range of 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- CMOS lower power consumption
- Direct interface with TTL levels
- 5 Volt tolerant inputs, for interfacing with 5 Volt logic

DESCRIPTION

The 74LVC157A is a high-performance, low-power, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC157A is a quad 2-input multiplexer which select 4 bits of data from two sources under the control of a common data select

input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input (\bar{E}) is active LOW. When \bar{E} is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions. Moving the data from two groups of registers to four common output buses is a common use of the 74LV157. The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The 74LVC157A is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nI_0 , nI_1 , to nY \bar{E} to nY S to nY	$C_L = 50 \text{ pF}$; $V_{CC} = 3.3 \text{ V}$	3.1 3.0 3.3	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	$V_I = \text{GND to } V_{CC}^1$	33	pF

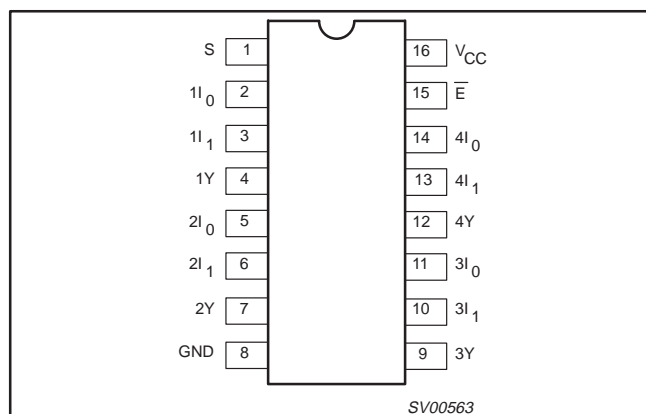
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic SO	-40°C to $+85^{\circ}\text{C}$	74LVC157A D	74LVC157A D	SOT109-1
16-Pin Plastic SSOP Type II	-40°C to $+85^{\circ}\text{C}$	74LVC157A DB	74LVC157A DB	SOT338-1
16-Pin Plastic TSSOP Type I	-40°C to $+85^{\circ}\text{C}$	74LVC157A PW	74LVC157APW DH	SOT403-1

PIN CONFIGURATION



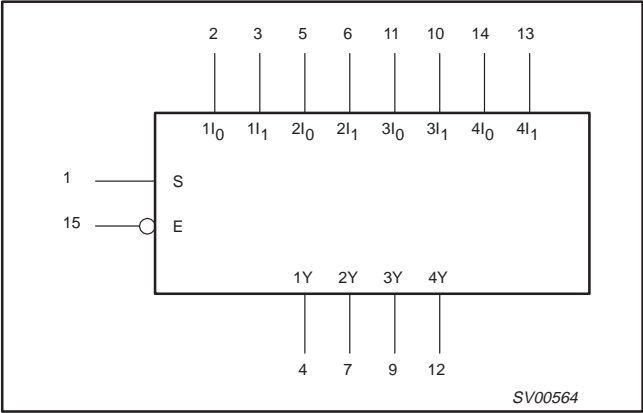
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	S	Common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	Data inputs from sources 0
3, 6, 10, 13	$1I_1$ to $4I_1$	Data inputs from sources 1
4, 7, 9, 12	1Y to 4Y	Multiplexer outputs
8	GND	Ground (0 V)
15	\bar{E}	Enable input (active LOW)
16	V_{CC}	Positive supply voltage

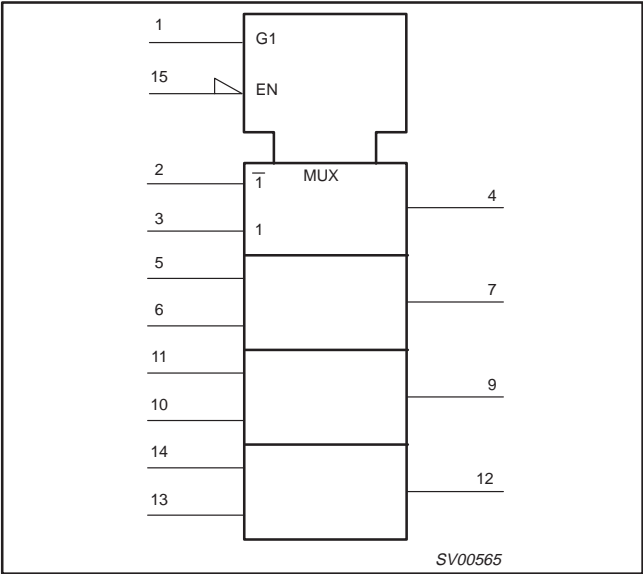
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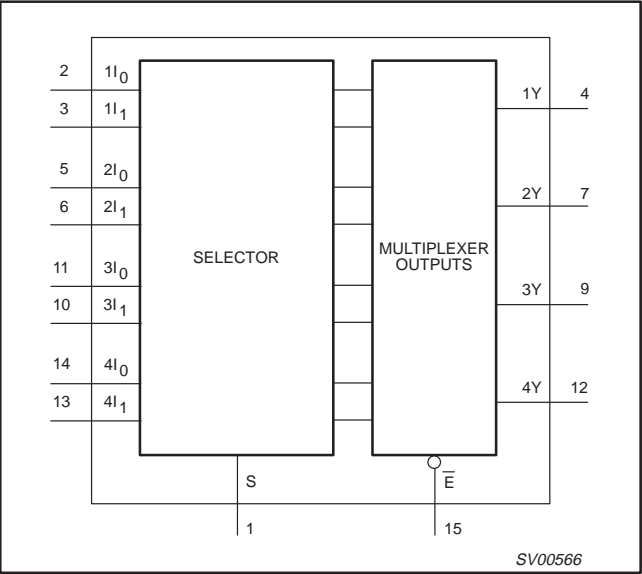
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM

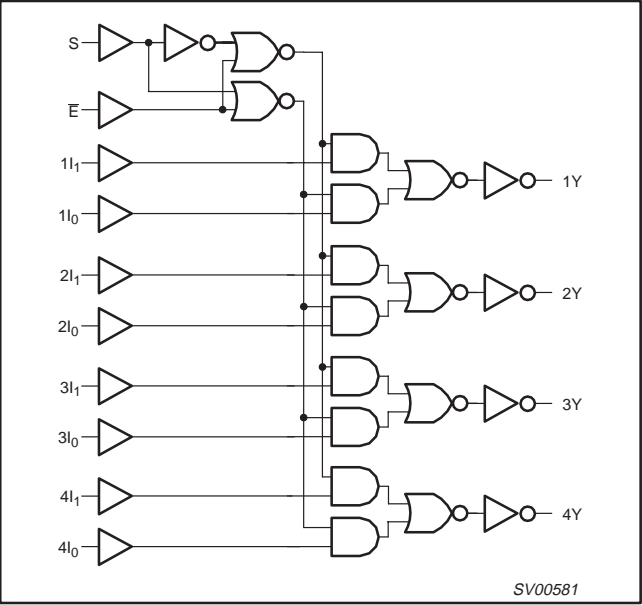


FUNCTION TABLE

INPUTS				OUTPUTS
\overline{E}	S	nI_0	nI_1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	Note 2	-0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage	Note 2	-0.5 to $V_{CC} + 0.5$	V
I_O	DC output diode current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 2.7 to 3.6V	2.0			
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 2.7 to 3.6V			0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.5			V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} - 0.2	V _{CC}		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -18mA	V _{CC} - 0.6			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} - 0.8			
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.40	V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		GND	0.20	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA			0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND		± 0.1	± 5	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0		0.1	10	μA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		5	500	μA

NOTE:1. All typical values are measured at V_{CC} = 3.3V and T_{amb} = 25°C.**AC CHARACTERISTICS**GND = 0 V; t_r = t_f ≤ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = -40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V _{CC} = 3.3V ± 0.3V			V _{CC} = 2.7V		V _{CC} = 1.2V	
			MIN	TYP ¹	MAX	MIN	MAX	TYP	
t _{PHL} /t _{PLH}	Propagation delay n _{I0} to nY; n _{I1} to nY	Figure 2, 3	1.5	3.1	5.7	1.5	6.7	12	ns
t _{PHL} /t _{PLH}	Propagation delay E to nY	Figure 1, 3	1.5	3.0	6.3	1.5	7.3	11	ns
t _{PHL} /t _{PLH}	Propagation delay S to nY	Figure 2, 3	1.5	3.3	6.8	1.5	7.8	13	ns

NOTE:1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

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AC WAVEFORMS

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7\text{ V}$
 $V_M = 1.5\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$
 $V_X = V_{OL} + 0.3\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$
 $V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7\text{ V}$
 $V_Y = V_{OH} - 0.3\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$
 $V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7\text{ V}$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

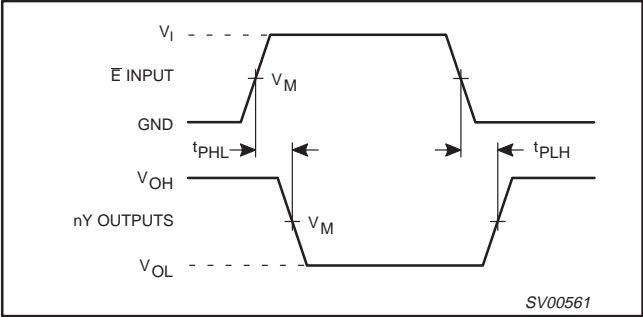


Figure 1. Enable input (E) to output (nY) propagation delays.

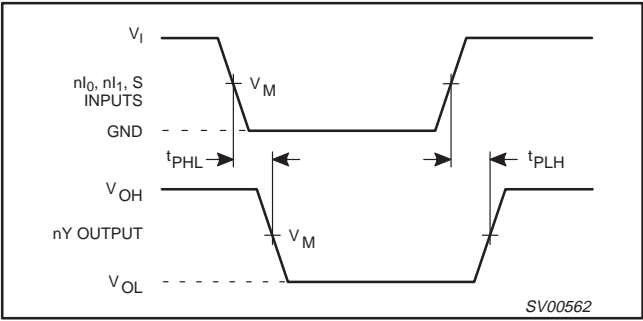


Figure 2. Data inputs (nI_0 , nI_1) and common data select input (S) to output (nY) propagation delays.

TEST CIRCUIT

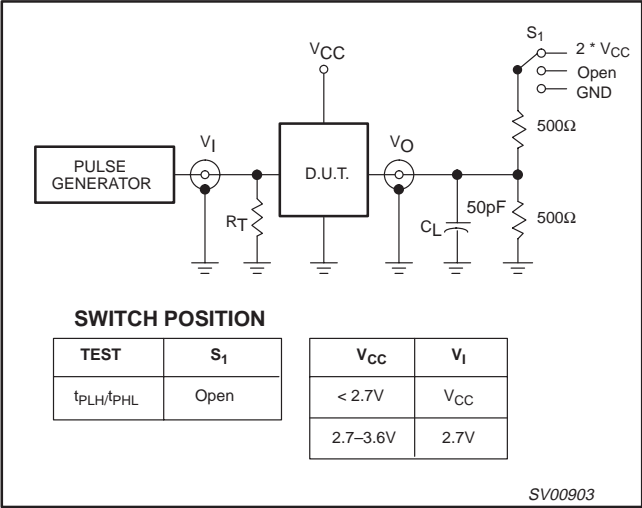


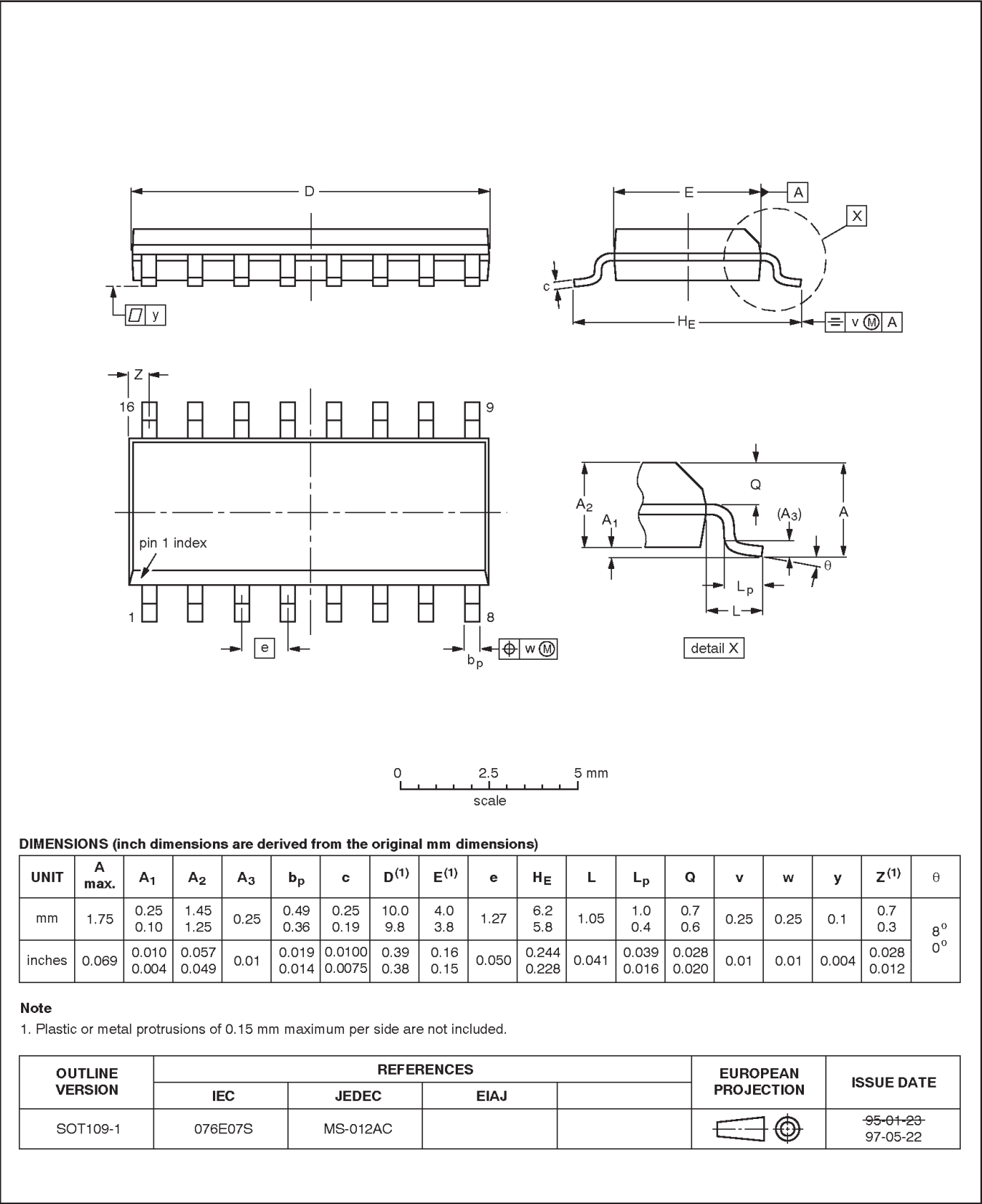
Figure 3. Load circuitry for switching times.

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

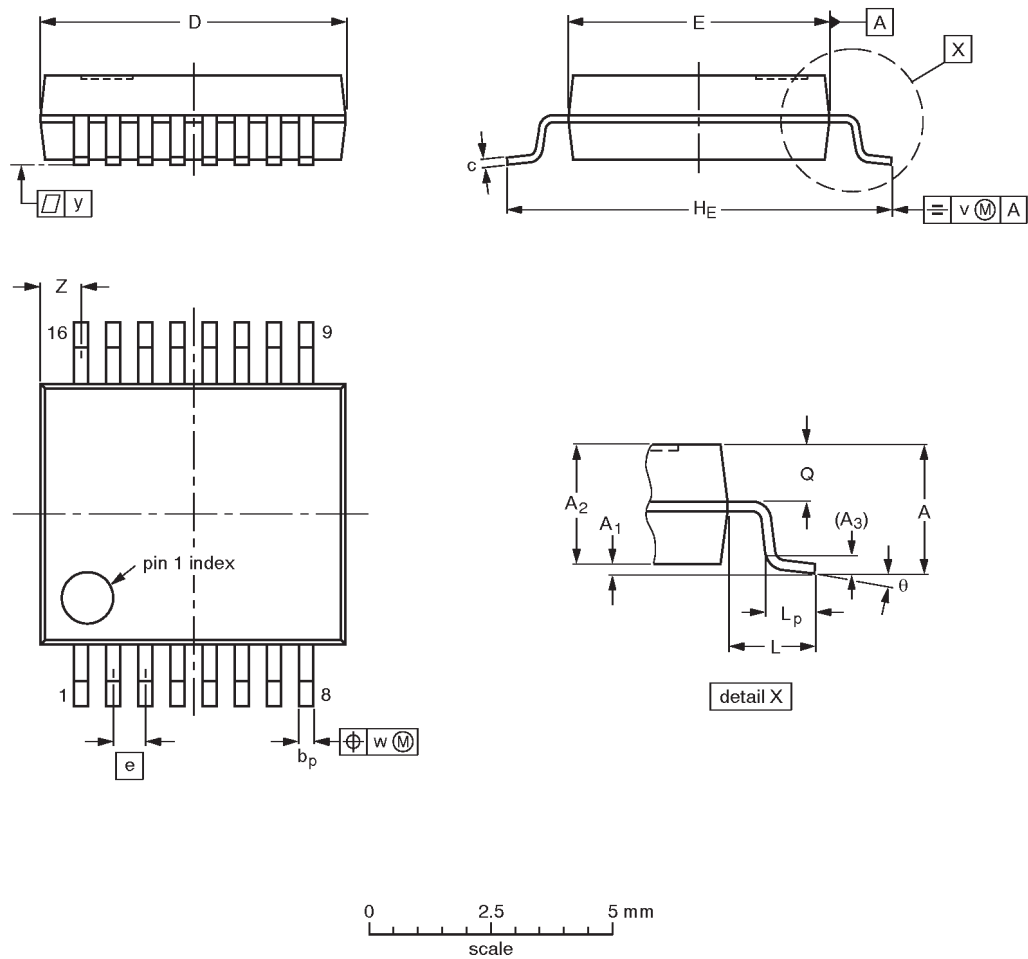


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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

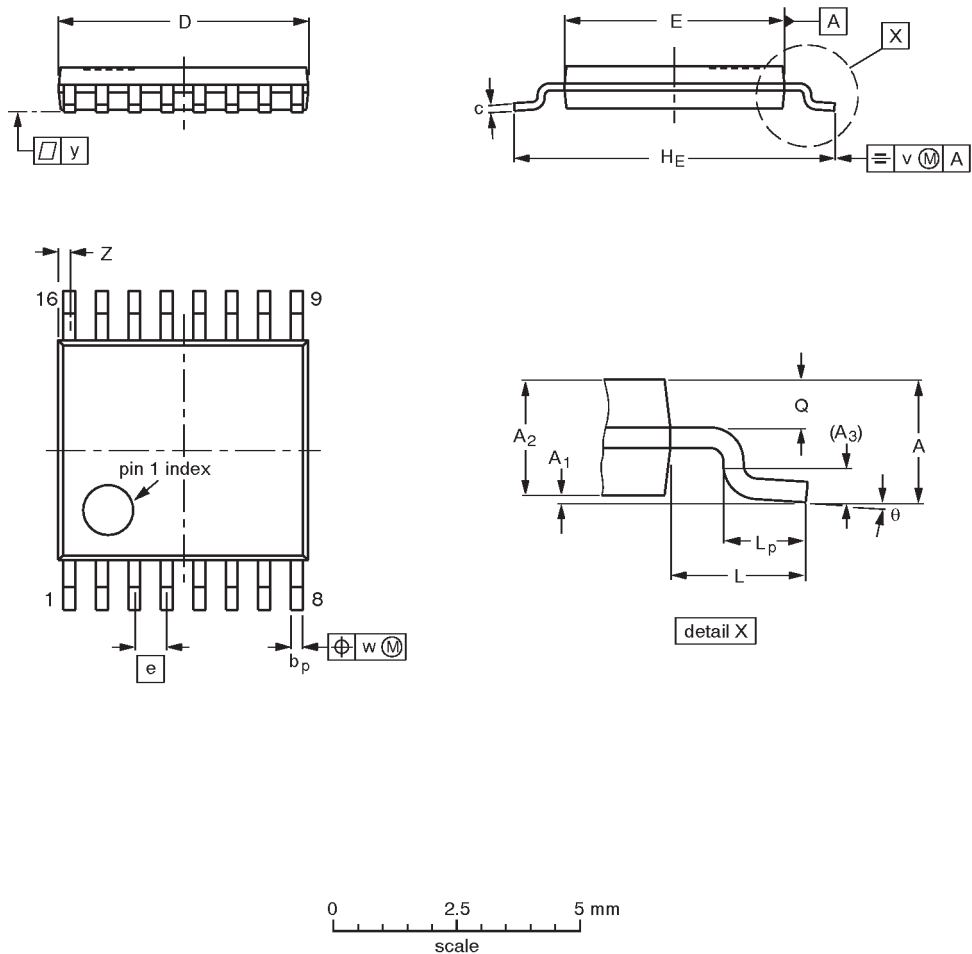
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14 95-02-04

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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