



# 12-Bit Buffered Multiplying CMOS D/A Converters

## PM-7545/PM-7645

### FEATURES

- Preadjusted Full Scale .....  $\pm 1$  LSB Maximum Gain Error
- Low Gain Temperature Coefficient ..... 2ppm/ $^{\circ}$ C
- Small 20-Pin 0.3" Wide DIP
- PM-7545 TTL Compatible for  $V_{DD} = 5V$
- PM-7645 TTL and 5V CMOS Compatible for  $V_{DD} = 15V$
- High ESD Resistance
- Available in Die Form

### ORDERING INFORMATION<sup>†</sup>

| MAXIMUM<br>GAIN ERROR<br>$T_A = +25^{\circ}$ C | PACKAGE: 20-PIN                                                   |                                                                               |                                                                 |
|------------------------------------------------|-------------------------------------------------------------------|-------------------------------------------------------------------------------|-----------------------------------------------------------------|
|                                                | MILITARY*<br>TEMPERATURE<br>-55 $^{\circ}$ C to +125 $^{\circ}$ C | EXTENDED<br>INDUSTRIAL<br>TEMPERATURE<br>-40 $^{\circ}$ C to +85 $^{\circ}$ C | COMMERCIAL<br>TEMPERATURE<br>0 $^{\circ}$ C to +70 $^{\circ}$ C |
| $\pm 1$ LSB                                    | PM7545AR                                                          | PM7545ER                                                                      | PM7545GP                                                        |
| $\pm 3$ LSB                                    | PM7545BR                                                          | PM7545FR                                                                      | —                                                               |
| $\pm 3$ LSB                                    | PM7545BRCB83                                                      | PM7545FP                                                                      | —                                                               |
| $\pm 3$ LSB                                    | —                                                                 | PM7545FPC                                                                     | —                                                               |
| $\pm 3$ LSB                                    | —                                                                 | PM7545FS                                                                      | —                                                               |
| $\pm 1$ LSB                                    | PM7645AR                                                          | PM7645ER                                                                      | PM7645GP                                                        |
| $\pm 3$ LSB                                    | PM7645BR                                                          | PM7645FR                                                                      | —                                                               |
| $\pm 3$ LSB                                    | —                                                                 | PM7645FP                                                                      | —                                                               |
| $\pm 3$ LSB                                    | —                                                                 | PM7645FPC                                                                     | —                                                               |
| $\pm 3$ LSB                                    | —                                                                 | PM7645FS                                                                      | —                                                               |

\* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

### CROSS REFERENCE

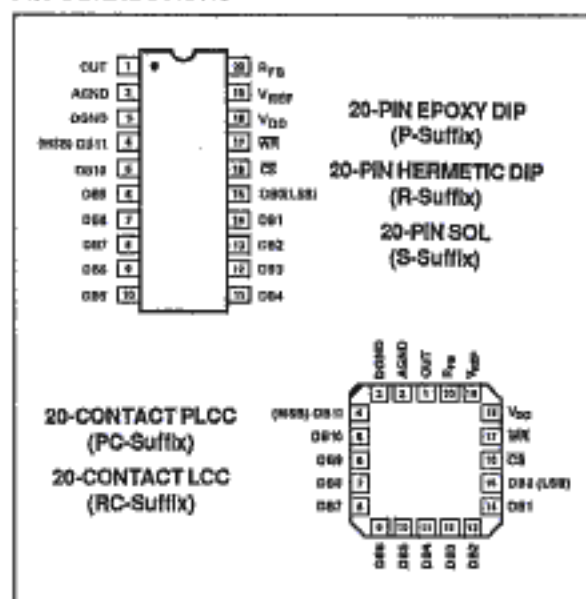
| PMI       | ADI       | TEMPERATURE RANGE |
|-----------|-----------|-------------------|
| PM7545AR  | AD7545GUD | MILITARY          |
| PM7545BR  | AD7545UD  |                   |
| PM7545BR  | AD7545TD  |                   |
| PM7545BR  | AD7545SD  |                   |
| PM7545ER  | AD7545GQQ | INDUSTRIAL        |
| PM7545FR  | AD7545CQ  |                   |
| PM7545FR  | AD7545BQ  |                   |
| PM7545FR  | AD7545AQ  |                   |
| PM7545GP  | AD7545GLN | COMMERCIAL        |
| PM7545FP  | AD7545LN  |                   |
| PM7545FP  | AD7545KN  |                   |
| PM7545FPC | AD7545JN  |                   |

### GENERAL DESCRIPTION

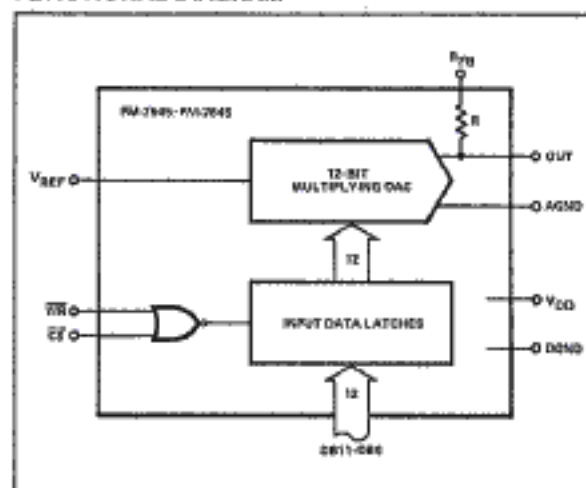
The PM-7545/PM-7645 are 12-bit CMOS multiplying DACs with internal data latches. Digital data is input in a 12-bit wide data format, while CS and WR control inputs are active low. During this time the latches are transparent allowing digital inputs direct connection to the DAC. When WR is returned to logic high, the current data word in the latch is saved.

The PM-7545 operates from 5 to 15 volt power supplies, offering TTL logic compatibility at  $V_{DD}$  of 5V and CMOS logic compatibility at  $V_{DD}$  of 15V. The PM-7645 is specified for operation at  $V_{DD}$  of 15V, offering TTL logic input compatibility.

### PIN CONNECTIONS



### FUNCTIONAL DIAGRAM



## PM-7545/PM-7645

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**ABSOLUTE MAXIMUM RATINGS** ( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

|                                         |                                             |
|-----------------------------------------|---------------------------------------------|
| $V_{DD}$ to DGND                        | -0.3, +17V                                  |
| Digital Input Voltage to DGND           | -0.3, $V_{DD}$                              |
| AGND to DGND                            | -0.3, $V_{DD}$                              |
| $V_{REF}$ , $V_{REF}$ to DGND           | $\pm 25\text{V}$                            |
| $V_{PIN 1}$ to DGND                     | -0.3, $V_{DD}$                              |
| Operating Temperature Range             |                                             |
| Military (AR, BR) Grades                | $-55^\circ\text{C}$ to $+125^\circ\text{C}$ |
| Industrial (ER, FR, FP, FPC, FS) Grades | $-40^\circ\text{C}$ to $+85^\circ\text{C}$  |
| Commercial (GP) Grade                   | $0^\circ\text{C}$ to $+70^\circ\text{C}$    |
| Junction Temperature                    | $+150^\circ\text{C}$                        |
| Storage Temperature                     | $-65^\circ\text{C}$ to $+150^\circ\text{C}$ |
| Lead Temperature (Soldering, 60 sec)    | $+300^\circ\text{C}$                        |

| PACKAGE TYPE            | $\theta_{JA}$ (Note 1) | $\theta_{JC}$ | UNITS              |
|-------------------------|------------------------|---------------|--------------------|
| 20-Pin Hermetic DIP (R) | 76                     | 11            | $^\circ\text{C/W}$ |
| 20-Pin Plastic DIP (P)  | 89                     | 27            | $^\circ\text{C/W}$ |
| 20-Contact LCC (RC, TC) | 88                     | 33            | $^\circ\text{C/W}$ |
| 20-Pin SOL (S)          | 88                     | 25            | $^\circ\text{C/W}$ |
| 20-Contact PLCC (PC)    | 73                     | 33            | $^\circ\text{C/W}$ |

## NOTE:

1.  $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for CerDIP, P-DIP, and LCC packages;  $\theta_{JC}$  is specified for device soldered to printed circuit board for SOL and PLCC packages.

## CAUTION:

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
- Do not apply voltages higher than  $V_{DD}$  or less than GND potential on any terminal except  $V_{REF}$ .
- The digital inputs are Zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper antistatic handling procedures.
- Remove power before inserting or removing units from their sockets.

**ELECTRICAL CHARACTERISTICS** at  $V_{DD} = +5\text{V}$ ,  $V_{REF} = +10\text{V}$ ,  $V_{OUT} = 0\text{V}$ , AGND = DGND = 0V;  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  apply for PM-7545AR/BR;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  apply for PM-7545ER/FR/FP/FPC/FS;  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$  apply for PM-7545GP, unless otherwise noted. 15V operating characteristics are shown on the following pages.

| PARAMETER                                          | SYMBOL            | CONDITIONS                                                                                                                                | PM-7545A/E/G |     |                 | PM-7545B/F |     |                 | UNITS             |
|----------------------------------------------------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------|--------------|-----|-----------------|------------|-----|-----------------|-------------------|
|                                                    |                   |                                                                                                                                           | MIN          | TYP | MAX             | MIN        | TYP | MAX             |                   |
| STATIC ACCURACY                                    |                   |                                                                                                                                           |              |     |                 |            |     |                 |                   |
| Resolution                                         | N                 |                                                                                                                                           | 12           | —   | —               | 12         | —   | —               | Bits              |
| Relative Accuracy                                  | INL               | T <sub>A</sub> = Full Temp. Range                                                                                                         | —            | —   | ±1/2            | —          | —   | ±1/2            | LSB               |
| Differential Nonlinearity                          | DNL               | T <sub>A</sub> = Full Temp. Range<br>(Note 1)                                                                                             | —            | —   | ±1              | —          | —   | ±1              | LSB               |
| Gain Error<br>(Notes 2, 3)                         | G <sub>ERR</sub>  | T <sub>A</sub> = +25°C<br>T <sub>A</sub> = Full Temp. Range                                                                               | —            | —   | ±1<br>±2        | —          | —   | ±3<br>±4        | LSB               |
| Gain Temperature Coefficient<br>ΔGain/ΔTemperature | TCG <sub>FS</sub> | (Note 4)                                                                                                                                  | —            | ±2  | ±5              | —          | ±2  | ±5              | ppm/°C            |
| DC Supply Rejection<br>ΔGain/ΔV <sub>DD</sub>      | PSR               | T <sub>A</sub> = +25°C<br>T <sub>A</sub> = Full Temp. Range<br>(ΔV <sub>DD</sub> = ±5%)                                                   | —            | —   | 0.002<br>0.004  | —          | —   | 0.002<br>0.004  | %/%               |
| Output Leakage Current at OUT                      | I <sub>LKB</sub>  | T <sub>A</sub> = +25°C, WR = CS = 0V,<br>All Digital Inputs = 0V<br>T <sub>A</sub> = Full Temp. Range<br>A/B Versions<br>E/F/G/H Versions | —            | —   | 10<br>200<br>50 | —          | —   | 10<br>200<br>50 | nA                |
| DYNAMIC PERFORMANCE                                |                   |                                                                                                                                           |              |     |                 |            |     |                 |                   |
| Propagation Delay<br>(Notes 4, 5, 6, 7)            | t <sub>PD</sub>   | T <sub>A</sub> = +25°C<br>(OUT Load = 100f, C <sub>EXT</sub> = 13pF)                                                                      | —            | —   | 300<br>—        | —          | —   | 300<br>—        | ns                |
| Current Settling Time                              | t <sub>s</sub>    | T <sub>A</sub> = Full Temp. Range<br>(To 1/2 LSB) (Note 4)<br>I <sub>OUT</sub> Load = 100Ω                                                | —            | —   | 1               | —          | —   | 1               | μs                |
| Digital Charge Injection                           | Q                 | T <sub>A</sub> = +25°C<br>T <sub>A</sub> = Full Temp. Range<br>V <sub>REF</sub> = AGND (Note 4)                                           | —            | —   | 300<br>400      | —          | —   | 300<br>400      | nA                |
| AC Feedthrough at I <sub>OUT</sub>                 | FT                | T <sub>A</sub> = Full Temp. Range<br>V <sub>REF</sub> = ±10V, f = 10kHz<br>All Digital Inputs = 0V                                        | —            | 5   | —               | —          | 5   | —               | mV <sub>p-p</sub> |

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**ELECTRICAL CHARACTERISTICS** at  $V_{DD} = +5V$ ,  $V_{REF} = +10V$ ,  $V_{OUT} = 0V$ ,  $AGND = DGND = 0V$ ;  $T_A = -55^\circ C$  to  $+125^\circ C$  apply for PM-7545AR/BR;  $T_A = -40^\circ C$  to  $+85^\circ C$  apply for PM-7545ER/FR/FP/FPC/FS;  $T_A = 0^\circ C$  to  $+70^\circ C$  apply for PM-7545GP, unless otherwise noted. 15V operating characteristics are shown on the following pages. *Continued*

| PARAMETER                                    | SYMBOL           | CONDITIONS                                                                                    | PM-7545A/E/G |     |     | PM-7545B/F |     |     | UNITS |
|----------------------------------------------|------------------|-----------------------------------------------------------------------------------------------|--------------|-----|-----|------------|-----|-----|-------|
|                                              |                  |                                                                                               | MIN          | TYP | MAX | MIN        | TYP | MAX |       |
| REFERENCE INPUT                              |                  |                                                                                               |              |     |     |            |     |     |       |
| Input Resistance<br>(Pin 18 to GND)          | R <sub>REF</sub> | T <sub>A</sub> = Full Temp. Range<br>Input Resistance                                         | 7            | 11  | 15  | 7          | 11  | 15  | kΩ    |
| ANALOG OUTPUTS                               |                  |                                                                                               |              |     |     |            |     |     |       |
| Output Capacitance<br>(Note 4)               | C <sub>OUT</sub> | T <sub>A</sub> = Full Temp. Range<br>DB0-DB11 = 0V, WR = CS = 0V                              | —            | —   | 70  | —          | —   | 70  | pF    |
| C <sub>OUT</sub>                             |                  | DB0-DB11 = V <sub>DD</sub> , WR = CS = 0V                                                     | —            | —   | 150 | —          | —   | 150 |       |
| DIGITAL INPUTS                               |                  |                                                                                               |              |     |     |            |     |     |       |
| Input High Voltage                           | V <sub>AH</sub>  | T <sub>A</sub> = Full Temp. Range                                                             | 2.4          | —   | —   | 2.4        | —   | —   | V     |
| Input Low Voltage                            | V <sub>AL</sub>  |                                                                                               | —            | —   | 0.8 | —          | —   | 0.8 |       |
| Input Current                                | I <sub>IN</sub>  | T <sub>A</sub> = +25°C                                                                        | —            | —   | 1   | —          | —   | 1   | μA    |
|                                              |                  | T <sub>A</sub> = Full Temp. Range                                                             | —            | —   | 10  | —          | —   | 10  |       |
| Input Capacitance<br>DB0-DB11, WR, CS        | C <sub>IN</sub>  | T <sub>A</sub> = Full Temp. Range<br>V <sub>IN</sub> = 0 (Note 4)                             | —            | —   | 8   | —          | —   | 8   | pF    |
| SWITCHING CHARACTERISTICS<br>(Notes 4, 5, 8) |                  | See Timing Diagram                                                                            |              |     |     |            |     |     |       |
| Chip Select to<br>Write Setup Time           | t <sub>CS</sub>  | T <sub>A</sub> = +25°C                                                                        | 260          | 200 | —   | 260        | 200 | —   | ns    |
|                                              |                  | T <sub>A</sub> = Full Temp. Range                                                             | 380          | 270 | —   | 380        | 270 | —   |       |
| Chip Select to<br>Write Hold Time            | t <sub>CH</sub>  | T <sub>A</sub> = Full Temp. Range                                                             | 0            | —   | —   | 0          | —   | —   | ns    |
| Write Pulse<br>Width                         | t <sub>WH</sub>  | T <sub>A</sub> = +25°C                                                                        | 250          | 175 | —   | 250        | 175 | —   | ns    |
|                                              |                  | T <sub>A</sub> = Full Temp. Range                                                             | 380          | 270 | —   | 380        | 270 | —   |       |
| Data Setup<br>Time                           | t <sub>DS</sub>  | T <sub>A</sub> = +25°C                                                                        | 140          | 100 | —   | 140        | 100 | —   | ns    |
|                                              |                  | T <sub>A</sub> = Full Temp. Range                                                             | 210          | 150 | —   | 210        | 150 | —   |       |
| Data Hold Time                               | t <sub>DH</sub>  | T <sub>A</sub> = Full Temp. Range                                                             | 10           | —   | —   | 10         | —   | —   | ns    |
| POWER SUPPLY                                 |                  |                                                                                               |              |     |     |            |     |     |       |
| Supply Current                               | I <sub>DD</sub>  | T <sub>A</sub> = Full Temp. Range<br>(All Digital Inputs V <sub>AH</sub> or V <sub>AL</sub> ) | —            | —   | 2   | —          | —   | 2   | mA    |
|                                              | I <sub>DD</sub>  | T <sub>A</sub> = +25°C                                                                        | —            | 2   | 90  | —          | 2   | 100 | μA    |
|                                              |                  | T <sub>A</sub> = Full Temp. Range<br>(All Digital Inputs 0V or V <sub>DD</sub> )              | —            | 5   | 100 | —          | 5   | 100 |       |

**NOTES:**

- 12-bit monotonic over full temperature range.
- Includes the effects of 5ppm max. gain T.C.
- Using internal  $R_{DD}$ , DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
- GUARANTEED and NOT TESTED.
- From digital input change to 90% of final analog output.
- All digital inputs = 0V to  $V_{DD}$  or  $V_{DD}$  to 0V.
- Logic inputs are MOS gates, typical input current (at  $+25^\circ C$ ) is less than 1nA.
- Sample tested at  $+25^\circ C$  to ensure compliance.
- Chip select  $\overline{CS}$  must be coincident or present before and/or after write  $\overline{WR}$ ; that is,  $t_{CS} \geq t_{WH}$ ,  $t_{CH} \geq 0$ .

## PM-7545/PM-7645

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ELECTRICAL CHARACTERISTICS at  $V_{DD} = +15V$ ,  $V_{REF} = +10V$ ,  $V_{OUT} = 0V$ ,  $AGND = DGND = 0V$ ;  $T_A = -55^\circ C$  to  $+125^\circ C$  apply for PM-7545/PM-7645AR/BF;  $T_A = -40^\circ C$  to  $+85^\circ C$  apply for PM-7545/PM-7645ER/FR/FP/FPC/FS;  $T_A = 0^\circ C$  to  $+70^\circ C$  apply for PM-7545/PM-7645GP, unless otherwise noted.

| PARAMETER                                          | SYMBOL            | CONDITIONS                                                                                                                                    | PM-7545A/E/G<br>PM-7645A/E/G |     |                 | PM-7545B/F<br>PM-7645B/F |     |                 | UNITS            |
|----------------------------------------------------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|-----|-----------------|--------------------------|-----|-----------------|------------------|
|                                                    |                   |                                                                                                                                               | MIN                          | TYP | MAX             | MIN                      | TYP | MAX             |                  |
| STATIC ACCURACY                                    |                   |                                                                                                                                               |                              |     |                 |                          |     |                 |                  |
| Resolution                                         | N                 |                                                                                                                                               | 12                           | —   | —               | 12                       | —   | —               | Bits             |
| Relative Accuracy                                  | INL               | T <sub>A</sub> = Full Temp. Range                                                                                                             | —                            | —   | ±1/2            | —                        | —   | ±1/2            | LSB              |
| Differential Nonlinearity                          | DNL               | T <sub>A</sub> = Full Temp. Range<br>(Note 1)                                                                                                 | —                            | —   | ±1              | —                        | —   | ±1              | LSB              |
| Gain Error<br>(Notes 2, 3)                         | G <sub>FSR</sub>  | T <sub>A</sub> = +25°C<br>T <sub>A</sub> = Full Temp. Range                                                                                   | —                            | —   | ±1<br>±2        | —                        | —   | ±3<br>±4        | LSB              |
| Gain Temperature Coefficient<br>ΔGain/ΔTemperature | TCG <sub>FS</sub> | (Note 4)                                                                                                                                      | —                            | ±2  | ±5              | —                        | ±2  | ±5              | ppm/°C           |
| DC Supply Rejection<br>ΔGain/ΔV <sub>DD</sub>      | PSR               | T <sub>A</sub> = +25°C<br>T <sub>A</sub> = Full Temp. Range (ΔV <sub>DD</sub> = ±5%)                                                          | —                            | —   | 0.002<br>0.004  | —                        | —   | 0.002<br>0.004  | %/%              |
| Output Leakage Current at OUT                      | I <sub>LKG</sub>  | T <sub>A</sub> = +25°C, WR = CS = 0V,<br>All Digital Inputs = 0V<br><br>T <sub>A</sub> = Full Temp. Range<br>A/B Versions<br>E/F/G/H Versions | —                            | —   | 10<br>200<br>50 | —                        | —   | 10<br>200<br>50 | nA               |
| DYNAMIC PERFORMANCE                                |                   |                                                                                                                                               |                              |     |                 |                          |     |                 |                  |
| Propagation Delay<br>(Notes 4, 5, 6, 7)            | t <sub>PD</sub>   | T <sub>A</sub> = +25°C<br>(OUT Load = 100fF, C <sub>EXT</sub> = 13pF)                                                                         | —                            | —   | 250             | —                        | —   | 250             | ns               |
| Current Settling Time                              | t <sub>s</sub>    | T <sub>A</sub> = Full Temp. Range<br>(To 1/2 LSB) (Note 4)<br>I <sub>OUT</sub> Load = 100fF                                                   | —                            | —   | 1               | —                        | —   | 1               | μs               |
| Digital Charge Injection                           | Q                 | T <sub>A</sub> = +25°C<br>T <sub>A</sub> = Full Temp. Range<br>V <sub>REF</sub> = AGND (Note 4)                                               | —                            | —   | 250<br>300      | —                        | —   | 250<br>300      | nVs              |
| AC Feedthrough at I <sub>OUT</sub>                 | FT                | T <sub>A</sub> = Full Temp. Range<br>V <sub>REF</sub> = ±10V, f = 10kHz<br>All Digital Inputs = 0V                                            | —                            | 5   | —               | —                        | 5   | —               | mV <sub>pp</sub> |
| REFERENCE INPUT                                    |                   |                                                                                                                                               |                              |     |                 |                          |     |                 |                  |
| Input Resistance<br>(Pin 19 to GND)                | R <sub>REF</sub>  | T <sub>A</sub> = Full Temp. Range<br>Input Resistance                                                                                         | 7                            | 11  | 15              | 7                        | 11  | 15              | kΩ               |
| ANALOG OUTPUTS                                     |                   |                                                                                                                                               |                              |     |                 |                          |     |                 |                  |
| Output Capacitance<br>(Note 4)<br>C <sub>OUT</sub> | C <sub>OUT</sub>  | T <sub>A</sub> = Full Temp. Range<br>DB0-DB11 = 0V, WR = CS = 0V<br>DB0-DB11 = V <sub>DD</sub> , WR = CS = 0V                                 | —                            | —   | 60<br>120       | —                        | —   | 60<br>120       | pF               |
| DIGITAL INPUTS                                     |                   |                                                                                                                                               |                              |     |                 |                          |     |                 |                  |
| Input High Voltage                                 | V <sub>IHH</sub>  | T <sub>A</sub> = Full Temp. Range, PM-7545                                                                                                    | 13.5                         | —   | —               | 13.5                     | —   | —               | V                |
| Input Low Voltage                                  | V <sub>ILL</sub>  |                                                                                                                                               | —                            | —   | 1.5             | —                        | —   | 1.5             | V                |
| Input High Voltage                                 | V <sub>IHH</sub>  | T <sub>A</sub> = Full Temp. Range, PM-7645                                                                                                    | 2.4                          | —   | —               | 2.4                      | —   | —               | V                |
| Input Low Voltage                                  | V <sub>ILL</sub>  |                                                                                                                                               | —                            | —   | 0.8             | —                        | —   | 0.8             | V                |
| Input Current                                      | I <sub>IN</sub>   | T <sub>A</sub> = +25°C<br>T <sub>A</sub> = Full Temp. Range                                                                                   | —                            | —   | 1<br>10         | —                        | —   | 1<br>10         | μA               |
| Input Capacitance<br>DB0—DB11, WR, CS              | C <sub>IN</sub>   | T <sub>A</sub> = Full Temp. Range<br>V <sub>IN</sub> = 0 (Note 4)                                                                             | —                            | —   | 8               | —                        | —   | 8               | pF               |

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**ELECTRICAL CHARACTERISTICS** at  $V_{DD} = +15V$ ,  $V_{REF} = +10V$ ,  $V_{OUT} = 0V$ ,  $AGND = DGND = 0V$ ;  $T_A = -55^\circ C$  to  $+125^\circ C$  apply for PM-7545/PM-7645AR/BR;  $T_A = -40^\circ C$  to  $+85^\circ C$  apply for PM-7545/PM-7645ER/FR/FP/FPC/FS;  $T_A = 0^\circ C$  to  $+70^\circ C$  apply for PM-7545/PM-7645GP, unless otherwise noted. *Continued*

| PARAMETER                                    | SYMBOL   | CONDITIONS                                                                        | PM-7545A/E/G<br>PM-7645A/E/G |            |            | PM-7545B/F<br>PM-7645B/F |            |            | UNITS |
|----------------------------------------------|----------|-----------------------------------------------------------------------------------|------------------------------|------------|------------|--------------------------|------------|------------|-------|
|                                              |          |                                                                                   | MIN                          | TYP        | MAX        | MIN                      | TYP        | MAX        |       |
| POWER SUPPLY                                 |          |                                                                                   |                              |            |            |                          |            |            |       |
| Supply Current                               | $I_{DD}$ | $T_A$ = Full Temp. Range<br>(All Digital Inputs $V_{INL}$ or $V_{INH}$ )          | —                            | —          | 2          | —                        | —          | 2          | mA    |
|                                              | $I_{DD}$ | $T_A$ = +25°C<br>$T_A$ = Full Temp. Range<br>(All Digital Inputs 0V or $V_{DD}$ ) | —                            | 2<br>5     | 100<br>100 | —                        | 2<br>5     | 100<br>100 | μA    |
| SWITCHING CHARACTERISTICS<br>(Notes 4, 5, 9) |          | See Timing Diagram                                                                | PM-7545 A/E/G                |            |            | PM-7545 B/F/H            |            |            |       |
| Chip Select to<br>Write Setup Time           | $t_{CS}$ | $T_A$ = +25°C<br>$T_A$ = Full Temp. Range                                         | 180<br>200                   | 120<br>150 | —          | 180<br>200               | 120<br>150 | —          | ns    |
| Chip Select to<br>Write Hold Time            | $t_{CH}$ | $T_A$ = Full Temp. Range                                                          | 0                            | —          | —          | 0                        | —          | —          | ns    |
| Write Pulse<br>Width                         | $t_{WH}$ | $T_A$ = +25°C<br>$T_A$ = Full Temp. Range                                         | 160<br>240                   | 100<br>170 | —          | 160<br>240               | 100<br>170 | —          | ns    |
| Data Setup<br>Time                           | $t_{DS}$ | $T_A$ = +25°C<br>$T_A$ = Full Temp. Range                                         | 90<br>120                    | 60<br>80   | —          | 90<br>120                | 60<br>80   | —          | ns    |
| Data Hold Time                               | $t_{DH}$ | $T_A$ = Full Temp. Range                                                          | 10                           | —          | —          | 10                       | —          | —          | ns    |
| SWITCHING CHARACTERISTICS<br>(Notes 4, 5, 9) |          | See Timing Diagram                                                                | PM-7545 A/E/G                |            |            | PM-7545 B/F/H            |            |            |       |
| Chip Select to<br>Write Setup Time           | $t_{CS}$ | $T_A$ = +25°C<br>$T_A$ = Full Temp. Range                                         | 190<br>210                   | —          | —          | 190<br>210               | —          | —          | ns    |
| Chip Select to<br>Write Hold Time            | $t_{CH}$ | $T_A$ = Full Temp. Range                                                          | 0                            | —          | —          | 0                        | —          | —          | ns    |
| Write Pulse<br>Width                         | $t_{WH}$ | $T_A$ = +25°C<br>$T_A$ = Full Temp. Range                                         | 160<br>210                   | —          | —          | 160<br>210               | —          | —          | ns    |
| Data Setup<br>Time                           | $t_{DS}$ | $T_A$ = +25°C<br>$T_A$ = Full Temp. Range                                         | 225<br>300                   | —          | —          | 225<br>300               | —          | —          | ns    |
| Data Hold Time                               | $t_{DH}$ | $T_A$ = Full Temp. Range                                                          | 10                           | —          | —          | 10                       | —          | —          | ns    |

**NOTES:**

- 12-bit monotonic over full temperature range.
- Includes the effects of 5ppm max. gain T.C.
- Using internal  $R_{FB}$  DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
- GUARANTEED and NOT TESTED.
- From digital input change to 90% of final analog output.
- All digital inputs  $= 0V$  to  $V_{DD}$  or  $V_{DD}$  to  $0V$ .
- Logic inputs are MOS gates, typical input current (at  $+25^\circ C$ ) is less than  $1nA$ .
- Sample tested at  $+25^\circ C$  to ensure compliance.
- Chip select  $\overline{CS}$  must be coincident or present before and/or after write  $\overline{WR}$ ; that is,  $t_{CS} \geq t_{WH}$ ,  $t_{CH} \geq 0$ .

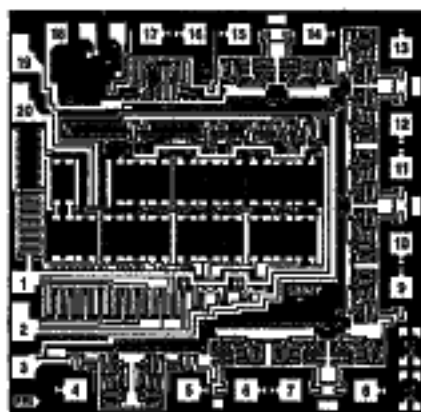
2



## PM-7545/PM-7645

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## DICE CHARACTERISTICS



DIE SIZE 0.102 × 0.100 inch, 10,200 sq. mils  
(2.59 × 2.54mm, 6.58 sq. mm)

- |               |                      |
|---------------|----------------------|
| 1. OUT        | 11. DB4              |
| 2. AGND       | 12. DB3              |
| 3. DGND       | 13. DB2              |
| 4. DB11 (MSB) | 14. DB1              |
| 5. DB10       | 15. DB0 (LSB)        |
| 6. DB9        | 16. CS               |
| 7. DB8        | 17. WR               |
| 8. DB7        | 18. V <sub>DD</sub>  |
| 9. DB6        | 19. V <sub>REF</sub> |
| 10. DB5       | 20. R <sub>FB</sub>  |

WAFER TEST LIMITS at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = +5$  or  $+15\text{V}$ ,  $V_{REF} = +10\text{V}$ ,  $V_{OUT} = 0\text{V}$ , AGND = DGND = 0V.

| PM-7545G/PM-7645G                                         |           |                                                                                |             |                               |  |
|-----------------------------------------------------------|-----------|--------------------------------------------------------------------------------|-------------|-------------------------------|--|
| PARAMETER                                                 | SYMBOL    | CONDITIONS                                                                     | LIMIT       | UNITS                         |  |
| Relative Accuracy                                         | INL       | Endpoint Linearity Error                                                       | $\pm 1/2$   | LSB MAX                       |  |
| Differential Nonlinearity                                 | DNL       |                                                                                | $\pm 1/2$   | LSB MAX                       |  |
| Gain Error                                                | $G_{FSZ}$ | DAC Latches Loaded with 1111 1111 1111                                         | $\pm 5$     | LSB MAX                       |  |
| Output Leakage                                            | $I_{LKG}$ | DAC Latches Loaded with 0000 0000 0000<br>Pad 1                                | $\pm 10$    | nA MAX                        |  |
| Input Resistance                                          | $R_{REF}$ | Pad 19                                                                         | 2/15        | k $\Omega$ MIN/k $\Omega$ MAX |  |
| Digital Input High                                        | $V_{IH1}$ | $V_{DD} = 5\text{V}$<br>$V_{DD} = 15\text{V}$ PM-7545 only                     | 2.4<br>13.5 | V MIN                         |  |
| Digital Input Low                                         | $V_{IL1}$ | $V_{DD} = 5\text{V}$<br>$V_{DD} = 15\text{V}$ PM-7545 only                     | 0.8<br>1.5  | V MAX                         |  |
| Digital Input High                                        | $V_{IH2}$ | $V_{DD} = 15\text{V}$ PM-7645 only                                             | 2.4         | V MIN                         |  |
| Digital Input Low                                         | $V_{IL2}$ | $V_{DD} = 15\text{V}$ PM-7645 only                                             | 0.8         | V MAX                         |  |
| Input Current                                             | $I_{IN}$  | $V_{IN} = 0\text{V}$ or $V_{DD}$                                               | $\pm 1$     | $\mu\text{A}$ MAX             |  |
| Supply Current                                            | $I_{DD}$  | All Digital Inputs $V_{IN1}$ or $V_{REF}$<br>All Digital Inputs 0V or $V_{DD}$ | 2<br>0.1    | mA MAX                        |  |
| DC Supply Rejection<br>( $\Delta G_{FSZ}/\Delta V_{DD}$ ) | PSS       | $\Delta V_{DD} = \pm 5\%$                                                      | 0.002       | %/% MAX                       |  |

## NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

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PM-7545/PM-7645

**TYPICAL ELECTRICAL CHARACTERISTICS** at  $V_{DD} = +5V$  or  $+15V$ ,  $AGND = DGND = 0V$ ,  $V_{REF} = +10V$ ,  $OUT = 0V$ ;  $T_A = 25^\circ C$ , unless otherwise noted. (Note 1)

| PARAMETER                            | SYMBOL    | CONDITIONS                             | PM-7545G/PM-7645G | UNITS |
|--------------------------------------|-----------|----------------------------------------|-------------------|-------|
|                                      |           |                                        | TYPICAL           |       |
| Digital Input Capacitance            | $C_{DI}$  |                                        | 7                 | pF    |
| Output Capacitance                   | $C_{OUT}$ | DAC Latches Loaded with 0000 0000 0000 | 60                | pF    |
|                                      |           | DAC Latches Loaded with 1111 1111 1111 | 110               |       |
| Propagation Delay<br>(Notes 2, 3, 4) | $t_{PD}$  | $V_{DD} = 15V$                         | 140               | ns    |
|                                      |           | $V_{DD} = 5V$ PM-7545 only             | 230               |       |

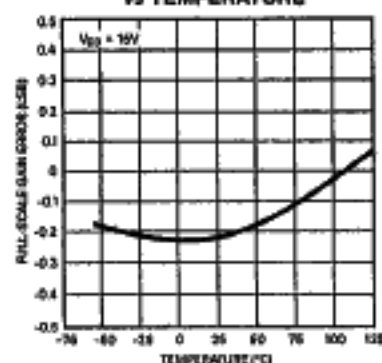
**NOTES:**

- These characteristics are for design guidance only and are not subject to test.
- From digital input change to 90% of final analog output.
- OUT load =  $100\Omega$ ,  $C_{EXT} = 12pF$ .
- $\overline{CS} = \overline{WR} = 0$ , DS0 to DS11 =  $0V$  to  $V_{DD}$  or  $V_{DD}$  to  $0V$ .

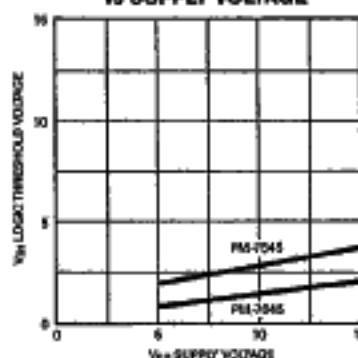
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**TYPICAL PERFORMANCE CHARACTERISTICS**

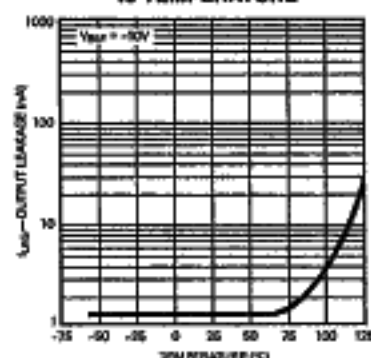
**FULL-SCALE GAIN ERROR  
vs TEMPERATURE**



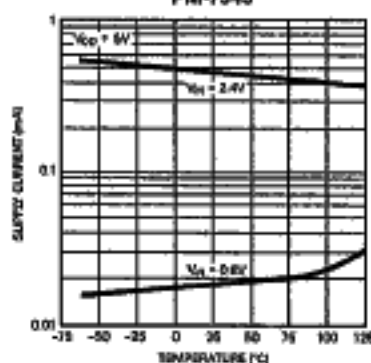
**LOGIC THRESHOLD VOLTAGE  
vs SUPPLY VOLTAGE**



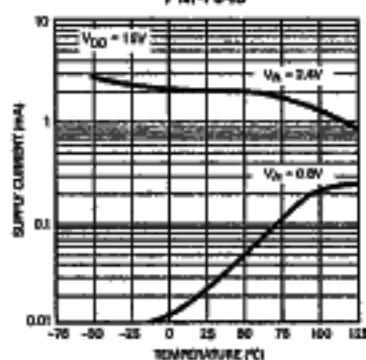
**OUTPUT LEAKAGE CURRENT  
vs TEMPERATURE**



**SUPPLY CURRENT  
vs TEMPERATURE  
PM-7545**



**SUPPLY CURRENT  
vs TEMPERATURE  
PM-7645**





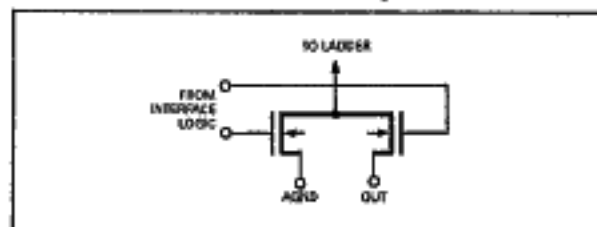


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PM-7545/PM-7645

The internal feedback resistor ( $R_{FB}$ ) has a normally closed switch in series as shown in Figure 1. This switch improves performance over temperature and power supply rejection; however when the circuit is not powered up the switch assumes an open state.

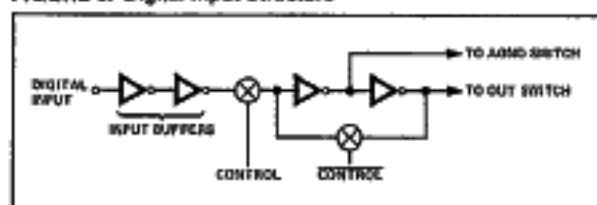
FIGURE 2: N-Channel Current Steering Switch



## DIGITAL SECTION

Figure 3 shows the digital structure for one bit. The digital signals CONTROL and CONTROL are generated from CS and WR.

FIGURE 3: Digital Input Structure



The input buffers are simple CMOS inverters designed such that when the PM-7545 is operated with  $V_{DD} = 5V$ , the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When the digital input is in the region of 1.0 volts to 6.0 volts, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents, it is recommended that the digital input voltages be as close to the supply rails ( $V_{DD}$  and  $DGND$ ) as is practically possible. The PM-7545 may be operated with any supply voltage in the range  $5 \leq V_{DD} \leq 15$  volts. With  $V_{DD} = +15V$ , the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V. The PM-7545 operates with  $V_{DD} = 15V$  only; the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels.

## BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the PM-7545/PM-7645. Resistor  $R1$  is used to trim for full scale. The following versions (PM-7545AR, PM-7545ER, PM-7545GP) have a guaranteed maximum gain error of  $\pm 1$  LSB at  $+25^\circ C$  and  $V_{DD} = +5V$ , and in many applications the gain trim resistors are

not required. Capacitor  $C1$  provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. The circuits of Figures 4 and 5 have constant input impedance at the  $V_{REF}$  terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range  $0$  to  $-V_{IN}$  (the inversion is introduced by the op amp); or  $V_{IN}$  can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier).  $V_{IN}$  can be any voltage in the range  $-20 \leq V_{IN} \leq +20$  volts (provided the op amp can handle such voltages) since  $V_{REF}$  is permitted to exceed  $V_{DD}$ . Table 2 shows the code relationship for the circuit of Figure 4.

2

FIGURE 4: Unipolar Binary Operation

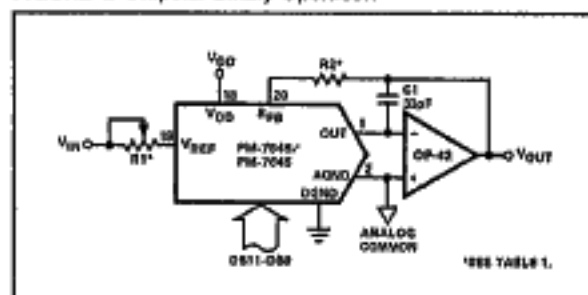


TABLE 1: Recommended Trim Resistor Value vs. Grades

| TRIM RESISTOR | CR   | HP/FR/BR | GP/ER/AR |
|---------------|------|----------|----------|
| R1            | 200Ω | 100Ω     | 20Ω      |
| R2            | 68Ω  | 33Ω      | 6.8Ω     |

TABLE 2: Unipolar Binary Code Table for Circuit of Figure 4

| BINARY NUMBER IN DAC REGISTER |      |      | ANALOG OUTPUT                                                    |  |
|-------------------------------|------|------|------------------------------------------------------------------|--|
| 1111                          | 1111 | 1111 | $-V_{IN} \cdot \left\{ \frac{4095}{4096} \right\}$               |  |
| 1000                          | 0000 | 0000 | $-V_{IN} \cdot \left\{ \frac{2048}{4096} \right\} = -1/2 V_{IN}$ |  |
| 0000                          | 0000 | 0001 | $-V_{IN} \cdot \left\{ \frac{1}{4096} \right\}$                  |  |
| 0000                          | 0000 | 0000 | 0 Volts                                                          |  |

Figure 5 and Table 3 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code. The inverter  $U_1$  on the MSB line, converts 2's-complement input code to offset binary code. The inverter  $U_1$  may be omitted if the inversion is done in software.

$R_3$ ,  $R_4$  and  $R_5$  must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of  $R_3$  value to  $R_4$  causes both offset and full scale error. Mismatch of  $R_5$  to  $R_4$  and  $R_3$  causes full scale error.

TABLE III: 2's Complement Code Table for Circuit of Figure 5

| DATA INPUT |      |      | ANALOG OUTPUT                                      |
|------------|------|------|----------------------------------------------------|
| 0111       | 1111 | 1111 | $+V_{IN} \cdot \left\{ \frac{2047}{2048} \right\}$ |
| 0000       | 0000 | 0001 | $+V_{IN} \cdot \left\{ \frac{1}{2048} \right\}$    |
| 0000       | 0000 | 0000 | 0 Volts                                            |
| 1111       | 1111 | 1111 | $-V_{IN} \cdot \left\{ \frac{1}{2048} \right\}$    |
| 1000       | 0000 | 0000 | $-V_{IN} \cdot \left\{ \frac{2048}{2048} \right\}$ |

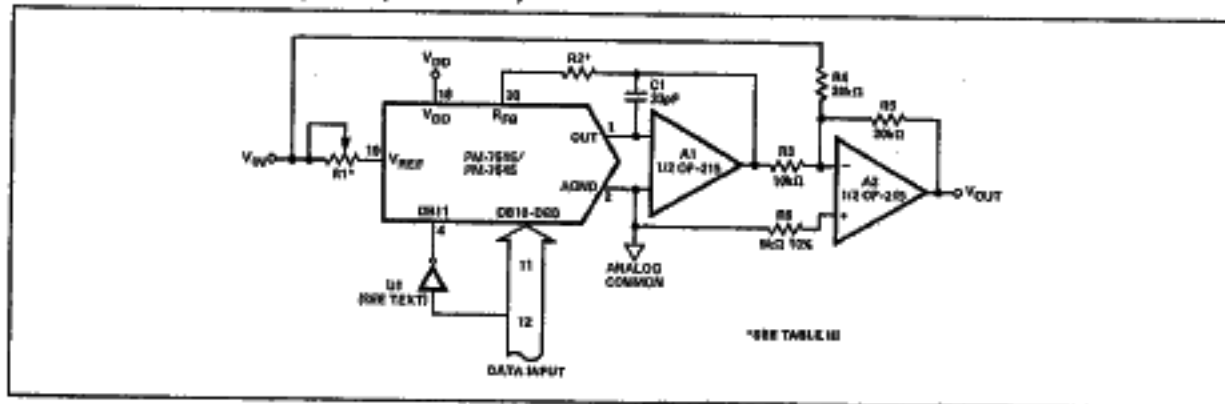
# APPLICATION HINTS

**Output Offset:** CMOS D/A converters exhibit a code-dependent output resistance that causes a code-dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is  $0.67 V_{OS}$  where  $V_{OS}$  is the amplifier input-offset voltage. To maintain monotonic operation, it is recommended that  $V_{OS}$  be no greater than 10% of 1 LSB over the temperature range of operation.

**General Ground Management:** AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the PM-7545/PM-7645. It is recommended that two diodes (1N914 or equivalent) be connected in inverse parallel between AGND and DGND pins in complex systems where AGND and DGND tie on the backplane.

**Digital Glitches:** When  $\overline{WR}$  and  $\overline{CS}$  are both low, the latches are transparent and the D/A converter inputs follow the data inputs. Some bus systems do not always have data valid for the whole period during which  $\overline{WR}$  is low. This will allow invalid data to briefly appear at the DAC inputs during the write cycle. This can cause unwanted glitches at the DAC output. Retiming the write pulse  $\overline{WR}$ , so that it only occurs when data is valid, will eliminate the problem.

FIGURE 5: Bipolar Operation (2's Complement Code)



## PM-7545/PM-7645

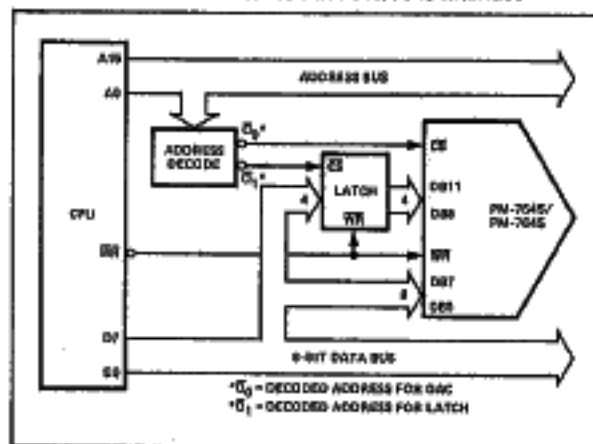
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## INTERFACING THE PM-7545/PM-7645 TO MICROPROCESSORS

The PM-7545 can be directly interfaced to either an 8 or 16-bit microprocessor via its 12-bit wide data latch using the  $\overline{CS}$  and  $\overline{WR}$  control signals.

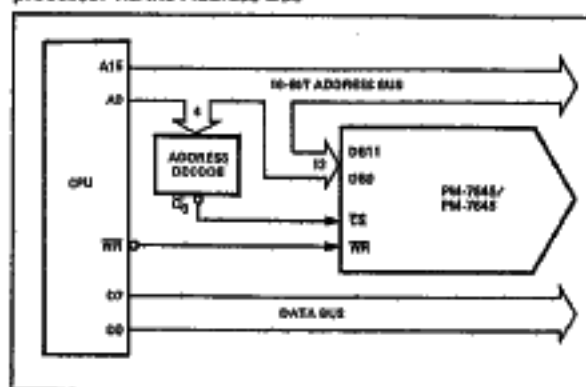
An 8-bit processor interface configuration is shown in Figure 6. It uses two memory addresses, one for the lower 8-bits and one for the upper 4-bits of data into the DAC via the latch.

FIGURE 6: 8-Bit Processor to PM-7545/7645 interface



Connection to an 8-bit processor with a full 16-bit wide address bus (such as the 6800, 8080, Z80) is shown in Figure 7. The 12 lower address lines are fed directly to the PM-7545; this allows the PM-7545 to use 4k bytes for its address location. The address field of the instruction is organized so that the lower 12-bits contain the DAC data. Data is written into the DAC using a single write instruction.

FIGURE 7: Connecting the PM-7545/7645 to an 8-Bit Microprocessor via the Address Bus



2