

DS21354DK E1 Single-Chip Transceiver Design Kit Daughter Card

www.maxim-ic.com

GENERAL DESCRIPTION

The DS21354 design kit is an easy-to-use evaluation board for the DS21354 E1 single-chip transceiver (SCT). The DS21354DK is intended to be used as a daughter card with either the DK2000 or the DK101 motherboards. The DS21354DK comes complete with a DS21354 SCT, transformers, termination resistors, configuration switches, line-protection circuitry, network connectors, and motherboard connectors. The DK101/DK2000 motherboard and Dallas' ChipView software give point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status, as well as multiple clock and signal routing configurations.

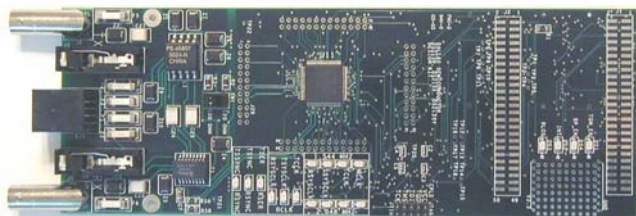
Each DS21354DK is shipped with a free DK101 motherboard. For complex applications, the DK2000 high-performance demo kit motherboard can be purchased separately.

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DESIGN KIT CONTENTS

DS21354DK Design Kit Daughter Card
DK101 Low-Cost Motherboard
CD ROM

ChipView Software
DS21354DK Data Sheet
DK101 Data Sheet
DS21354 Data Sheet
DS21354 Errata Sheet



FEATURES

- Demonstrates Key Functions of the DS21354 E1 SCT Transceiver
- Includes DS21354 SCT, Transformers, Bantam, BNC and RJ48 Network Connectors, and Termination Passives
- BNC Connections for 75Ω E1
- Bantam and RJ48 Connectors for 120Ω E1
- Multitap Transformer to Facilitate True Impedance Matching for 75Ω and 120Ω/100Ω Paths
- Compatible with DK101 and DK2000 Demo Kit Motherboards
- DK101/DK2000 and ChipView Software Provide Point-and-Click Access to the DS21354 Register Set
- Software-Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- LEDs for Loss-Of-Signal and Interrupt Status as well as Indications for Multiple Clock and Signal Routing Configurations
- Easy-to-Read Silk Screen Labels Identify the Signals Associated with all Connectors, Jumper, and LEDs
- Network Interface Protection for Overvoltage and Overcurrent Events Area Available for Further Customization

ORDERING INFORMATION

PART	DESCRIPTION
DS21354DK	DS21354 Design Kit Daughter Card (with include DK101 motherboard)

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COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1–C5, C8–C12, C15–C19, C21, C22, C29–C34	23	0.1μF 10%, 16V ceramic capacitors (0603)	Digi-Key	311-1088-1-ND
C7, C36	2	1μF 10%, 16V ceramic capacitors (1206)	Digi-Key	PCC1882CT-ND
C13, C14	2	0.1μF 10%, 16V ceramic capacitors (0805)	Digi-Key	311-1142-1-ND
C23	1	0.1μF 10%, 25V ceramic capacitor (1206)	Digi-Key	PCC1883CT-ND
C24–C27	4	0.22μF, 50V ceramic capacitors	Digi-Key	UNK
C35	1	10μF 20%, 16V tantalum capacitor (B case)	Digi-Key	PCS3106CT-ND
DS1, DS4–DS18	16	LED, green, SMD	Digi-Key	P501CT-ND
DS2, DS3	2	LED, red, SMD	Digi-Key	P500CT-ND
F1–F6	6	250V, 1.25A fuse, SMT	Teccor Electronics	F1250T
J1, J2	2	Male 0.1, SMD, 50-pin, dual-row vertical	Samtec	TSM-125-01-T-DV
J3, J4	2	Bantam connectors	SWK	RTT34B02
J5, J6	2	Connector BNC RA 5-pin	Kruvand	UCBJR220
J7–J9	3	Socket, SMD, 50-pin, dual-row vertical	Samtec	TFM-125-02-S-D-LC
JT10	1	Connector, 10-pin, dual-row vertical	Digi-Key	S2012-05-ND
L1	1	Choke, dual 4-line 24μH, 8-pin SO	Pulse Engineering	PE-65857
R1, R14, R21	3	51.1Ω 1%, 1/8W resistors (1206)	Digi-Key	P51.1FCT-ND
R2, R3, R58, R59	4	0Ω 5%, 1/8W resistors (1206)	Digi-Key	P0.0ETR-ND
R4, R5, R60	3	51.1Ω 1%, 1/10W resistors (0805)	Digi-Key	P51.1CCT-ND
R6, R9, R10, R13, R15–R19, R22, R23, R25–R29, R32, R37, R38, R44, R47–R49, R61	24	10kΩ 1%, 1/10W resistors (0805)	Digi-Key	P10.0KCCT-ND
R7, R8, R11, R12, R30, R31, R35, R36, R39–R43, R45, R50–R53	18	330Ω 0.1%, 1/10W MF resistors (0805)	Digi-Key	P330ZCT-ND
R24	1	1.0kΩ 1%, 1/10W resistor (0805)	Digi-Key	P1.00KCCT-ND
R33, R34	2	Not populate	—	Not populated
R46	1	4.7kΩ 1%, 1/8W resistor (0805)	Digi-Key	9C08052A4701FK HFT
R54, R55	2	61.9Ω 1%, 1/8W resistors (1206)	Digi-Key	P61.9FCT-ND
R56, R57	2	49.9Ω 1%, 1/8W resistors (1206)	Digi-Key	P49.9FCT-ND
RJ1	1	RJ48 connector	Molex	43223
SW1	1	Switch DPDT slide 6-pin TH	Avnet	SSA22
T1	1	XFMR 16-pin SMT	Pulse Engineering	TX1099
U1–U4, U6	5	BBUS switch 10-bit CMOS, 150-mil, 24-pin SO	IDT	IDTQS3R861Q
U5	1	144-pin macrocell CPLD	Avnet	XC95144XL-10TQ100C
U7–U10	4	Quad bus switch, 150-mil, 16-pin SO	IDT	IDTQS3125Q
U11	1	T1/E1/J1 XCVR 100-pin QFP, 0°C to +70°C	Dallas Semiconductor	DS2156L
Z1, Z6–Z8	4	160V, 500A Sidactor	Teccor Electronics	P1800SCMC
Z2, Z3	2	58V, 500A Sidactor	Teccor Electronics	P0640SCMC
Z4, Z5	2	6V, 50A Sidactor	Teccor Electronics	P0080SAMC
Z9, Z10	2	25V, 500A Sidactor	Teccor Electronics	P0300SCMC

BASIC OPERATION

This design kit relies upon several supporting files, which can be downloaded from our website at www.maxim-ic.com/DS21354DK. See the DS21354DK QuickView data sheet for these files.

Hardware Configuration

Using the DK101 processor board:

- Connect the daughter card to the DK101 processor board.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V. (The external 5V connector and the TIM 5V supply headers are unused.)
- All processor board DIP switch settings should be in the ON position with exception for the flash programming switch, which should be OFF.
- From the Programs menu, launch the host application named ChipView.EXE. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

Using the DK2000 processor board:

- Connect the daughter card to the DK2000 processor board.
- Connect J1 to the power supply that is delivered with the kit. Alternately, a PC power supply can be connected to connector J2.
- From the Programs menu, launch the host application named ChipView.EXE. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

General:

- Upon power-up the RLOS LED is lit, as well as the MCLK-2.048MHz and TCLK-2.048MHz LEDs.
- Due to the dual winding transformer, only the 120Ω line build-out configuration setting is needed to cover 75Ω E1 and 120Ω E1.

Quick Setup (Demo Mode)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Demo Mode.
- The program requests a configuration file, then select DS21354_E1_DSNCOM_DRV.R.cfg.
- The Demo Mode screen appears. Upon external loopback, the LOS and OOF indicators extinguish.

Quick Setup (Register View)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Register View.
- The program requests a definition file, then select DS21354.def.
- The Register View screen appears, showing the register names, acronyms, and values. Note: During the definition file load process, all registers are initialized according to the init value filed in the definition file (because the SETUP field in the .def file is turned on).
- Predefined register settings for several functions are available as initialization files.
 - INI files are loaded by selecting the menu **F**ile→**R**eg Ini File→**L**oad Ini File.
 - Load the INI file DS21354e1_fas_crc4_cas.ini.
 - After loading the INI file the following may be observed:
 - The RLOS LED extinguishes upon external loopback.
 - The device is now configured for E1 FAS with CRC4 and CAS.

Miscellaneous:

- Clock frequencies and certain pin bias levels are provided by a register-mapped CPLD, which is on the DS21354 daughter card.
- The definition file for this CPLD is named DS215x_35x_CPLD_V2.def. See the [CPLD Register Map](#) section for definitions.
- All files referenced above are available for download in the section marked "File Locations."

REGISTER MAP

The DK101 daughter card address space begins at 0x81000000.

The DK2000 daughter card address space begins at:

0x30000000 for slot 0

0x40000000 for slot 1

0x50000000 for slot 2

0x60000000 for slot 3

All offsets given in [Table 1](#) are relative to the beginning of the daughter card address space.

Table 1. Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0015	CPLD	Board identification and clock/signal routing
0X1000 to 0X10ff	Single-Chip Transceiver	Board is populated with one of the following: DS2155, DS2156, DS21352, or DS21354. Please see the data sheet(s) for details.

Registers in the CPLD can be easily modified using ChipView.exe, a host-based user-interface software, along with the definition file named *DS215x_35x_CPLD_V2.def*. Definition files for the SCT are named *DS2155.def*, *DS21352.def*, or *DS21354.def*, depending on the board population option.

CPLD Register Map

Table 2. CPLD Register Map

OFFSET	NAME	TYPE	DESCRIPTION
0X0000	BID	Read-Only	Board ID
0X0002	XBIDH	Read-Only	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0011	SWITCH1	Read-Write	Pin to 1.544MHz
0X0012	SWITCH2	Read-Write	Pin to 2.048MHz
0X0013	SWITCH3	Read-Write	Pin-to-Pin Connect
0X0014	SWITCH4	Read-Write	Pin-to-Pin Connect
0X0015	LEVELS	Read-Write	Set Level on Pin 1 = 3.3V

ID Registers

OFFSET	NAME	TYPE	VALUE	DESCRIPTION
0X0000	BID	Read-Only	0xD	Board ID
0X0002	XBIDH	Read-Only	0x0	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	0x0	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	0x5	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Displays current FAB revision	Board FAB Revision
0X0006	AREV	Read-Only	Displays current assembly revision	Board Assembly Revision
0X0007	PREV	Read-Only	Displays current PLD firmware	PLD Revision

			revision	
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Control Registers

The control registers are used primarily to control several banks of FET switches that route clocks and backplane signals. Please note that certain register settings cause line contention, e.g., setting SWITCH1.4 and SWITCH2.4 both to 0 would drive MCLK with both 1.544MHz and 2.048MHz.

SWITCH1: PIN TO 1.544MHz (OFFSET = 0x0011) INITIAL VALUE = 0xF

(MSB)							(LSB)
—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK

NAME	POSITION	FUNCTION
MCLK	SWITCH1.3	0 = Connect MCLK to the 1.544MHz clock 1 = Open Switch 1.4
TCLK	SWITCH1.2	0 = Connect TCLK to the 1.544MHz clock 1 = Open Switch 1.3
RSYSCLK	SWITCH1.1	0 = Connect RSYSCLK to the 1.544MHz clock 1 = Open Switch 1.2
TSYSCLK	SWITCH1.0	0 = Connect TSYSCLK to the 1.544MHz clock 1 = Open Switch 1.1

SWITCH2: PIN TO 2.048MHz (Offset = 0X0012) INITIAL VALUE = 0x3

(MSB)							(LSB)
—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK

NAME	POSITION	FUNCTION
MCLK	SWITCH2.3	0 = Connect MCLK to the 2.048MHz clock 1 = Open Switch 2.4
TCLK	SWITCH2.2	0 = Connect TCLK to the 2.048MHz clock 1 = Open Switch 2.3
RSYSCLK	SWITCH2.1	0 = Connect RSYSCLK to the 2.048MHz clock 1 = Open Switch 2.2
TSYSCLK	SWITCH2.0	0 = Connect TSYSCLK to the 2.048MHz clock 1 = Open Switch 2.1

SWITCH3: PIN-TO-PIN CONNECT (Offset = 0X0013) INITIAL VALUE = 0xF

(MSB)							(LSB)
—	—	—	—	TSS_RS	TCL_RC	RSY_RC	TSY_RC

NAME	POSITION	FUNCTION
TSS_RS	SWITCH3.3	0 = Connect TSSYNC to RSYNC 1 = Open Switch 3.4
TCL_RC	SWITCH3.2	0 = Connect TCLK to RCLK 1 = Open Switch 3.3
RSY_RC	SWITCH3.1	0 = Connect RSYSCLK to RCLK 1 = Open Switch 3.2
TSY_RC	SWITCH3.0	0 = Connect TSYSCLK to RCLK 1 = Open Switch 3.1

SWITCH4: PIN-TO-PIN CONNECT (Offset = 0X0014) INITIAL VALUE = 0x3**(MSB)****(LSB)**

—	—	—	—	URCLK_2048	UTCLK_2048	RSER_TSER	RSYNC_TSYNC
---	---	---	---	------------	------------	-----------	-------------

NAME	POSITION	FUNCTION		
URCLK_2048	SWITCH4.3	0 = Connect UR_CLK (TSSYNC) to 2.048MHz 1 = Open Switch 4.4		
UTCLK_2048	SWITCH4.2	0 = Connect UT_CLK (TCHCLK) to 2.048MHz 1 = Open Switch 4.3		
RSER_TSER	SWITCH4.1	0 = Connect RER to TSER 1 = Open Switch 4.2		
RSYNC_TSYNC	SWITCH4.0	0 = Connect RSYNC to TSYNC 1 = Open Switch 4.1		

LEVELS: SET LEVEL ON PIN (Offset = 0X0015) INITIAL VALUE = 0x6**(MSB)****(LSB)**

—	—	—	—	—	BP_EN	PPCTDM_EN	TUSEL
---	---	---	---	---	-------	-----------	-------

NAME	POSITION	FUNCTION
—	LEVELS1.3	—
BP_EN	LEVELS1.2	0 = Enable IDT switches that connect the UTOPIA bus to daughter card header
PPCTDM_EN	LEVELS1.1	0 = Enable IDT switches that connect the TDM bus to the daughter card header
TUSEL	LEVELS1.0	0 = Set DS2156.TUSEL to enable TDM backplane 1 = Set DS2156.TUSEL to enable UTOPIA backplane

Note (DS2156 only): When the UTOPIA backplane is enabled (LEVELS.TUSEL = 1) there is a possibility for contention between the UTOPIA bus master and TSYCLK, TSER, and RSER. To avoid this, the following switches should be opened when the UTOPIA backplane is enabled: SWITCH1.0, SWITCH2.0, SWITCH3.0, and SWITCH4.1

DS21354 INFORMATION

For more information about the DS21354, please consult the DS21354 data sheet available on our website at www.maxim-ic.com/DS21354. Software downloads are also available for this design kit.

DS21354DK INFORMATION

For more information about the DS21354DK, including software downloads, please consult the DS21354DK data sheet available on our website at www.maxim-ic.com/DS21354DK.

TECHNICAL SUPPORT

For additional technical support, please e-mail your questions to telecom.support@dalsemi.com.

SCHEMATICS

The DS21354DK schematics are featured in the following 13 pages.

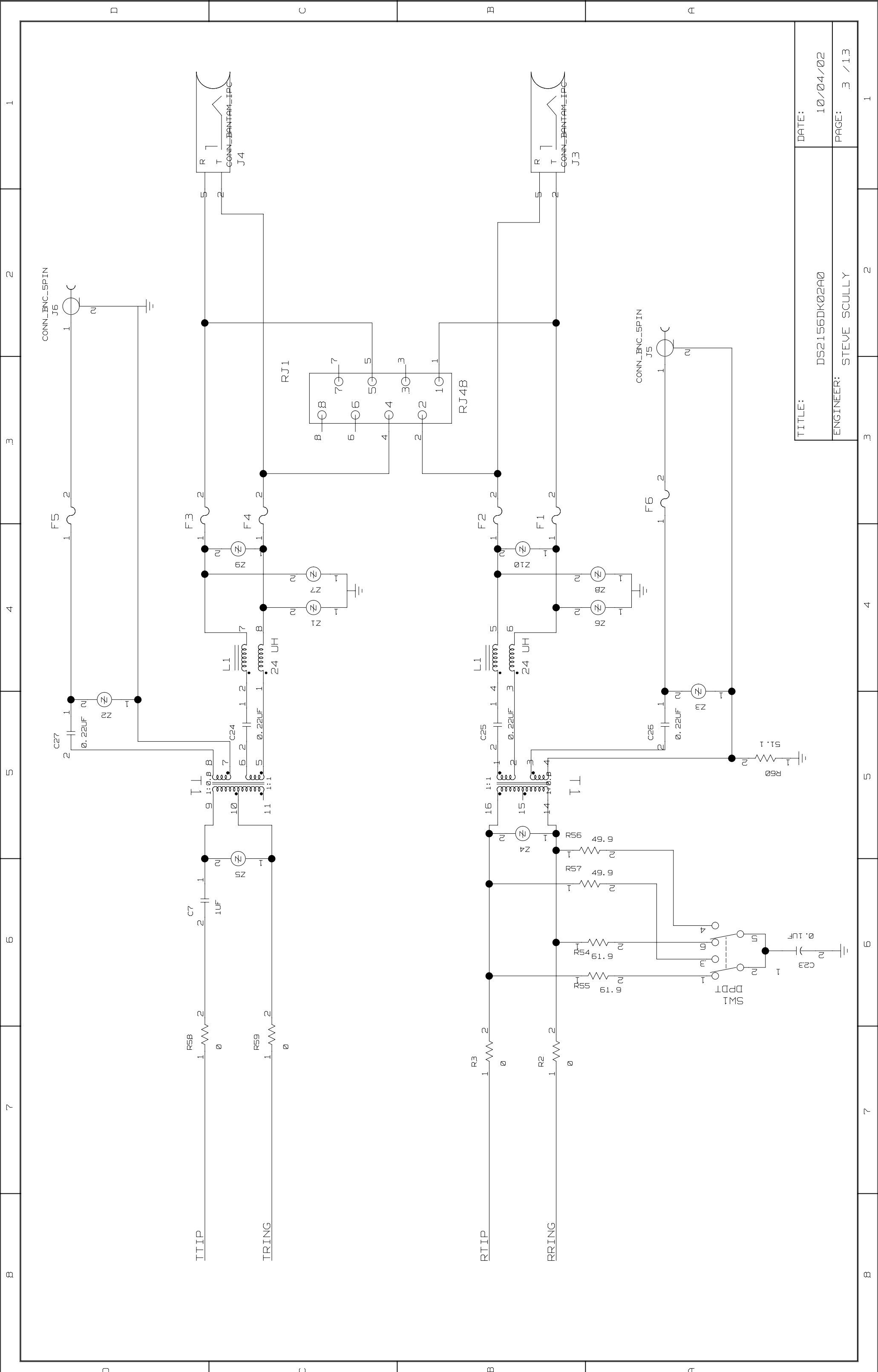
DOCUMENT REVISION HISTORY

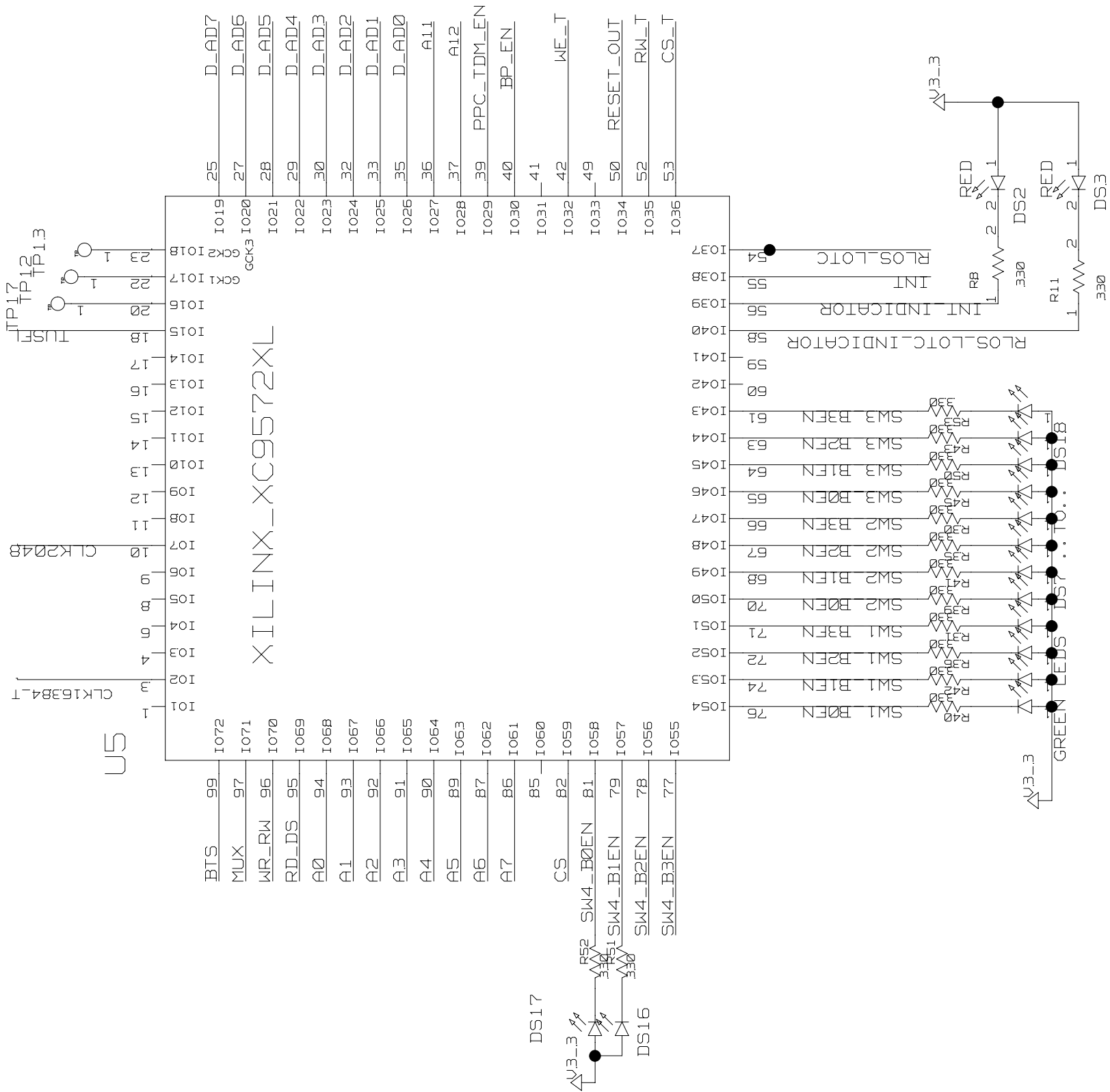
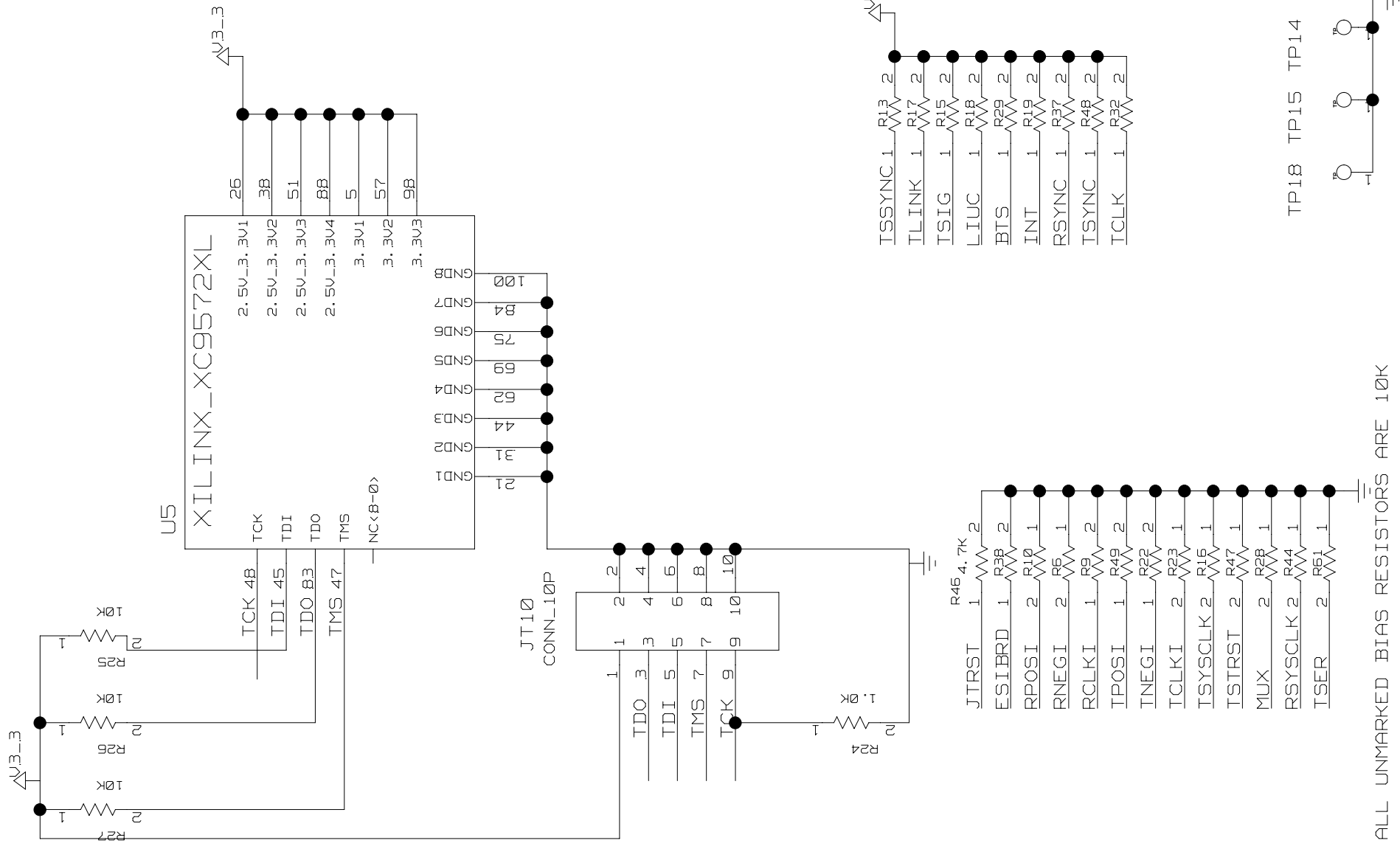
REVISION DATE	DESCRIPTION
060303	Initial DS21354DK data sheet release.
011904	Updated the <i>General Description</i> and <i>Features</i> sections; added the <i>Demo Kit Contents</i> section.
012705	Updated schematics (removed component values for Fuse and Sidactor; see <i>Component List</i>).
110106	Updated schematics.

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DS2156, DS2155, DS2135Y DESIGN KIT									C
CONTENTS									B
1. COVER PAGE									A
2. SCT POPULATION OPTION (DS2155, DS2156, DS21352 OR DS21354)									
3. TX AND RX ANALOG PATHS									
4. TIM ADDRESS AND DATA BUS									
5. CPLD ADDRESS DATA CONNECTIONS, BIAS LEVELS FOR SCT									
6. UTOPIA: TIM HEADER AND BUS SWITCHES									
7. TESTPOINTS FOR UTOPIA 2									
8. UTOPIA: NETLIST ASSOCIATIONS									
9. SWITCHING FOR CLOCKS AND TDM									
10. SUPPLY DECOUPLING									
11. SCT TESTPOINTS									
12. NETLIST CROSS-REFERENCE									
13. PART CROSS-REFERENCE									
TITLE:						DS2156DK02A0		DATE:	10/04/02
ENGINEER:						STEVE SCULLY		PAGE:	1 / 13
8		7	6	5	4	3	2	1	D

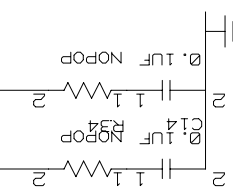
10/04/02

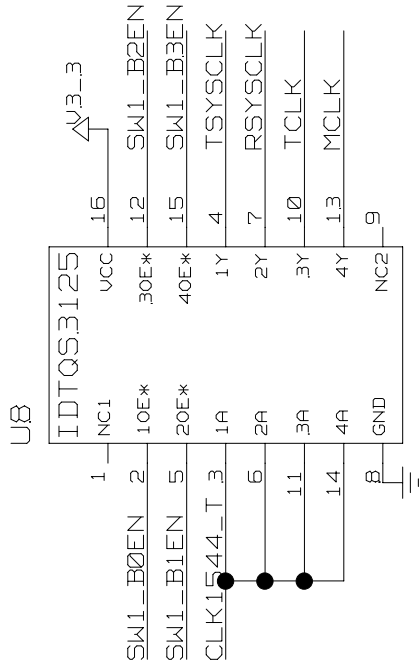
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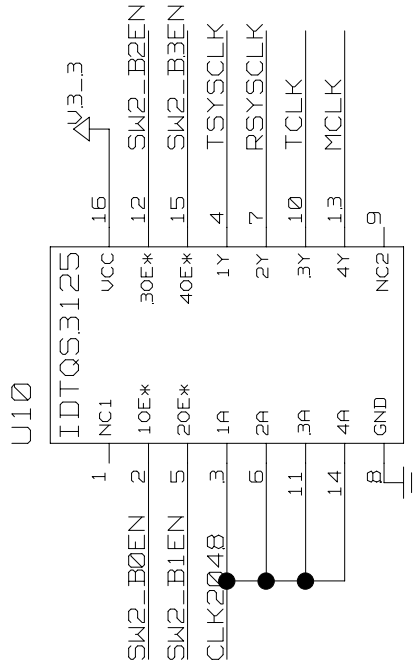


TITLE:	DS2156DK02A0	DATE:	10/04/02
ENGINEER:	STEVE SCULLY	PAGE:	5 / 13

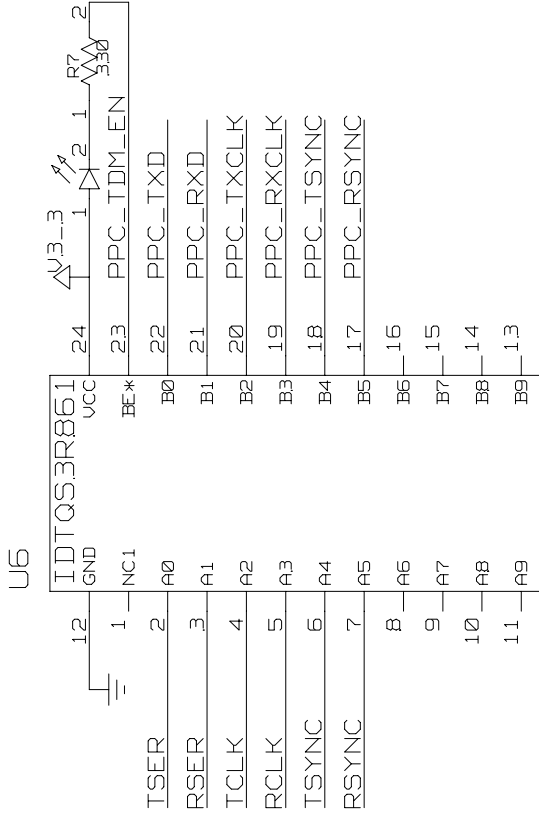
8		7	6	5	4	3	2	1
RXADDR0 UR_ADDR0 RXA_0 UR_ENB RCHCLK				RXENB RXENA UR_ENB BPCLK			TXDATA_6 TXDATA_6 UT_DATA6 TSIG	
RXADDR1 UR_ADDR1 RXA_1 UR_ADDR1 RSIGF				RXSOC RXSOC UR_SOC RCHBLK				
RXADDR2 UR_ADDR2 RXA_2_RXCLAV_1 UR_ADDR2 RSIG				TXADDR0 TXA_0 UT_ADDR0 UOP3			TXDATA_7 TXDATA_7 UT_DATA7 TSYSCLK	
RXADDR3 UR_ADDR3 RXA_3_RXCLAV_2 UR_ADDR3 RMSYNC				TXADDR1 TXA_1 UT_ADDR1 TCHBLK				
RXADDR4 UR_ADDR4 RXA_4_RXCLAV_3 UR_ADDR4 RFSYNC				TXADDR2 TXA_2_TXCLAV_1 UT_ADDR2 TLCLK				
RXCLAV0 UR_CLAV RXCLAV_0 UR_CLAV RSER				TXADDR3 TXA_3_TXCLAV_2 UT_ADDR3 TLINK			TXENABLE TXENA UT_ENB UOP1	
RXDATA_0 UR_DATA0 RXDATA_0 UR_DATA0 RLINK				TXADDR4 TXA_4_TXCLAV_3 UT_ADDR4 TPOSI				
RXDATA_1 UR_DATA1 RXDATA_1 UR_DATA1 RLCLK				TXCLAV0 UT_CLAV TXCLAV_0 LIUC			TXSOC TXSOC UT_SOC UOP0	
RXDATA_2 UR_DATA2 RXDATA_2 UR_DATA2 RPOSI				TXDATA_0 TXDATA_0 UT_DATA0 TNEGI				
RXDATA_3 UR_DATA3 RXDATA_3 UR_DATA3 RNEGI				TXDATA_1 TXDATA_1 UT_DATA1 TCLKI				
RXDATA_4 UR_DATA4 RXDATA_4 UR_DATA4 RCLKI				TXDATA_2 TXDATA_2 UT_DATA2 TCLKO			UT_CLK TSSYNC	
RXDATA_5 UR_DATA5 RXDATA_5 UR_DATA5 RCLKO				TXDATA_3 TXDATA_3 UT_DATA3 TNEGO			UR_CLK TCHCLK	
RXDATA_6 UR_DATA6 RXDATA_6 UR_DATA6 RNEGO				TXDATA_4 TXDATA_4 UT_DATA4 TPOSO				
RXDATA_7 UR_DATA7 RXDATA_7 UR_DATA7 RPOSO				TXDATA_5 TXDATA_5 UT_DATA5 TSER				
TITLE: DS2156DK02A0						DATE: 10/04/02		
						ENGINEER: STEVE SCULLY		PAGE: 8 / 13
8		7	6	5	4	3	2	1



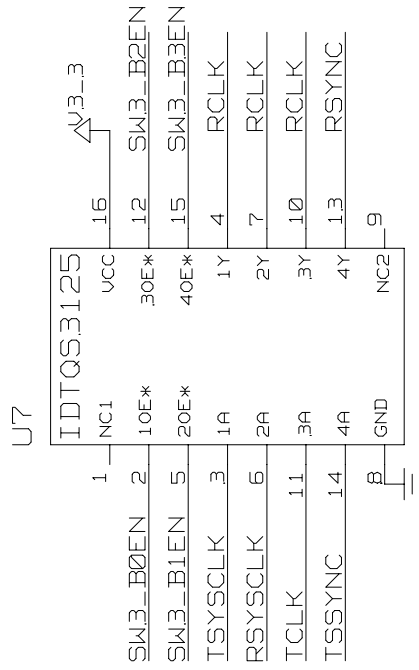
SWITCH 1 IS MEMORY MAPPED
TO PLD REGISTER 1
LOGIC 0 OPENS SWITCH 1



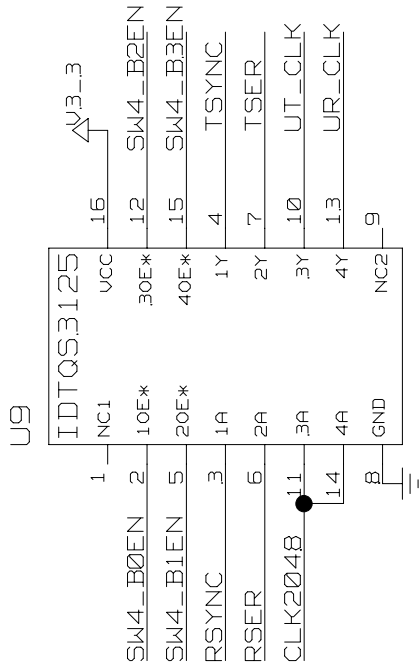
LOGIC 1
LOGIC 0
TO PLD REGISTER SWITCH
SWITCH 2 IS NEXT, MAPPED



PPC-TDM-EN IS BIT MAPPED TO
PLD-ADDRESSES 15 BITCHES
LOGIC CLOSURES SWITCHES



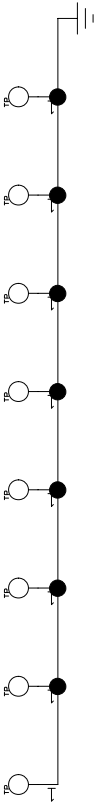
SWITCH 3 IS MEMORY MAPPED
TO PLD REGISTER 13
LOGIC 0 CLEANS SWITCH
LOGIC 1 OPENS SWITCH



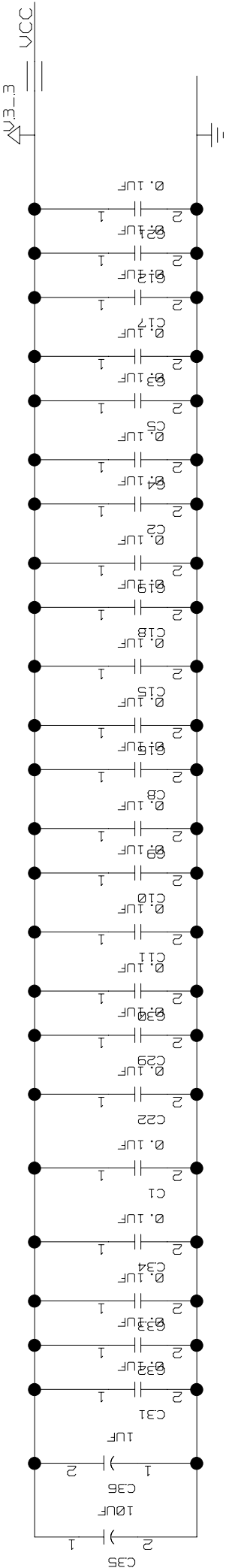
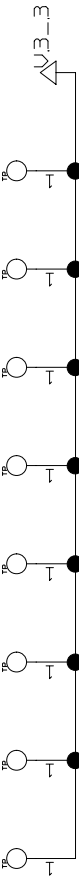
SWITCH 4 IS MEMORY MAPPED
TO PLD REGISTER 0X14
LOGIC 0 CLOSSES SWITCH
LOGIC 1 OPENS SWITCH

D	C	B	A
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16

TP24 TP25 TP26 TP27 TP28 TP29 TP23 TP30



TP33 TP38 TP37 TP36 TP35 TP34 TP32 TP31



B		7	6	5	4	3	2	1
*** Signal Cross-Reference for the entire design ***								
BXCLK	2CB> 11C7>	2D6> BB7> 11D6<						
A0	4C6<> 5C4<> 2B3< 11B3<	2C3> 5B2<> 11C3>						
A1	4C6<> 5C4<> 2B3< 11B3<	2A5> BC7> 11A5>						
A2	4C6<> 5C4<> 2B3< 11B3<	BB7> 2CB< 5AB< 11C7<						
A3	4C6<> 5C4<> 2B3< 11B3<	BB7> 2CB< 5AB< 11C7<						
A4	4C6<> 5C4<> 2B3< 11B3<	2CB> BA7> 11C7>						
A5	4C6<> 5C4<> 2B3< 11B3<	2CB< 3BB< 11C7<						
A6	4C6<> 5C4<> 2B3< 11B3<	2A5> BC7> 9A6<> 9B3<> 11A5>						
A7	4C6<> 5C4<> 2B3< 11B3<	2A5> BD7> 11A5>						
A8	4C6<> 5C4<> 2B3< 11B3<	2A5> BD7> 11A4>						
A9	4B6<> 7B1<>	2D6<> 9A6<> 9B3<> 9C1<> 11D5<>						
A10	4C3<> 7C3<>	5A6<						
A11	4C3<> 5C1<> 7C3<>	9B6<> 9C3<> 9D6<> 2D6< 5AB< 11D5<						
A12	4C3<> 5C1<> 7B3<>	2CB< 3BB< 11C7<						
A13	4B3<> 7B3<>	4B6<> 5B1<> 7B1<>						
A14	4B3<>	7BB<> 8D8						
A15	4B3<>	7BB<> 8D8						
BPCLK	2A5> BD4> 11A4>	7BB<> 8D8						
BP_EN	5C1<> 6B2< 6B6< 6C2< 6C6<	7BB<> 8CB						
BTS	5D4<> 2B3< 5A6< 11A3<	7B6<> 8CB						
CLK1544_T	7B3<> 9D8<> 4B2<	6B2<> BD7>						
CLK204B	5D3<> 9B3<> 9B8<>	6A7<> 6C7<> BC7>						
CLK163B4_T	4B4<> 5D3<> 7B3<>	6A7<> 6B2<> BC7>						
CS_T	5B4<> 2C3< 11C3<	7AB<> 8CB						
	4BB<> 5B1<> 7B3<>	6A7<> 8C7>						
D_AD0	2B3<> 4B6<> 5C1<> 11B3<>	6B7<> 7CB<> BB7> BB8						
D_AD1	2C3<> 4B6<> 5C1<> 11B3<>	6A2<> 7C6<> BB7> BB8						
D_AD2	2C3<> 4B6<> 5C1<> 11C3<>	6B7<> 7CB<> BB7> BB8						
D_AD3	2C3<> 4B6<> 5C1<> 11C3<>	6B2<> 7C6<> BB7> BB8						
D_AD4	2C3<> 4B6<> 5C1<> 11C3<>	6B7<> 7C6<> BB7> BB8						
D_AD5	2C3<> 4B6<> 5C1<> 11C3<>	6B7<> 7C6<> BA7> BAB						
D_AD6	2C3<> 4A6<> 5C1<> 11C3<>	6B2<> 7CB<> BA7> BAB						
D_AD7	2C3<> 4A6<> 5D1<> 11C3<>	6B7<> 7C6<> BA7> BAB						
ESI8RD	2A5<> 11A4<>> 5AB<	6B2<> 7CB<> BA7> BAB						
ESI8S0	2A6<> 11A6<>	6A2<> BD4>						
ESI8S1	2A6<> 11A5<>	6B5<>						
INT	2C3> 4AB<> 5A2<> 11C3> 5A6<	6B7<> 7B6<> BD4> BD5						
INT_INDICATOR	5A2<>	4C2<>						
JTCLK	2AB< 11A7<	4C2<>						
JTDI	2AB< 11A7<	4C2<>						
JTDO	2AB< 11A7>	4C2<>						
JTMS	2BB< 11B7<	4C2<>						
JTRST	2BB< 5AB< 11A7<	5A4<> 9D8<						
LIUC	BB4> 2CB< 5A6< 11B7<	5A4<> 9D8<						
MCLK	9B6<> 9C6<> 2A5< 11A5<	5A3<> 9D6<						
MUX	5C4<> 2A3< 5AB< 11A3<	5A3<> 9B8<						
NIMD8	4B2<>	5A3<> 9B8<						
NIMD9	4B2<>	5A3<> 9B6<						
NIMD10	4B2<>	5A3<> 9D3<						
NIMD11	4B2<>	5A3<> 9D1<						
NIMD12	4B2<>	5B4<> 9B3<						
NIMD13	4B2<>	5B4<> 9B3<						
NIMD14	4B2<>	5B4<> 9B2<						
NIMD15	4C2<>	2D3> BC4> 11C3>						
N_P27	2A4< 11A4<	2D5> 11D4> BA1<						
N_P28	2A3< 11A3<	5BB<> 5D8<						
PPC_RSYNC	4CB<> 9A4<>	9A6<> 9B6<> 9C3<> 9C6<> 2D5< 5A6<						
PPC_RXCLK	4CB<> 9A4<>	11D5<						
PPC_RXD	4CB<> 9A4<>	BB4> 2BB< 5AB< 11B7<						
PPC_TDM_EN	5C1<> 9A4<	2BB> BA4> 11B7>						
PPC_TSYNC	4BB<> 9A4<>	2D5<> 11D4<>						
PPC_TXCLK	4CB<> 9A4<>	5BB<> 5D7<						
PPC_TXD	4CB<> 9A4<>	5BB<> 5C7<						
RCHBLK	2C3> BD4> 11C3>	4D3<> 4D8<>						
RCHCLK	2D6> BD7> 11D5>	2D5> BC4> 11D4>						
RCL	2CB> 11C7>	BC4> 2D5< 5B6< 11D5<						
RCLK	2D6> 9A6<> 9C1<> 9C1<> 9D1<> 11D6>	5BB<> 5C7<						
RCLKI	BA7> 2CB< 5AB< 11C7<	TCLKI						
RCLKO	2CB> BA7> 11C7>	TCLKO						
RDATA	2D6> 11D5>	TDATA						
RD_DS	5C4> 2A3< 11A3<	TDI						
RESET_OUT	4B6<> 5B1<> 7B1<>	TDO						
RFSYNC	2D6> BC7> 11D5>	TIMSV						
RLCLK	2D6> BB7> 11D5>	TLCLK						
		TLINK						
		TMS						

B		7		6		5		4		3		2		1	
*** Part Cross-Reference for the entire design ***															
1	DS2156_TQFP 11D7														
C1	CAP 10B5														
C2	CAP 10B3														
C3	CAP 10B2														
C4	CAP 10B2														
C5	CAP 10B2														
C7	CAP 3D5														
C8	CAP 10B4														
C9	CAP 10B4														
C10	CAP 10B4														
C11	CAP 10B4														
C12	CAP 10B2														
C13	CAP 8A1														
C14	CAP 8A1														
C15	CAP 10B3														
C16	CAP 10B3														
C17	CAP 10B2														
C18	CAP 10B3														
C19	CAP 10B3														
C21	CAP 10B2														
C22	CAP 10B5														
C23	CAP 3A6														
C24	CAP 3C5														
C25	CAP 3B5														
C26	CAP 3A5														
C27	CAP 3D5														
C29	CAP 10B4														
C30	CAP 10B4														
C31	CAP 10B6														
C32	CAP 10B5														
C33	CAP 10B5														
C34	CAP 10B5														
C35	CAP 10B5														
C36	CAP 10B6														
DS1	LED 9B4														
DS2	LED 5A2														
DS3	LED 5A2														
DS4	LED 6D5														
DS5	LED 5A3														
DS6	LED 5A4														
DS7	LED 5A3														
DS8	LED 5A4														
DS9	LED 5A4														
DS10	LED 5A3														
DS11	LED 5A4														
DS12	LED 5A3														
DS13	LED 5A3														
DS14	LED 5A3														
DS15	LED 5A3														
DS16	LED 5B5														
DS17	LED 5B5														
DS18	LED 5A3														
F1	FUSE 3B4														
F2	FUSE 3B4														
F3	FUSE 3D4														
F4	FUSE 3C4														
F5	FUSE 3D4														
F6	FUSE 3A3														
J1	CONN_50P1 7D5														
J2	CONN_50P1 7D7														
J3	CONN_BANTAM_IPC 3B1														
J4	CONN_BANTAM_IPC 3C1														
J5	CONN_BNC_SPIN 3A3														
J6	CONN_BNC_SPIN 3D2														
J7	CONN_50P2 6D4														
J8	CONN_50P2 4D3														
J9	CONN_50P2 4D7														
JT10	CONN_10P 5CB														
L1	CHOKE_DUAL-T1 3B4 3C4														
R1	RES1 4B2														
R2	RES 3B7														
R3	RES 3B7														
R4	RES 6A2														
R5	RES 6C2														
R6	RES1 5A7														