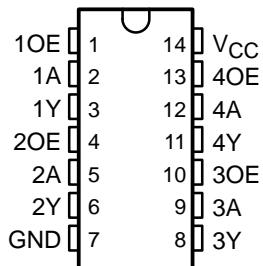


- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 6.5 ns at 5 V
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

#### description/ordering information

The SN74F126 bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

D, N, OR NS PACKAGE  
(TOP VIEW)



To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74F126N	SN74F126N
	SOIC – D	Tube	SN74F126D	F126
		Tape and reel	SN74F126DR	
	SOP – NS	Tape and reel	SN74F126NSR	74F126

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

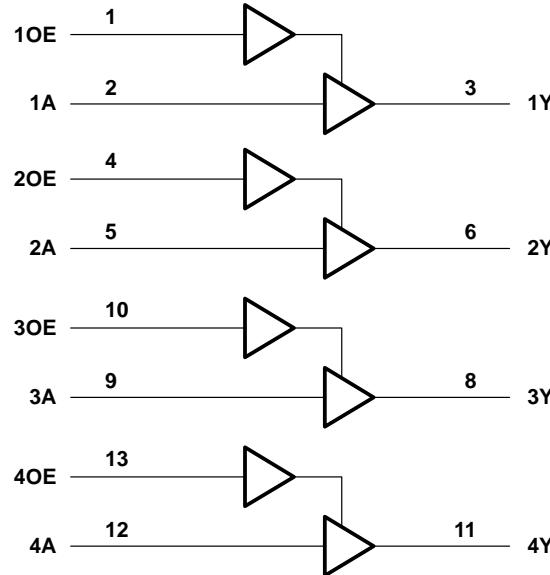


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**SN74F126  
QUADRUPLE BUS BUFFER GATE  
WITH 3-STATE OUTPUTS**

SDFS017B – JANUARY 1989 – REVISED NOVEMBER 2002

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-15	mA
$I_{OL}$	Low-level output current			64	mA
$T_A$	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74F126  
QUADRUPLE BUS BUFFER GATE  
WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	I <sub>I</sub> = -18 mA	4.5 V			-1.2	V
V <sub>OH</sub>	I <sub>OH</sub> = -3 mA	4.5 V	2.4	3.3		V
	I <sub>OH</sub> = -15 mA		2	3.1		
	I <sub>OH</sub> = -3 mA	4.75 V	2.7			
V <sub>OL</sub>	I <sub>OL</sub> = 64 mA	4.5 V	0.4	0.55		V
I <sub>I</sub>	V <sub>I</sub> = 7 V	0			0.1	mA
I <sub>IH</sub>	V <sub>I</sub> = 2.7 V	5.5 V			20	µA
I <sub>IL</sub>	V <sub>I</sub> = 0.5 V	5.5 V			-20	µA
I <sub>OZH</sub>	V <sub>O</sub> = 2.7 V	5.5 V			50	µA
I <sub>OZL</sub>	V <sub>O</sub> = 0.5 V	5.5 V			-50	µA
I <sub>OS</sub> ‡	V <sub>O</sub> = 0	5.5 V	-100		-225	mA
I <sub>CCH</sub>	Outputs open	5.5 V	20	30		mA
I <sub>CCL</sub>	Outputs open	5.5 V	32	48		mA
I <sub>CCZ</sub>	Outputs open	5.5 V	26	39		mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

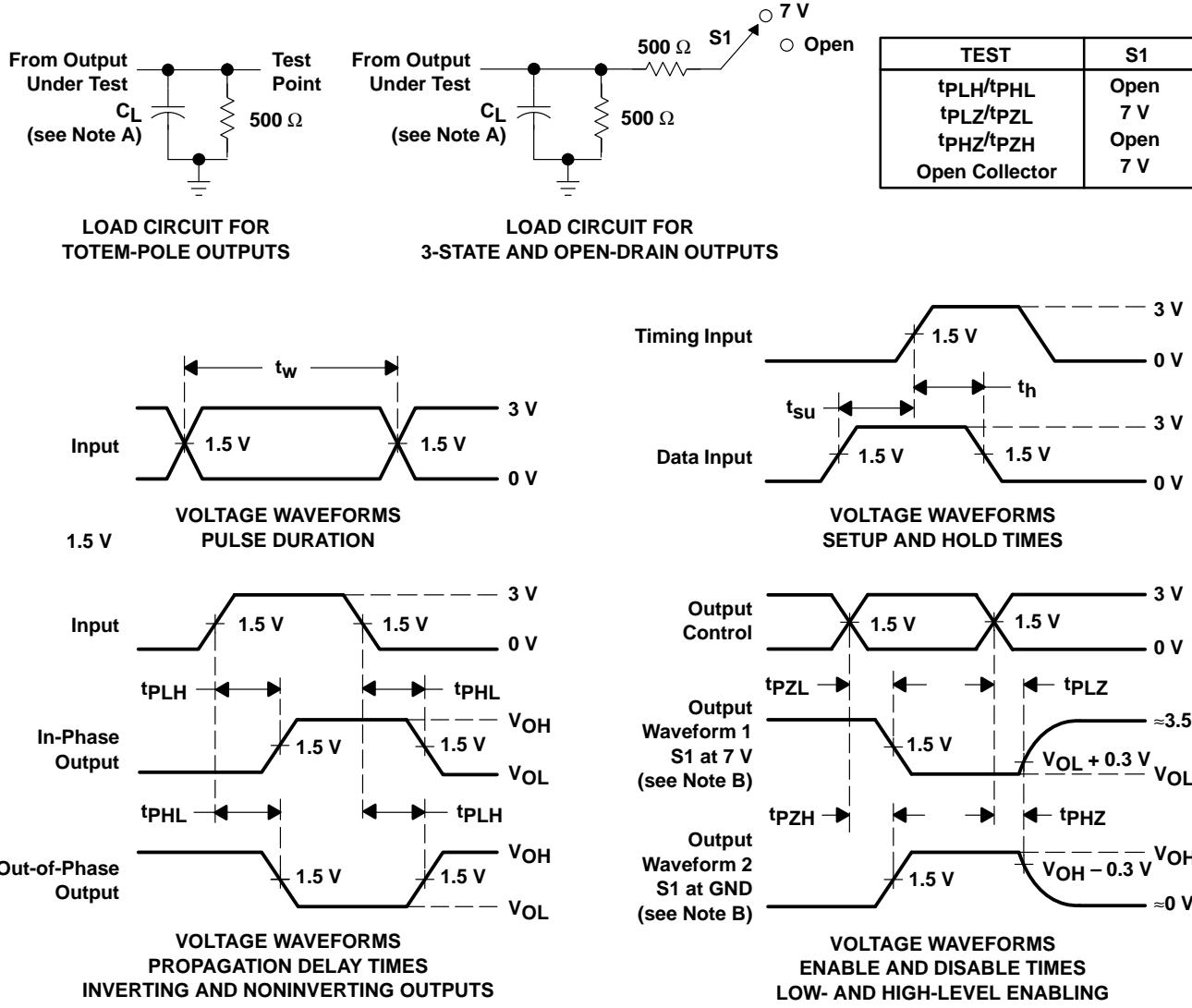
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX§	UNIT	
			MIN	TYP	MAX	
t <sub>PLH</sub>	A	Y	2	4	6.5	ns
			3	5.5	8	
t <sub>PHL</sub>	OE	Y	3.8	6	7.5	ns
			3.8	6	8	
t <sub>PZH</sub>	OE	Y	2	4.5	6.5	ns
			3	5.5	7.5	
t <sub>PZL</sub>	OE	Y	2	4.5	6.5	ns
			3	5.5	7.5	
t <sub>PHZ</sub>	OE	Y	2	4.5	6.5	ns
			3	5.5	7.5	
t <sub>PLZ</sub>	OE	Y	2	4.5	6.5	ns
			3	5.5	7.5	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN74F126**  
**QUADRUPLE BUS BUFFER GATE**  
**WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION**



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns, duty cycle = 50%.
- The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74F126D</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	F126
<a href="#">SN74F126DR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F126
SN74F126DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F126
<a href="#">SN74F126N</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F126N
SN74F126N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F126N

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

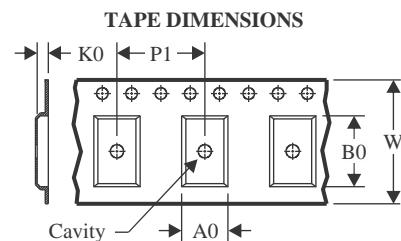
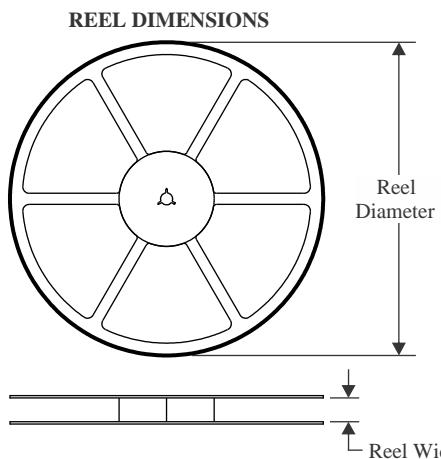
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

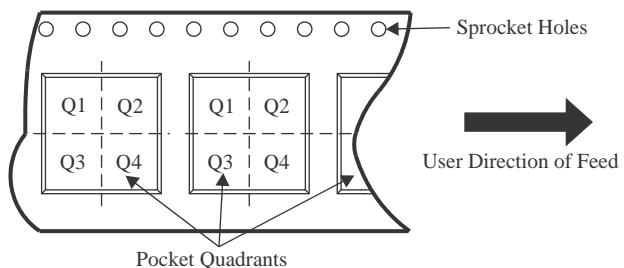
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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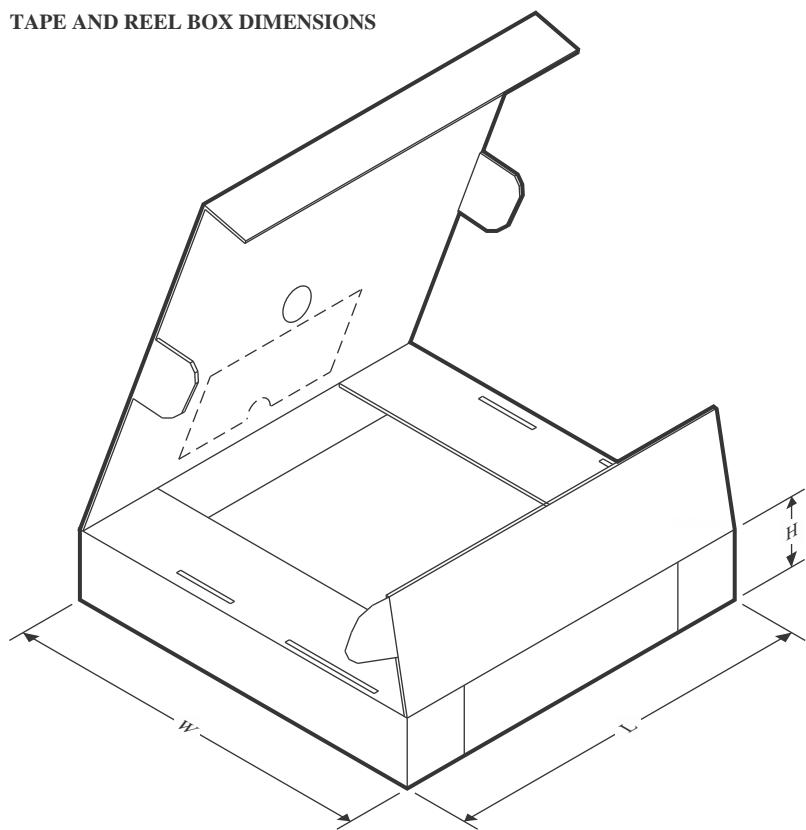
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


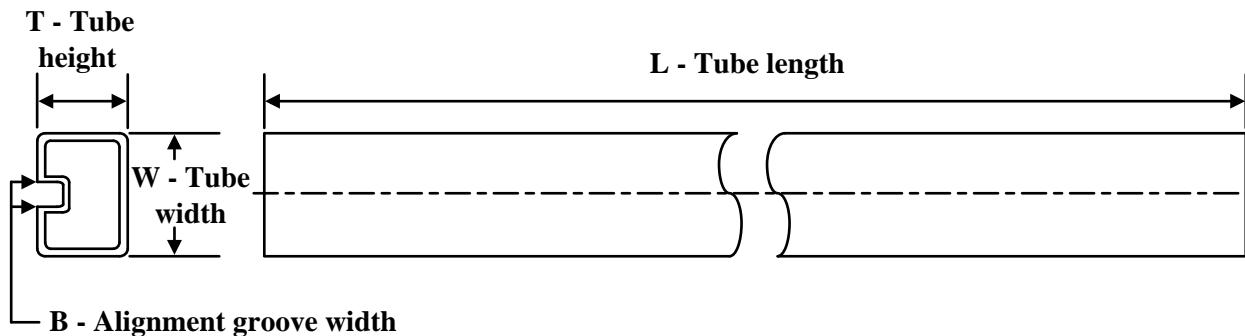
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F126DR	SOIC	D	14	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

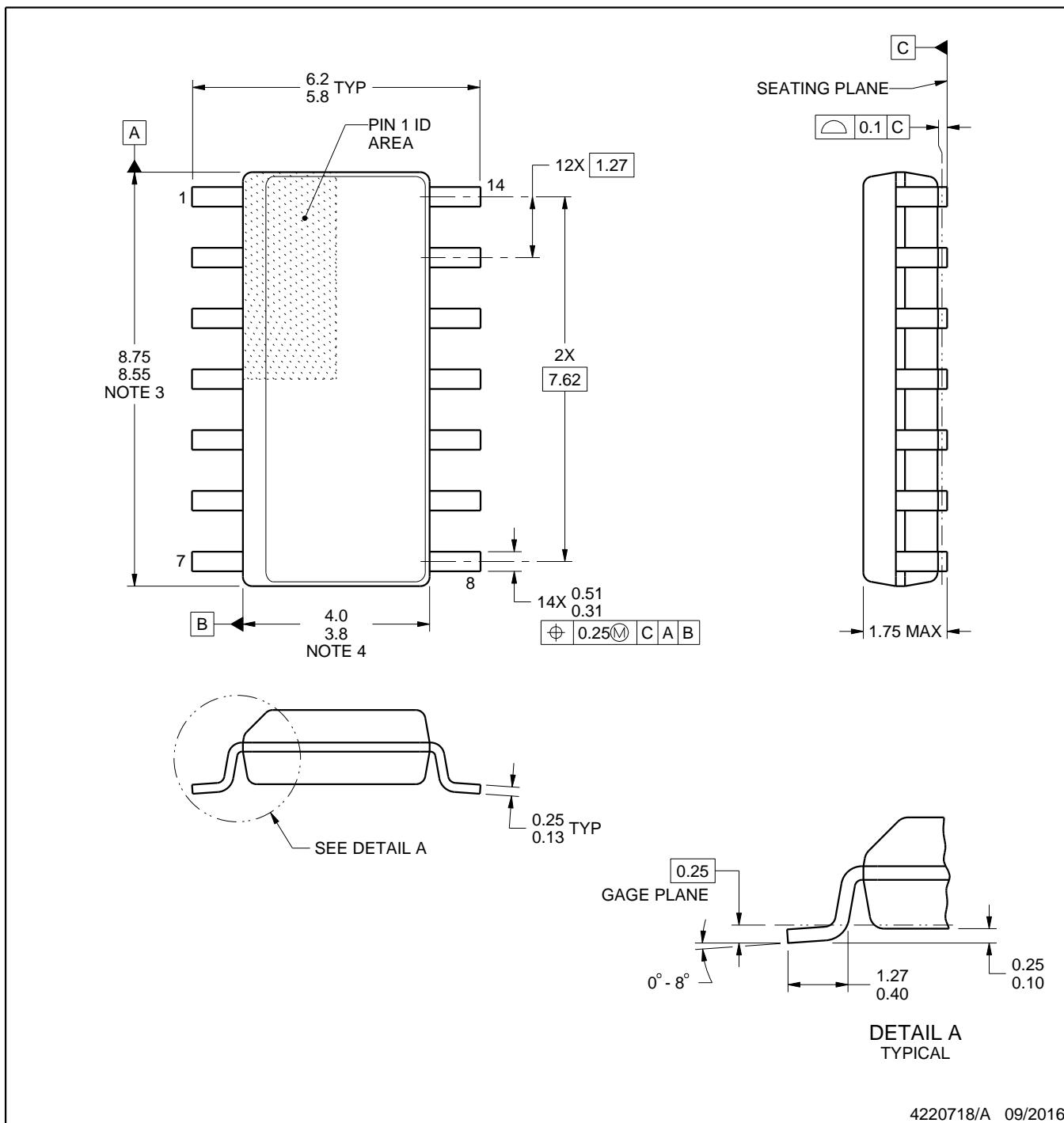
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
SN74F126N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F126N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F126N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74F126N.A	N	PDIP	14	25	506	13.97	11230	4.32

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

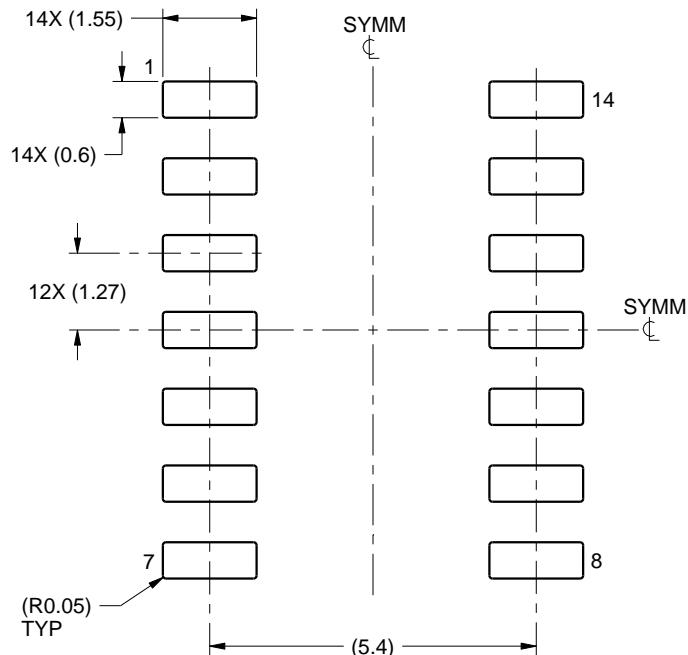
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

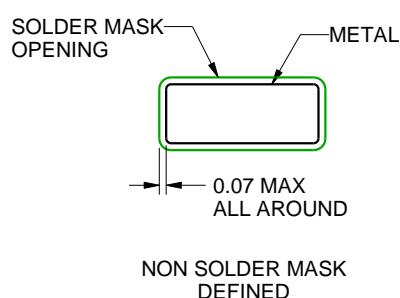
D0014A

SOIC - 1.75 mm max height

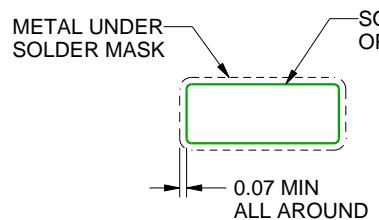
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

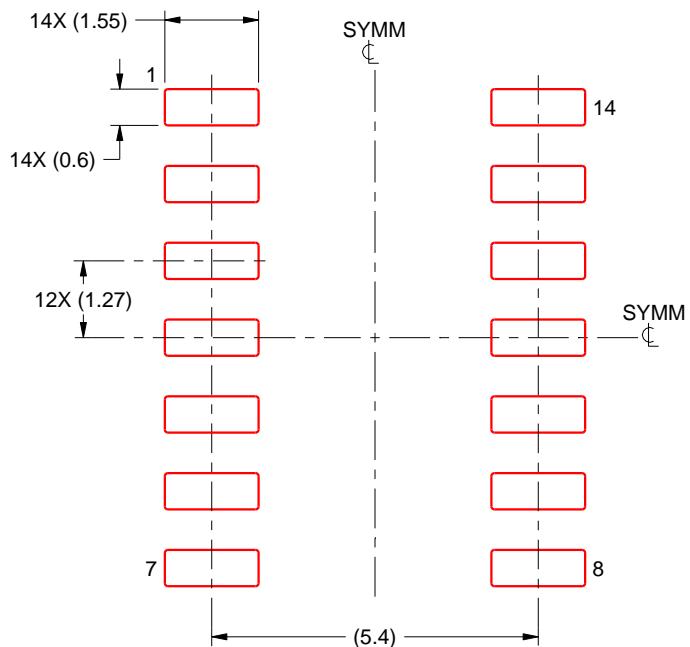
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**D0014A**

## **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



**SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X**

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



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