N-Channel Depletion-Mode Vertical DMOS FETs

Features

- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on-resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

- Normally-on switches
- Solid state relays
- Converters
- Constant current sources
- Power supply circuits
- Telecom

General Description

The Supertex DN3525 is a low threshold depletion-mode (normally-on) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Part Number	Package Option	Packing
DN3525N8-G	TO-243AA (SOT-89)	2000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package.
Contact factory for Wafer / Die availablity.
Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

Product Summary

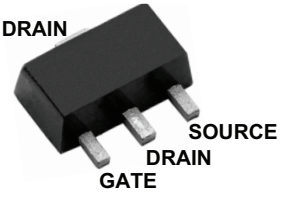
BV_{DSX}/BV_{DGX}	$R_{DS(ON)}$ (max)	I_{DSS} (min)
250mA	6.0Ω	300mA

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSX}
Drain-to-gate voltage	BV_{DGX}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



TO-243AA (SOT-89)

Typical Thermal Resistance

Package	θ_{ja}
TO-243AA (SOT-89)	133°C/W

Note:

Mounted on FR5 board, 25mm x 25mm x 1.57mm.

Product Marking

W = Code for week sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or 

TO-243AA (SOT-89)

Thermal Characteristics

Package	I_D (continuous)†	I_D (pulsed)	Power Dissipation @T_A = 25°C	I_{DR}†	I_{DRM}
TO-243AA	360mA	1.0A	1.6W‡	360mA	1.0A

Notes:

† I_D (continuous) is limited by max rated T_J.

‡ Mounted on FR5 board, 25mm x 25mm x 1.57mm.

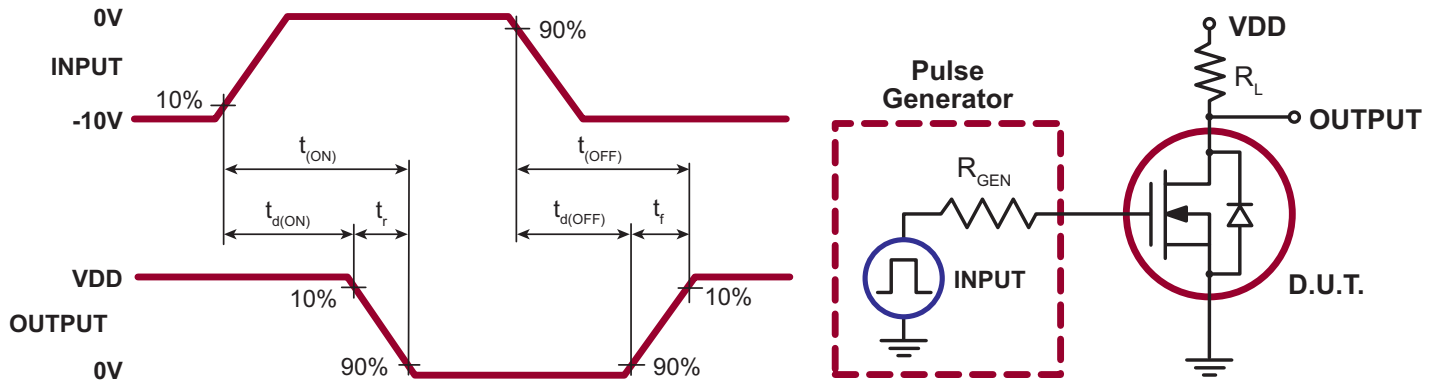
Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSX}	Drain-to-source breakdown voltage	250	-	-	V	V_{GS} = -5.0V, I_D = 100µA
$V_{GS(OFF)}$	Gate-to-source off voltage	-1.5	-	-3.5	V	V_{DS} = 15V, I_D = 1.0mA
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with temperature	-	-	-4.5	mV/°C	V_{DS} = 15V, I_D = 1.0mA
I_{GSS}	Gate body leakage current	-	-	100	nA	V_{GS} = ±20V, V_{DS} = 0V
$I_{D(OFF)}$	Drain-to-source leakage current	-	-	1.0	µA	V_{DS} = Max rating, V_{GS} = -5.0V
		-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = -5.0V, T_A = 125°C
I_{DSS}	Saturated drain-to-source current	300	-	-	mA	V_{GS} = 0V, V_{DS} = 15V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	6.0	Ω	V_{GS} = 0V, I_D = 200mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.1	%/°C	V_{GS} = 0V, I_D = 200mA
G_{FS}	Forward transconductance	225	-	-	mmho	V_{DS} = 10V, I_D = 150mA
C_{ISS}	Input capacitance	-	270	350	pF	V_{GS} = -5.0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	20	60		
C_{RSS}	Reverse transfer capacitance	-	5.0	20		
$t_{d(ON)}$	Turn-on delay time	-	-	20	ns	V_{DD} = 25V, I_D = 150mA, R_{GEN} = 25Ω, V_{GS} = 0V to -10V
t_r	Rise time	-	-	25		
$t_{d(OFF)}$	Turn-off delay time	-	-	25		
t_f	Fall time	-	-	40		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	V_{GS} = -5.0V, I_{SD} = 150mA
t_{rr}	Reverse recovery time	-	800	-	ns	V_{GS} = -5.0V, I_{SD} = 150mA

Notes:

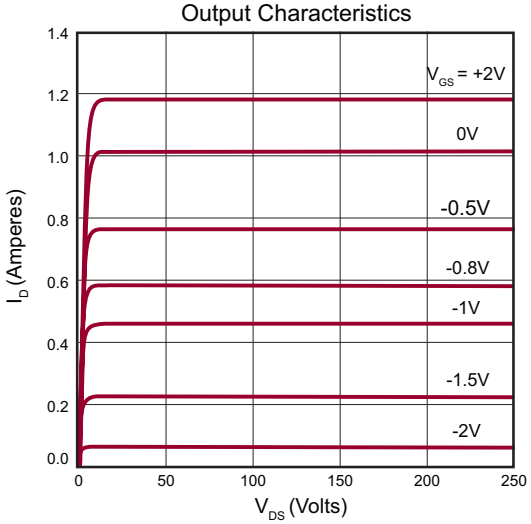
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit

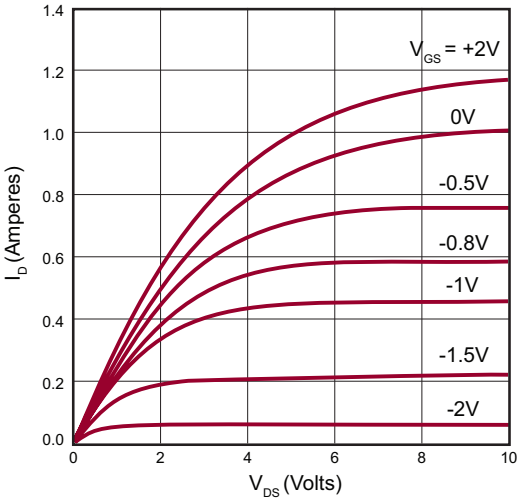


Typical Performance Curves

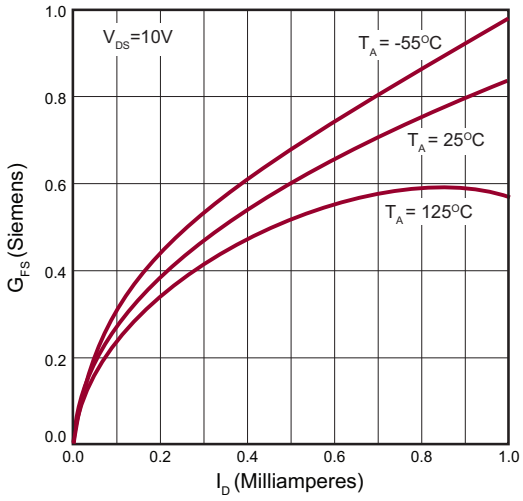
Output Characteristics



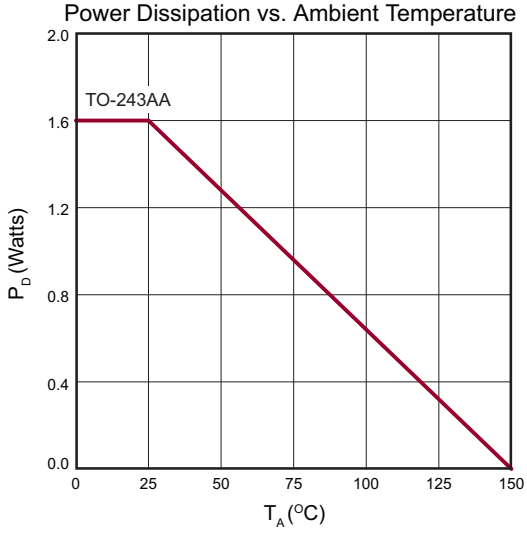
Saturation Characteristics



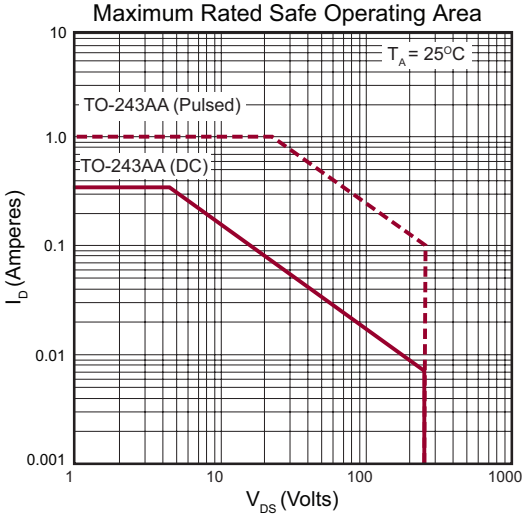
Transconductance vs. Drain Current



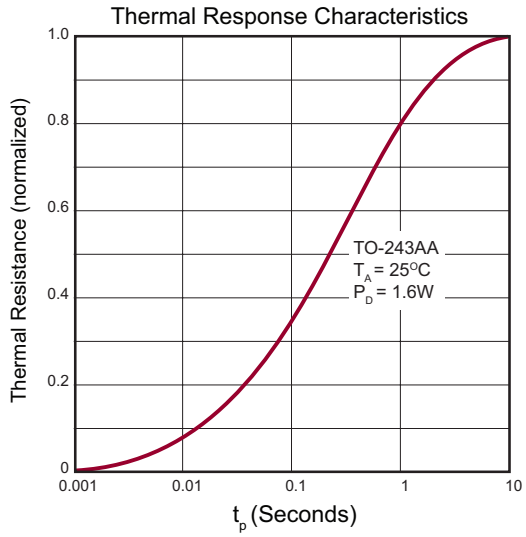
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

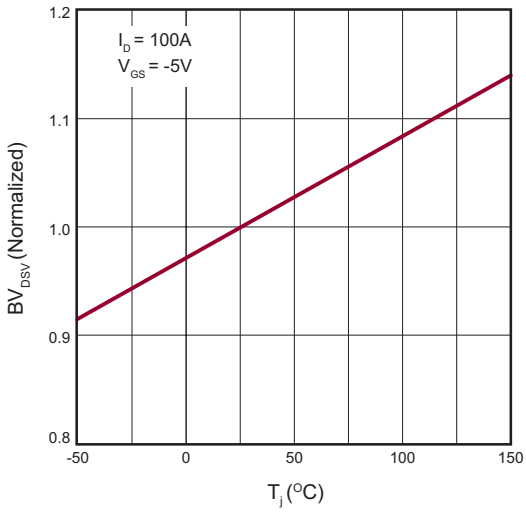


Thermal Response Characteristics

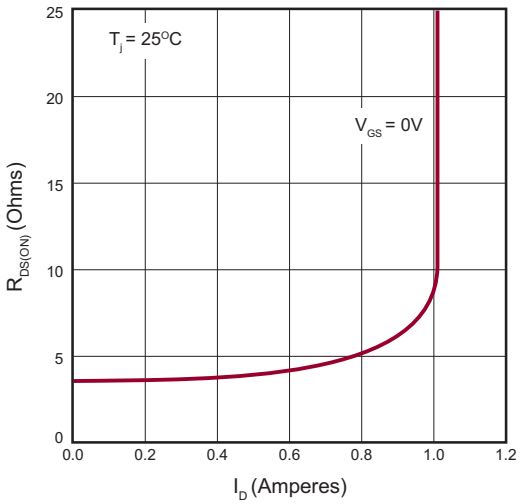


Typical Performance Curves *(cont.)*

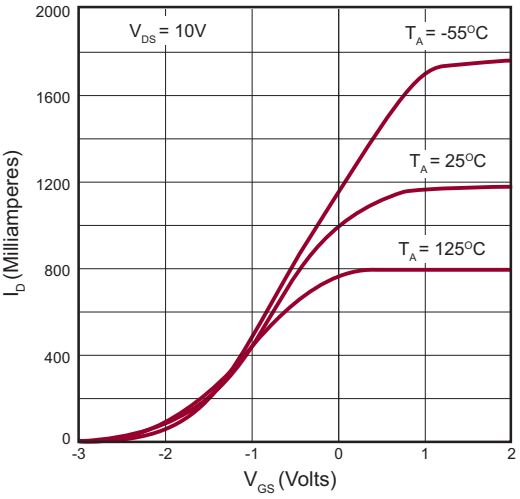
BV$_{DSV}$ Variation with Temperature



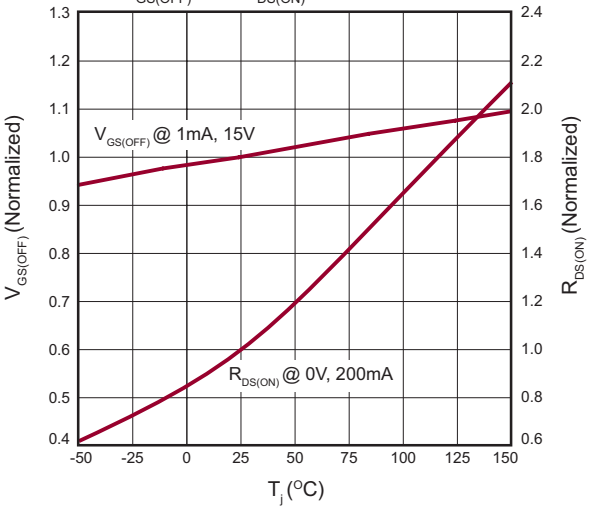
On Resistance vs. Drain Current



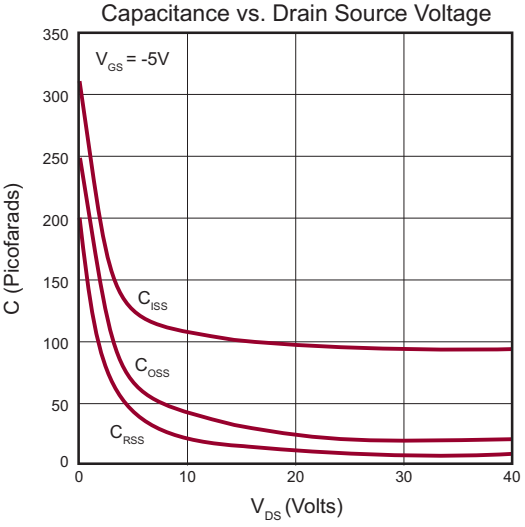
Transfer Characteristics



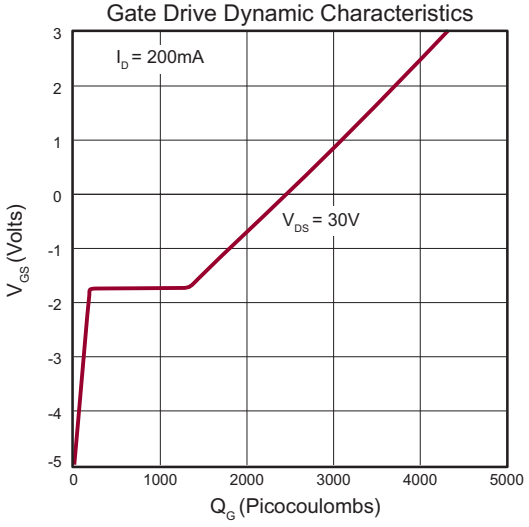
V$_{GS(OFF)}$ and R$_{DS(ON)}$ w/ Temperature



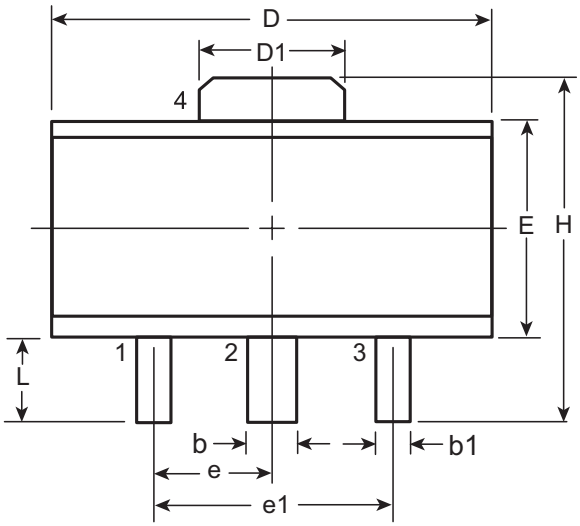
Capacitance vs. Drain Source Voltage



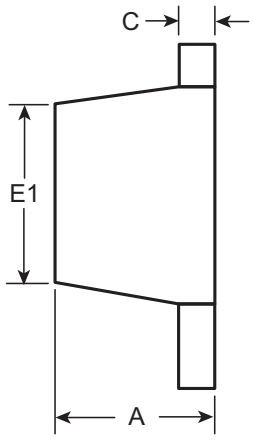
Gate Drive Dynamic Characteristics



3-Lead TO-243AA (SOT-89) Package Outline (N8)



Top View



Side View

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.73†
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.
† *This dimension differs from the JEDEC drawing*
Drawings not to scale.
Supertex Doc. #: *DSPD-3TO243AAN8, Version F111010.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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