OctalLIU™

Octal E1/T1/J1 Line Interface Component for Long- and Short-Haul Applications

PEF 22508 E, Version 1.1

Wireline Communications

Never stop thinking.

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Preface

The OctalLIU™ is an 8 channel E1/T1/J1 Line interface Component, it is designed to fulfill all required interfacing between 8 analog E1/T1/J1 lines and 8 digital framers.

The digital functions as well as the analog characteristics can be configured either via a flexible microprocessor interface, SPI interface or via a SCI interface.

Organization of this Document

This Data Sheet is organized as follows:

- **Chapter 1**, “Introduction”: Gives a general description of the product and its family, lists the key features, and presents some typical applications.
- **Chapter 2**, “Pin Descriptions”: Lists pin locations with associated signals, categorizes signals according to function, and describe signals.
- **Chapter 3**, “Functional Description”: Describes the functional blocks and principle operation modes, organized into separate sections for E1 and T1/J1 operation
- **Chapter 4**, “Registers”: Gives a detailed description of all implemented registers and how to use them in different applications/configurations.
- **Chapter 5**, “Package Outlines”: Shows the mechanical characteristics of the device packages.
- **Chapter 6**, “Electrical Characteristics”: Specifies maximum ratings, DC and AC characteristics.
- **Chapter 7**, “Operational Description”: Shows the operation modes and how they are to be initialized (separately for E1 and T1/J1).
- **Chapter 8**, “Appendix”: Gives an example for over voltage protection and information about application notes and tool support.

Related Documentation

This document refers to the following international standards (in alphabetical/numerical order):

ANSI/EIA-656
ANSI T1.102
ANSI T1.231
ANSI T1.403
AT&T PUB 43802
AT&T PUB 54016
AT&T PUB 62411
ESD Ass. Standard EOS/ESD-5.1-1993
ETSI ETS 300 011
ETSI ETS 300 233
ETSI TBR12
ETSI TBR13
FCC Part68
H.100
H-MVIP
IEEE 1149.1
TR-TSY-000009
TR-TSY-000253
TR-TSY-000499
ITU-T G.703
ITU-T G.736
ITU-T G.737
ITU-T G.738
ITU-T G.739
ITU.T G.733
ITU-T G.775
ITU-T G.823
ITU-T G.824
ITU-T I.431
JT-G703
JT-G704
JT-G706
JT-G33
JT-I431
MIL-Std. 883D
UL 1459

1 Introduction

The OctalLIU™ is the latest addition to Infineon's family of sophisticated E1/T1/J1 Line interface Components. This monolithic 8 channel device is designed to fulfill all required interfacing between eight analog E1/T1/J1 lines and eight digital framer interfaces for world market telecommunication systems.

The device is supplied in a 17 mm x 17 mm LBGA package, and is designed to minimize the number of external components required, so reducing system costs and board space.

Due to its multitude of implemented functions, it fits to a wide range of networking applications and fulfills the according international standards.

Crystal-less jitter attenuation with only one master clock source reduces the amount of required external components.

Equipped with a flexible microprocessor interface, a SCI and a SPI interface, it connects to various control processor environment. A standard boundary scan interface is provided to support board level testing. LBGA device packaging, minimum number of external components and low power consumption lead to reduced overall system costs.

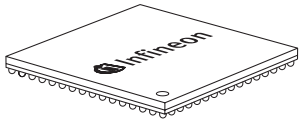
Other members of the FALC® family are the QuadLIU™ supporting four line interface components on a single chip, the OctalFALC™ and the QuadFALC® E1/T1/J1 Framer And Line interface Components for long-haul and short-haul applications, supporting 8 or 4 channels on a single chip respectively.

Octal E1/T1/J1 Line Interface Component for Long- and Short-Haul Applications
OctalLIU™

PEF 22508 E

Version 1.1

1.1 Features



P-LBGA-256-1

Line Interface

- High-density, generic interface for all E1/T1/J1 applications
- Eight Analog receive and transmit circuits for long-haul and short-haul applications
- E1 or T1/J1 mode selectable
- Data and clock recovery using an integrated digital phase-locked loop
- Clock generator for jitter-free transmit clocks per channel
- Jitter specifications of ITU-T I.431, G.703, G.736 (E1), G.823 (E1) and AT&T TR62411 (T1/J1) and PUB 62411 are met
- Maximum line attenuation up to -43 dB at 1024 kHz (E1) and up to -36 dB at 772 kHz (T1/J1)
- Flexible programmable transmit pulse shapes for E1 and T1/J1 pulse masks
- Programmable line build-out for CSU signals according to ANSI T1.403 and FCC68: 0 dB, -7.5 dB, -15 dB, -22.5 dB (T1/J1)
- Programmable low transmitter output impedances for high transmit return loss and generic E1/T1/J1 applications
- Tristate function of the analog transmit line outputs
- Transmit line monitor protecting the device from damage
- Flexible tristate functions of the digital receive outputs
- Receive line monitor mode
- Integrated analog switch for generic E1/T1/J1 applications to meet termination resistance 75/120 Ω for E1, 100 Ω for T1 and 110 Ω for J1
- Crystal-less wander and jitter attenuation/compensation according to TR 62411, ETS-TBR 12/13, PUB 62411
- Common master clock reference for E1 and T1/J1 with any frequency within 1.02 and 20 MHz
- Power-down function
- Support of automatic protection switching
- Dual-rail or single-rail digital inputs and outputs
- Unipolar CMI for interfacing fiber-optical transmission routes
- Selectable line codes (E1: HDB3, AMI/T1: B8ZS, AMI with ZCS)
- Loss-of-signal indication with programmable thresholds according to ITU-T G.775, ETS300233 (E1) and ANSI T1.403 (T1/J1)
- Optional data stream muting upon LOS detection
- Programmable receive slicer threshold
- Local loop, digital loop and remote loop for diagnostic purposes. Automatic remote loop switching is possible with In-Band and Out-Band loop codes
- Low power device, two power supply voltages: 1.8 V and 3.3 V

Type	Package
PEF 22508 E	PG-LBGA-256-1

- Alarm and performance monitoring per second 16-bit counter for code violations, PRBS bit errors
- Insertion and extraction of alarm indication signals (AIS)
- Single-bit defect insertion
- Flexible clock frequency for receiver and transmitter
- Dual elastic stores for both, receive and transmit route clock wander and jitter compensation; controlled slip capability and slip indication
- Programmable elastic buffer size: 2 frames/1 frame/short buffer/bypass
- Programmable In-band loop code detection and generation (TR62411)
- Local loop back, payload loop back land remote loop back capabilities (TR54016)
- Flexible pseudo-random binary sequence generator and monitor

Microprocessor Interfaces

- Asynchronous 8/16-bit microprocessor bus interface (Intel or Motorola type selectable)
- SPI bus interface
- SCI bus interface
- All registers directly accessible
- Multiplexed and non-multiplexed address bus operations on asynchronous 8/16-bit microprocessor bus interface
- Hard/software reset options
- Extended interrupt capabilities
- One-second timer (internal or external timing reference)

General

- Boundary scan standard IEEE 1149.1
- PG-LBGA-256-1 package; body size 17 mm × 17 mm; ball pitch 1.0 mm
- Temperature range from -40 to +85 °C
- 1.8 V and 3.3 V power supply
- Typical power consumption 140 mW per channel

Applications

- Wireless base stations
- E1/T1/J1 ATM gateways, multiplexer
- E1/T1/J1 **C**hannel & **D**ata **S**ervice **U**nits (CSU, DSU)
- E1/T1/J1 Internet access equipment
- LAN/WAN router
- ISDN PRI, PABX
- **D**igital **A**ccess **C**rossconnect **S**ystems (DACS)
- SONET/SDH add/drop multiplexer

1.2 Logic Symbol

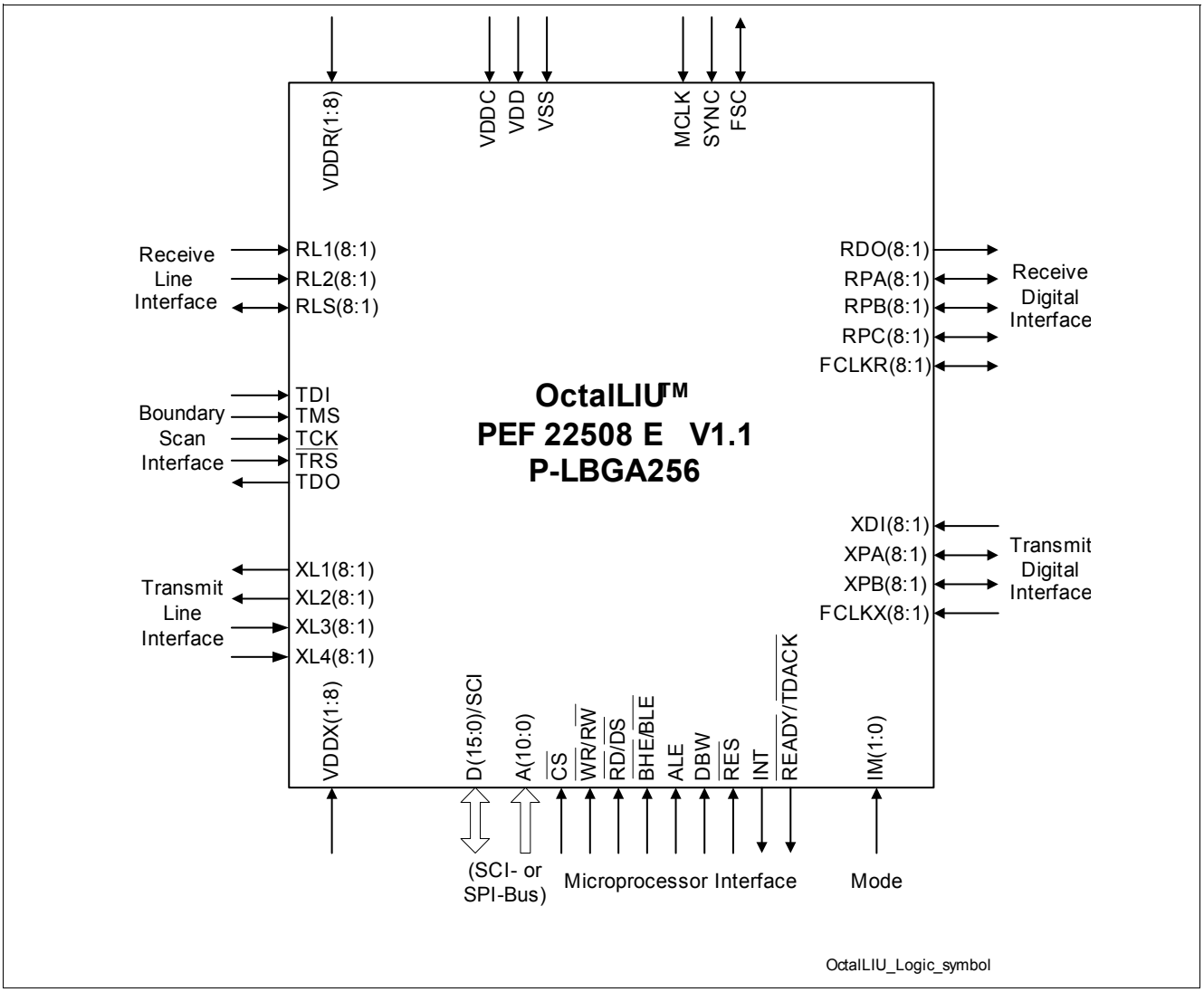


Figure 1 Logic Symbol

1.3 Typical Applications

Figure 2 shows a multiple link application, **Figure 3** a repeater application using the OctalLIU™.

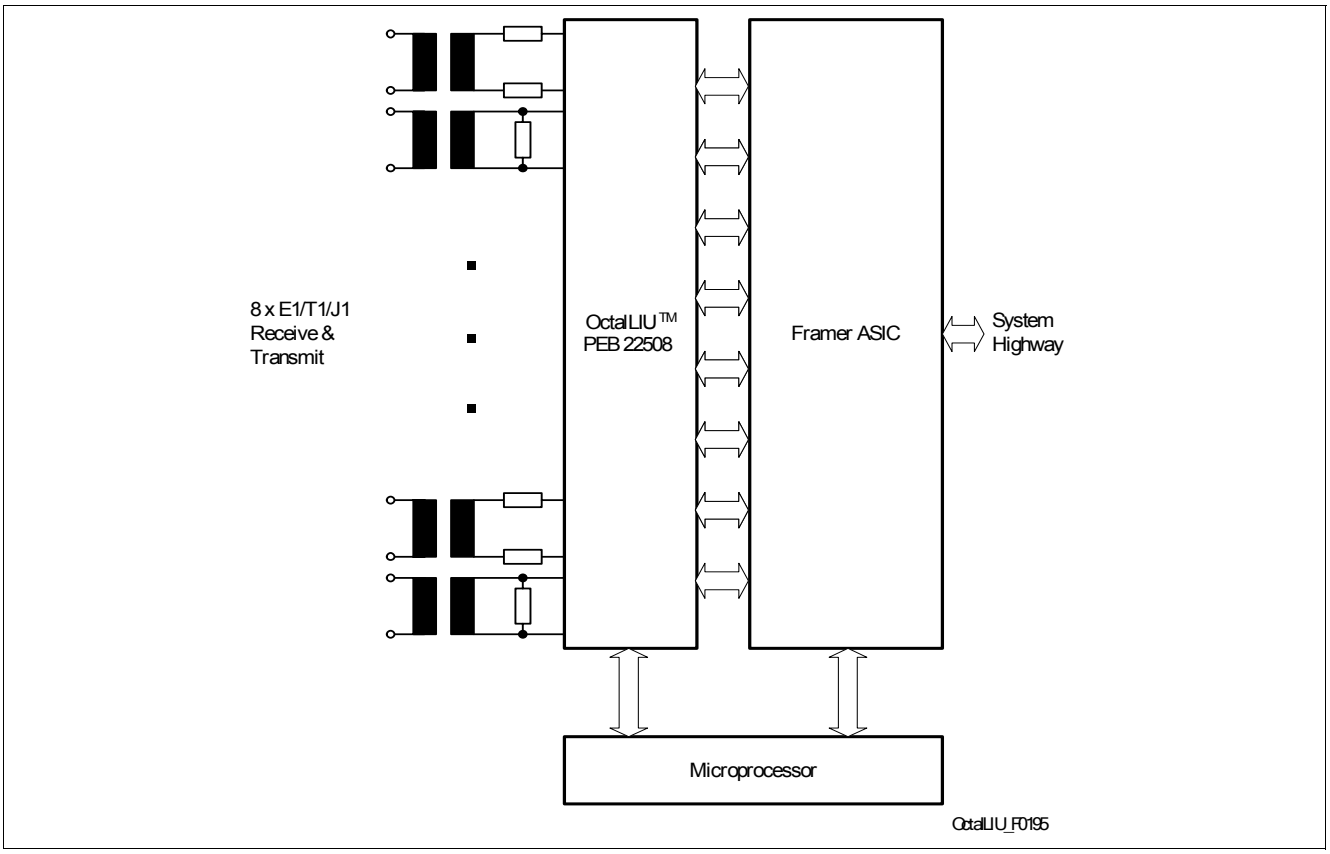


Figure 2 Typical Multiple Link Application

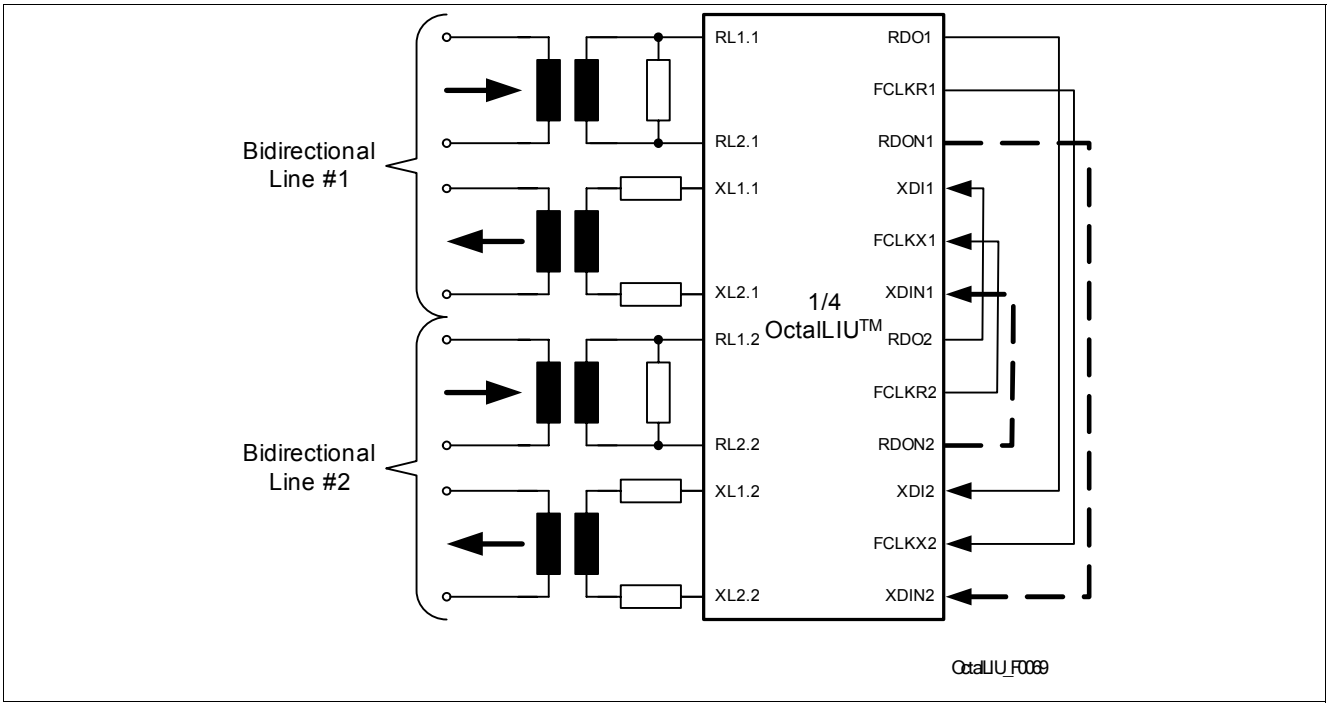


Figure 3 Typical Multiple Repeater Application between line #1 and Line #2

2 Pin Descriptions

In this chapter the function and placement of all pins are described.

2.1 Pin Diagram PG-LBGA-256 (top view)

Figure 4 shows the ball layout of the OctalLIU™.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
16	Reserved	XPB8	XPA8	FCLKX8	FCLKR8	RPA7	A0	RD	A3	A9	FCLKX6	FCLKR6	RPC5	FCLKR5	RPA5	Reserved
15	RL27	VSS	XDIP8	RPB8	XPB7	RDOP7	ALE	WR	A4	A8	RPC6	XPB5	RPB5	RDOP5	VSS	RL26
14	RLS7	VSS	XL37	XL17	XPA7	RPB7	READY	Reserved	A2	A7	XDIP6	XPA5	XL16	XL36	VSS	RLS6
13	RL17	VDDR7	XL47	XL27	RDOP8	FCLKR7	SYNC	BHE	A1	A6	RPB6	RPA6	XL26	XL46	VSS	RL16
12	VSS	VSS	VDDX7	VDDX7	RPA8	FCLKX7	SEC	CS	A5	A10	XPA6	FCLKX5	VDDX6	VDDX6	VDDR6	VSS
11	RL18	VDDR8	VSS	XL38	XL18	RPC8	VDDC	INT	VDDP	VDDP	XPB6	XDIP5	XL15	XL35	VDDR5	RL15
10	RL28	RLS8	VSS	XL48	XL28	RPC7	VSS	VSS	VSS	VSS	VDDC	RDOP6	XL25	XL45	TDO	RLS5
9	VSS	VSS	VDDX8	VDDX8	RPC2	XDIP7	VSS	VSS	VSS	VSS	VDDC	TDI	VDDX5	VDDX5	TCK	RL25
8	RL21	VSS	VDDX1	VDDX1	RPB2	FCLKX2	VSS	VSS	VSS	VSS	VDDC	TMS	VDDX4	VDDX4	VSS	VSS
7	RLS1	VDDR1	XL31	XL11	RPC1	XDIP2	VSS	VSS	VSS	VSS	XPA3	XL14	XL34	VSS	RLS4	RL24
6	RL11	IM1	XL41	XL21	RPA2	XPB2	VSS	VDDPLL	MCLK	VSS	RDOP3	XL24	XL44	TRSQ	VDDR4	RL14
5	VSS	VDDR2	VDDX2	VDDX2	XDIP1	XPA2	VDDP	VDDP	VDDP	VDDP	XDIP3	RPB4	VDDX3	VDDX3	DBW	VSS
4	RL12	IM0	XL32	XL12	RDOP2	D12	VDDC	VDDC	VDDC	FCLKR3	RPA3	RPA4	XL13	XL33	VDDR3	RL13
3	RLS2	RES	XL42	XL22	XPA1	D13	D9	D5	D3	D2	FCLKX3	RDOPP4	XL23	XL43	VSS	RLS3
2	RL22	VSS	RDOP1	RPB1	XPB1	D14	D10	D7	D4	D0	RPB3	XPB3	RPC4	XDIP4	VSS	RL23
1	Reserved	RPA1	FCLKR1	FCLKX1	FCLKR2	D15	D11	D8	D6	D1	RPC3	FCLKR4	FCLKX4	XPA4	XPB4	Reserved

Figure 4 Pin Configuration (Ball Layout) PG-LBGA-256

2.2 Pin Definitions and Functions

The following table describes all pins and their functions:

Table 1 I/O Signals

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
Operation Mode Selection and Device Initialization					
	B3	$\overline{\text{RES}}$	I	PU	**Hardware Reset** Active low
	B6	IM1	I	PU	**Interface Mode Selection** 00_B: Asynchronous Intel Bus Mode. 01_B: Asynchronous Motorola Bus Mode 10_B: SPI Bus Slave Mode. 11_B: SCI Bus Slave Mode
	B4	IM0	I	PU	
Asynchronous and Serial Micro Controller Interfaces					
	K12	A10	I	PU	**Address Bus Line 10 (MSB)**
	K16	A9	I	PU	**Address Bus Line 9**
	K15	A8	I	PU	**Address Bus Line 8**
	K14	A7	I	PU	**Address Bus Line 7**
	K13	A6	I	PU	**Address Bus Line 6**
	J12	A5	I	PU	**Address Bus Line 5**
		A5	I	PU	**SCI source address bit 5 (MSB)** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
	J15	A4	I	PU	**Address Bus Line 4**
		A4	I	PU	**SCI source address bit 4** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
	J16	A3	I	PU	**Address Bus Line 3**
		A3	I	PU	**SCI source address bit 3** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
	J14	A2	I	PU	**Address Bus Line 2**
		A2	I	PU	**SCI source address bit 2** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
	J13	A1	I	PU	**Address Bus Line 1**
		A1	I	PU	**SCI source address bit 1** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
	G16	A0	I	PU	**Address Bus Line 0**
		A0	I	PU	**SCI source address bit 0 (LSB)** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	1F	D15	IO	PU	**Data Bus Line 15**
		PLL10	I	PU	**PLL programming bit 10** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	2F	D14	IO	PU	**Data Bus Line 14**
		PLL9	I	PU	**PLL programming bit 9** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	F3	D13	IO	PU	**Data Bus Line 13**
		PLL8	I	PU	**PLL programming bit 8** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	F4	D12	IO	PU	**Data Bus Line 12**
		PLL7	I	PU	**PLL programming bit 7** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	G1	D11	IO	PU	**Data Bus Line 11**
		PLL6	I	PU	**PLL programming bit 6** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	G2	D10	IO	PU	**Data Bus Line 10**
		PLL5	I	PU	**PLL programming bit 5** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	G3	D9	IO	PU	**Data Bus Line 9**
		PLL4	I	PU	**PLL programming bit 4** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	H1	D8	IO	PU	**Data Bus Line 8**
		PLL3	I	PU	**PLL programming bit 3** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	H2	D7	IO	PU	**Data Bus Line 7**
		PLL2	I	PU	**PLL programming bit 2** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	J1	D6	IO	PU	**Data Bus Line 6**
		PLL1	I	PU	**PLL programming bit 1** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	H3	D5	IO	PU	**Data Bus Line 5**
		PLL0	I	PU	**PLL programming bit 0** Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´.
	J2	D4	IO	PU	**Data Bus Line 4**

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	J3	D3	IO	PU	**Data Bus Line 3**
	K3	D2	IO	PU	**Data Bus Line 2**
		SCI_CLK	I	–	**SCI Bus Clock** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
		SCLK	I	–	**SPI Bus Clock** Only used if SPI interface mode is selected by IM(1:0) = ´10b´.
	K1	D1	IO	PU	**Data Bus Line 1**
		SCI_RXD	I	PU	**SCI Bus Serial Data In** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
		SDI	I	PU	**SPI Serial Data In** Only used if SPI interface mode is selected by IM(1:0) = ´10b´.
	K2	D0	IO	PU	**Data Bus Line 0**
		SCI_TXD	I	PP or oD	**SCI Bus Serial Data Out** Only used if SCI interface mode is selected by IM(1:0) = ´11b´.
		SDO	I	PU	**SPI Bus Serial Data Out** Only used if SPI interface mode is selected by IM(1:0) = ´10b´.
	G15	ALE	I	PU	**Address Latch Enable** A high on this line indicates an address on an external multiplexed address/data bus. The address information provided on lines A(10:0) is internally latched with the falling edge of ALE. This function allows the OctalLIU™ to be connected to a multiplexed address/data bus without the need for external latches. In this case, pins A(7:0) must be connected to the data bus pins externally. In case of demultiplexed mode this pin can be connected directly to VDD or can be left open.
	H16	$\overline{RD}$	I	PU	**Read Enable** Intel bus mode. This signal indicates a read operation. When the OctalLIU™ is selected via CS, the RD signal enables the bus drivers to output data from an internal register addressed by A(10:0) to the Data Bus.
		$\overline{DS}$	I	PU	**Data Strobe** Motorola bus mode. This pin serves as input to control read/write operations.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	H15	$\overline{WR}$	I	PU	**Write Enable** Intel bus mode. This signal indicates a write operation. When CS is active the OctalLIU™ loads an internal register with data provided on the data bus.
		$\overline{RW}$	I	PU	**Read/Write Select** Motorola bus mode. This signal distinguishes between read and write operation.
	R5	DBW	I	PU	**Data Bus Width select** Bus interface mode A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Byte transfers are implemented by using A0 and $\overline{BHE}$/$\overline{BLE}$.
	H13	$\overline{BHE}$	I	PU	**Bus High Enable** Intel bus mode. If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte of the data bus D(15:8). In 8-bit bus interface mode this signal has no function and should be tied to VDD or left open.
		$\overline{BLE}$	I	PU	**Bus Low Enable** Motorola bus mode. If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte of the data bus D(7:0). In 8-bit bus interface mode this signal has no function and should be tied to VDD or left open.
	H12	$\overline{CS}$	I	PU	**Chip Select** Low active chip select.
	H11	INT	O	–	**Interrupt Request** Interrupt request. INT serves as general interrupt request for all interrupt sources. These interrupt sources can be masked via registers IMR(7:0). Interrupt status is reported via registers GIS (Global Interrupt Status) and ISR(7:0). Output characteristics (push-pull active low/high, open drain) are determined by programming register IPC.
	G14	$\overline{READY}$	O	–	**Data Ready** Only if Intel bus mode is selected. Asynchronous handshake signal to indicate successful read or write cycle.
		$\overline{DTACK}$	O	–	**Data Acknowledge** Only if Motorola bus mode is selected. Asynchronous handshake signal to indicate successful read or write cycle.
Line Interface Receiver					

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	A6	RL1.1	I (analog)	–	**Line Receiver input 1, port 1** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		ROID1	I	–	**Receive Optical Interface Data, port 1** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´01_b´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.
	A8	RL2.1	I (analog)	–	**Line Receiver input 2, port 1** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
	A7	RLS21	IO (analog)	–	**Receive Line Switch, port 1** Connector of the analog switch.
	A4	RL1.2	I (analog)	–	**Line Receiver input 1, port 2** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		ROID2	I	–	**Receive Optical Interface Data, port 2** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´01_b´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.
	A2	RL2.2	I (analog)	–	**Line Receiver input 2, port 2** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
	A3	RLS22	IO (analog)	–	**Receive Line Switch, port 2** Connector of the analog switch.
	T4	RL1.3	I (analog)	–	**Line Receiver input 1, port 3** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		ROID3	I	–	**Receive Optical Interface Data, port 3** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´01_b´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.
	T2	RL2.3	I (analog)	–	**Line Receiver input 2, port 3** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
	T3	RLS23	IO (analog)	–	**Receive Line Switch, port 3** Connector of the analog switch.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	T6	RL1.4	I (analog)	–	**Line Receiver input 1, port 4** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		ROID4	I	–	**Receive Optical Interface Data, port 4** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´01_b´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.
	T7	RL2.4	I (analog)	–	**Line Receiver input 2, port 4** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
	R7	RLS24	IO (analog)	–	**Receive Line Switch, port 4** Connector of the analog switch.
	T11	RL1.5	I (analog)	–	**Line Receiver input 1, port 5** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		ROID5	I	–	**Receive Optical Interface Data, port 5** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´01_b´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.
	T9	RL2.5	I (analog)	–	**Line Receiver input 2, port 5** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
	T10	RLS25	IO (analog)	–	**Receive Line Switch, port 5** Connector of the analog switch.
	T13	RL1.6	I (analog)	–	**Line Receiver input 1, port 6** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		ROID6	I	–	**Receive Optical Interface Data, port 6** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´01_b´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.
	T15	RL2.6	I (analog)	–	**Line Receiver input 2, port 6** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
	T14	RLS26	IO (analog)	–	**Receive Line Switch, port 6** Connector of the analog switch.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	A13	RL1.7	I (analog)	–	**Line Receiver input 1, port 7** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		ROID7	I	–	**Receive Optical Interface Data, port 7** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´01_b´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.
	A15	RL2.7	I (analog)	–	**Line Receiver input 2, port 7** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
	A14	RLS27	IO (analog)	–	**Receive Line Switch, port 7** Connector of the analog switch.
	A11	RL1.8	I (analog)	–	**Line Receiver input 1, port 8** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
		ROID8	I	–	**Receive Optical Interface Data, port 8** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´01_b´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required.
	A10	RL2.8	I (analog)	–	**Line Receiver input 2, port 8** Analog input from the external transformer. Selected if LIM1.DRS is cleared.
	B10	RLS28	IO (analog)	–	**Receive Line Switch, port 8** Connector of the analog switch.
Line Interface Transmitter					
	D7	XL1.1	O (analog)	–	**Transmit Line 1, port 1** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
		XOID1	O	–	**Transmit Optical Interface Data, port 1** Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK2 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and MR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
	D6	XL2.1	O (analog)	–	**Transmit Line 2, port 1** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	C7	XL3.1	I (analog)	–	**Transmit Line 3, port 1** Analog transmit input 1.
	C6	XL4.1	I (analog)	–	**Transmit Line 4, port 1** Analog transmit input 2.
	D4	XL1.2	O (analog)	–	**Transmit Line 1, port 2** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
		XOID2	O	–	**Transmit Optical Interface Data, port 2** Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK2 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and MR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
	D3	XL2.2	O (analog)	–	**Transmit Line 2, port 2** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
	C4	XL3.2	I (analog)	–	**Transmit Line 3, port 2** Analog transmit input 1.
	C3	XL4.2	I (analog)	–	**Transmit Line 4, port 2** Analog transmit input 2.
	N4	XL1.3	O (analog)	–	**Transmit Line 1, port 3** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
		XOID3	O	–	**Transmit Optical Interface Data, port 3** Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK3 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and MR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	N3	XL2.3	O (analog)	–	**Transmit Line 2, port 3** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
		XFM3	O	–	**Transmit Frame Marker, port 3** This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = 1 and MR0.XC1 = 0). Data is clocked on positive transitions of XCLK3. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. In remote loop configuration the XFM3 marker is not valid.
	P4	XL3.3	I (analog)	–	**Transmit Line 3, port 3** Analog transmit input 1.
	P3	XL4.3	I (analog)	–	**Transmit Line 4, port 3** Analog transmit input 2.
	M7	XL1.4	O (analog)	–	**Transmit Line 1, port 4** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
		XOID4	O	–	**Transmit Optical Interface Data, port 4** Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK4 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and MR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
	M6	XL2.4	O (analog)	–	**Transmit Line 2, port 4** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
	N7	XL3.4	I (analog)	–	**Transmit Line 3, port 4** Analog transmit input 1.
	N6	XL4.4	I (analog)	–	**Transmit Line 4, port 4** Analog transmit input 2.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	N11	XL1.5	O (analog)	–	**Transmit Line 1, port 5** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
		XOID5	O	–	**Transmit Optical Interface Data, port 5** Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK5 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and MR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
	N10	XL2.5	O (analog)	–	**Transmit Line 2, port 5** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
	P11	XL3.5	I (analog)	–	**Transmit Line 3, port 5** Analog transmit input 1.
	P10	XL4.5	I (analog)	–	**Transmit Line 4, port 5** Analog transmit input 2.
	N14	XL1.6	O (analog)	–	**Transmit Line 1, port 6** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
		XOID6	O	–	**Transmit Optical Interface Data, port 6** . Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK6 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and MR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
	N13	XL2.6	O (analog)	–	**Transmit Line 2, port 6** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
	P14	XL3.6	I (analog)	–	**Transmit Line 3, port 6** Analog transmit input 1.
	P13	XL4.6	I (analog)	–	**Transmit Line 4, port 6** Analog transmit input 2.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	D14	XL1.7	O (analog)	–	**Transmit Line 1, port 7** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
		XOID7	O	–	**Transmit Optical Interface Data, port 7** Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK7 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and MR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
	D13	XL2.7	O (analog)	–	**Transmit Line 2, port 7** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
	C14	XL3.7	I (analog)	–	**Transmit Line 3, port 7** Analog transmit input 1.
	C13	XL4.7	I (analog)	–	**Transmit Line 4, port 7** Analog transmit input 2.
	E11	XL1.8	O (analog)	–	**Transmit Line 1, port 8** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
		XOID8	O	–	**Transmit Optical Interface Data, port 8** Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK8 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and MR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared.
	E10	XL2.8	O (analog)	–	**Transmit Line 2, port 8** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared.
	D11	XL3.8	I (analog)	–	**Transmit Line 3, port 8** Analog transmit input 1.
	D10	XL4.8	I (analog)	–	**Transmit Line 4, port 8** Analog transmit input 2.
Clock Signals					

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	J6	MCLK	I	–	**Master Clock** A reference clock of better than ±32 ppm accuracy in the range of 1.02 to 20 MHz must be provided on this pin. The OctalLIU™ internally derives all necessary clocks from this master (see registers GCM(6:1)).
	G13	SYNC	I	PU	**Clock Synchronization of DCO-R** If a clock is detected on pin SYNC the DCO-R circuitry of the OctalLIU™ synchronizes to this 1.544/2.048 MHz clock (see LIM0.MAS, CMR1.DCS and CMR2.DCF). Additionally, in master mode the OctalLIU™ is able to synchronize to an 8 kHz reference clock (IPC.SSYF = ´1´). If not connected, an internal pull-up transistor ensures high input level.
	G12	FSC	O	–	**8 kHz Frame Synchronization** The optionally synchronization pulse is active high or low for one 2.048/1.544 MHz cycle (pulse width = 488 ns for E1and 648 ns or T1/J1).
Digital (Framer) Interface Receive					
	C2	RDO1	O	–	**Receive Data Out, port 1** Received data at RL1, RL2 is sent to RDOP, RDON. Clocking of data is done with the rising or falling edge of RCLK.
	C1	FCLKR1	I/O	PU	**Framer Data Clock Receive, port 1** Input if PC5.CSRP = ´0´, output if PC5.CSRP = ´1´.
	E4	RDO2	O	–	**Receive Data Out, port 2** See description of RDOP1.
	E1	FCLKR2	I/O	PU	**Framer Data Clock Receive, port 2** See description of FCLKR1.
	L6	RDO3	O	–	**Receive Data Out, port 3** See description of RDOP1.
	K4	FCLKR3	I/O	PU	**Framer Data Clock Receive, port 3** See description of FCLKR1.
	M3	RDO4	O	–	**Receive Data Out, port 4** See description of RDOP1.
	M1	FCLKR4	I/O	PU	**Framer Data Clock Receive, port 4** See description of FCLKR1.
	P15	RDO5	O	–	**Receive Data Out, port 5** See description of RDOP1.
	P16	FCLKR5	I/O	PU	**Framer Data Clock Receive, port 5** See description of FCLKR1.
	M10	RDO6	O	–	**Receive Data Out, port 6** See description of RDOP1.
	M16	FCLKR6	I/O	PU	**Framer Data Clock Receive, port 6** See description of FCLKR1.
	F15	RDO7	O	–	**Receive Data Out, port 7** See description of RDOP1.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	F13	FCLKR7	I/O	PU	**Framer Data Clock Receive, port 7** See description of FCLKR1.
	E13	RDO8	O	–	**Receive Data Out, port 8** See description of RDOP1.
	E16	FCLKR8	I/O	PU	**Framer Data Clock Receive, port 8** See description of FCLKR1.
Digital (Framer) Interface Transmit					
	E5	XDI1	I	–	**Transmit Data In, port 1** NRZ transmit data received from the framer. Latching of data is done with rising or falling transitions of FCLKX1 according to bit DIC3.RESX.
	D1	FCLKX1	I/O	–	**Framer Data Clock Transmit, port 1**
	F7	XDI2	I	–	**Transmit Data In, port 2** See description of XDI1.
	F8	FCLKX2	I/O	–	**Framer Data Clock Transmit, port 2** See description of FCLKX1.
	L5	XDI3	I	–	**Transmit Data In, port 3** See description of XDI1.
	L3	FCLKX3	I/O	–	**Framer Data Clock Transmit, port 3** See description of FCLKX1.
	P2	XDI4	I	–	**Transmit Data In, port 4** See description of XDI1.
	N1	FCLKX4	I/O	–	**Framer Data Clock Transmit, port 4** See description of FCLKX1.
	M11	XDI5	I	–	**Transmit Data In, port 5** See description of XDI1.
	M12	FCLKX5	I/O	–	**Framer Data Clock Transmit, port 5** See description of FCLKX1.
	L14	XDI6	I	–	**Transmit Data In, port 6** See description of XDI1.
	L16	FCLKX6	I/O	–	**Framer Data Clock Transmit, port 6** See description of FCLKX1.
	F9	XDI7	I	–	**Transmit Data In, port 7** See description of XDI1.
	F12	FCLKX7	I/O	–	**Framer Data Clock Transmit, port 7** See description of FCLKX1.
	C15	XDI8	I	–	**Transmit Data In, port 8** See description of XDI1.
	D16	FCLKX8	I/O	–	**Framer Data Clock Transmit, port 8** See description of FCLKX1.
Multi Function Pins					

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	B1	RPA1	I/O	PU/–	**Receive Multifunction Pins A to C, port 1** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESR latching/transmission of data is done with the rising or falling edge of FCLKR. If not connected, an internal pull-up transistor ensures a high input level. An input function must not be selected twice or more. Selectable pin functions are described below.
	D2	RPB1	I/O	PU/–	
	E7	RPC1	I/O	PU/–	
	B1	RPA1	I	PU	**Receive Line Termination (RLT), port 1** PC(1:3).RPC(3:0) = ´1000_b´. These input function controls together with LIM0.RTRS the analog switch of the receive line interface: A logical equivalence is build out of LIM0.RTRS and RLT.
	D2	RPB1	I	PU	
	E7	RPC1	I	PU	
	B1	RPA1	I	PU	**General Purpose Input (GPI), port 1** PC(1:3).RPC(3:0) = ´1001_b. The pin is set to input. The state of this input is reflected in the register bits MFPI.RPA, MFPI.RPB or MFPI.RPC respectively.
	D2	RPB1			
	E7	RPC1			
	B1	RPA1	O	–	**General Purpose Output High (GPOH), port 1** PC(1:3).RPC(3:0) = ´1010_b´. The pin level is set fix to high level.
	D2	RPB1			
	E7	RPC1			
	B1	RPA1	O	–	**General Purpose Output Low (GPOL), port 1** PC(1:3).RPC(3:0) = ´1011_b´. The pin level is set fix to low level.
	D2	RPB1			
	E7	RPC1			
	B1	RPA1	O	–	**Loss of Signal Indication Output (LOS), port 1** PC(1:3).RPC(3:0) = ´1100_b. The output reflects the Loss of Signal status as readable in LSR0.LOS.
	D2	RPB1			
	E7	RPC1			
	B1	RPA1	O	–	**Receive Data Output Negative (RDON), port 1** PC(1:3).RPC(3:0) = ´1110_b´. Receive data output negative for dual rail mode on digital (framer) interface (LIM3.DRR = ´1´). Bipolar violation output for single rail mode on digital (framer) interface (LIM3.DRR = ´0´).
	D2	RPB1			
	E7	RPC1			
	B1	RPA1	O	–	**Receive Clock Output (RCLK), port 1** PC(1:3).RPC(3:0) = ´1111_b´. Default setting after reset Receive clock output RCLK. After reset RCLK is configured to be internally pulled up weekly. By setting of PC5.CRP RCLK is an active output. RCLK source and frequency selection is made by CMR1.RS(1:0) if COMP = ´1´ or by CMR4.RS(2:0) if COMP = ´0´.
	D2	RPB1			
	E7	RPC1			

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	E6	RPA2	I/O	PU/–	**Receive Multifunction Pins A to C, port 2** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESR latching/transmission of data is done with the rising or falling edge of FCLKR. If not connected, an internal pull-up transistor ensures a high input level. An input function must not be selected twice or more. Selectable pin functions as described for port 1.
	E8	RPB2			
	E9	RPC2			
	L4	RPA3	I/O	PU/–	**Receive Multifunction Pins A to C, port 3** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESR latching/transmission of data is done with the rising or falling edge of FCLKR. If not connected, an internal pull-up transistor ensures a high input level. An input function must not be selected twice or more. Selectable pin functions as described for port 1.
	L2	RPB3			
	L1	RPC3			
	M4	RPA4	I/O	PU/–	**Receive Multifunction Pins A to C, port 4** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESR latching/transmission of data is done with the rising or falling edge of FCLKR. If not connected, an internal pull-up transistor ensures a high input level. An input function must not be selected twice or more. Selectable pin functions as described for port 1.
	M5	RPB4			
	N2	RPC4			

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	R16	RPA5	I/O	PU/–	**Receive Multifunction Pins A to C, port 5** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESR latching/transmission of data is done with the rising or falling edge of FCLKR. If not connected, an internal pull-up transistor ensures a high input level. An input function must not be selected twice or more. Selectable pin functions as described for port 1.
	N15	RPB5			
	N16	RPC5			
	M13	RPA6	I/O	PU/–	**Receive Multifunction Pins A to C, port 6** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESR latching/transmission of data is done with the rising or falling edge of FCLKR. If not connected, an internal pull-up transistor ensures a high input level. An input function must not be selected twice or more. Selectable pin functions as described for port 1.
	L13	RPB6			
	L15	RPC6			
	F16	RPA7	I/O	PU/–	**Receive Multifunction Pins A to C, port 7** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESR latching/transmission of data is done with the rising or falling edge of FCLKR. If not connected, an internal pull-up transistor ensures a high input level. An input function must not be selected twice or more. Selectable pin functions as described for port 1.
	F14	RPB7			
	F10	RPC7			

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	E12	RPA8	I/O	PU/–	**Receive Multifunction Pins A to C, port 8** Depending on programming of bits PC(1:3).RPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESR latching/transmission of data is done with the rising or falling edge of FCLKR. If not connected, an internal pull-up transistor ensures a high input level. An input function must not be selected twice or more. Selectable pin functions as described for port 1.
	D15	RPB8			
	F11	RPC8			
	E3	XPA1	I/O	PU/–	**Transmit Multifunction Pins A and B, port 1** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESX latching/transmission of data is done with the rising or falling edge of FCLKX. If not connected, an internal pull-up transistor ensures a high input level. Each input function (TCLK, XDIN, XLT or $\overline{XLT}$) may only be selected once. Selectable pin functions are described below.
	E2	XPB1	I/O	PU/–	
	E3	XPA1	I	PU	**Transmit Clock (TCLK), port 1** PC(1:2).XPC(3:0) = ´0011_b´ A 2.048/8.192 MHz (E1) or 1.544/6.176 MHz (T1/J1) clock has to be sourced by the framer if the internally generated transmit clock (generated by DCO-X) shall not be used. Optionally this input is used as a synchronization clock for the DCO-X circuitry with a frequency of 2.048 (E1) or 1.544 MHz (T1/J1).
	E2	XPB1	I	PU	
	E3	XPA1	O	–	**Transmit Clock (XCLK), port 1** PC(1:2).XPC(3:0) = ´0111_b´ Transmit line clock of 2.048 MHz (E1) or 1.544 MHz (T1/J1) derived from FCLKX/R, RCLK or generated internally by DCO circuitries.
	E2	XPB1	O	–	
	E3	XPA1	I	PU	**Transmit Line Tristate (XLT), port 1** PC(1:2).XPC(3:0) = ´1000_b´ A high level on this port sets the transmit lines XL1/2 or XDOP/N into tristate mode. This pin function is logically OR´d with register bit XPM2.XLT.
	E2	XPB1	I	PU	

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	E3	XPA1	I	PU	**General Purpose Input (GPI), port 1** PC(1:2).XPC(3:0) = ´1001_b. The pin is set to input. The state of this input is reflected in the register bits MFPI.XPA, MFPI.XPB or MFPI.XPC respectively.
	E2	XPB1	I	PU	
	E3	XPA1	O	–	**General Purpose Output High (GPOH), port 1** PC(1:2).XPC(3:0) = ´1010_b´. The pin level is set fix to high level.
	E2	XPB1	O	–	
	E3	XPA1	O	–	**General Purpose Output Low (GPOL), port 1** PC(1:2).XPC(3:0) = ´1011_b´. The pin level is set fix to high level.
	E2	XPB1	O	–	
	E3	XPA1	I	PU	**Transmit Data Input Negative (XDIN), port 1** PC(1:2).XPC(3:0) = ´1101_b. Transmit data input negative for dual rail mode on framer side (LIM3.DRX = ´1´). Depending on bit DIC3.RESX latching of data is done with the rising or falling edge of FCLKX.
	E2	XPB1	I	PU	
	E3	XPA1	I	PU	**Transmit Line Tristate, low active, port 1** $\overline{\text{XLT}}$: PC(1:2).XPC(3:0) = ´1110_b´. A low level on this port sets the transmit lines XL1/2 or XDOP/N into tristate mode. This pin function is logically OR´d with register bit XPM2.XLT.
	E2	XPB1	I	PU	
	F5 F6	XPA2 XPB2	I/O	PU/–	**Transmit Multifunction Pins A and B, port 2** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESX latching/transmission of data is done with the rising or falling edge of FCLKX. If not connected, an internal pull-up transistor ensures a high input level. Each input function (TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. Selectable pin functions as described for port 1.
	L7 M2	XPA3 XPB3	I/O	PU/–	**Transmit Multifunction Pins A and B, port 3** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESX latching/transmission of data is done with the rising or falling edge of FCLKX. If not connected, an internal pull-up transistor ensures a high input level. Each input function (TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. Selectable pin functions as described for port 1.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	P1 R1	XPA4 XPB4	I/O	PU/–	**Transmit Multifunction Pins A and B, port 4** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESX latching/transmission of data is done with the rising or falling edge of FCLKX. If not connected, an internal pull-up transistor ensures a high input level. Each input function (TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. Selectable pin functions as described for port 1.
	M14 M15	XPA5 XPB5	I/O	PU/–	**Transmit Multifunction Pins A and B, port 5** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESX latching/transmission of data is done with the rising or falling edge of FCLKX. If not connected, an internal pull-up transistor ensures a high input level. Each input function (TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. Selectable pin functions as described for port 1.
	L12 L11	XPA6 XPB6	I/O	PU/–	**Transmit Multifunction Pins A and B, port 6** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESX latching/transmission of data is done with the rising or falling edge of FCLKX. If not connected, an internal pull-up transistor ensures a high input level. Each input function (TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. Selectable pin functions as described for port 1.

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	E14 E15	XPA7 XPB7	I/O	PU/–	**Transmit Multifunction Pins A and B, port 7** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESX latching/transmission of data is done with the rising or falling edge of FCLKX. If not connected, an internal pull-up transistor ensures a high input level. Each input function (TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. Selectable pin functions as described for port 1.
4 4	C16 B16	XPA8 XPB8	I/O	PU/–	**Transmit Multifunction Pins A and B, port 8** Depending on programming of bits PC(1:2).XPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the OctalLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESX latching/transmission of data is done with the rising or falling edge of FCLKX. If not connected, an internal pull-up transistor ensures a high input level. Each input function (TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once. Selectable pin functions as described for port 1.
Power Supply					
	7B	V_{DDR1}	S	–	**Positive Power Supply** For the analog receiver 1 (3.3 V)
	5B	V_{DDR2}	S	–	**Positive Power Supply** For the analog receiver 2 (3.3 V)
	4R	V_{DDR3}	S	–	**Positive Power Supply** For the analog receiver 3 (3.3 V)
	6R	V_{DDR4}	S	–	**Positive Power Supply** For the analog receiver 4 (3.3 V)
	11R	V_{DDR5}	S	–	**Positive Power Supply** For the analog receiver 5 (3.3 V)
	12R	V_{DDR6}	S	–	**Positive Power Supply** For the analog receiver 6 (3.3 V)
	13B	V_{DDR7}	S	–	**Positive Power Supply** For the analog receiver 7 (3.3 V)
	11B	V_{DDR8}	S	–	**Positive Power Supply** For the analog receiver 8 (3.3 V)
	8C 8D	V_{DDX1}	S	–	**Positive Power Supply** For the analog transmitter 1

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	5C	V_{DDX2}	S	–	**Positive Power Supply** For the analog transmitter 2
	5D				
	5N	V_{DDX3}	S	–	**Positive Power Supply** For the analog transmitter 3
	5P				
	8N	V_{DDX4}	S	–	**Positive Power Supply** For the analog transmitter 4
	8P				
	9N	V_{DDX5}	S	–	**Positive Power Supply** For the analog transmitter 5
	9P				
	12N	V_{DDX6}	S	–	**Positive Power Supply** For the analog transmitter 6
	12P				
	12C	V_{DDX7}	S	–	**Positive Power Supply** For the analog transmitter 7
	12D				
	9C	V_{DDX8}	S	–	**Positive Power Supply** For the analog transmitter 8
	9D				
	4G	V_{DDC}	S	–	**Positive Power Supply** For the digital core (1.8 V)
	11G				
	4H				
	4J				
	8L				
	9L				
	10L				
	6H	V_{DDPLL}	S	–	**Positive Power Supply** For the analog PLL
	5G	V_{DDP}	S	–	**Positive Power Supply** For the digital pads(3.3 V) For correct operation, all V_{DD} pins have to be connected to positive power supply.
	5H				
	5J				
	5K				
	11J				
	11K				

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	5A	V_{SS}	S	–	**Power Ground** Common for all sub circuits (0 V) For correct operation, all V_{SS} pins have to be connected to ground.
	9A				
	12A				
	2B				
	8B				
	9B				
	12B				
	14B				
	15B				
	10C				
	11C				
	6G				
	7G				
	8G				
	9G				
	10G				
	7H				
	8H				
	9H				
	10H				
	7J				
	8J				
	9J				
	10J				
	6K				
	7K				
	8K				
	9K				
	10K				
	7P				
	2R				
	3R				
	8R				
	13R				
	14R				
	15R				
	5T				
	8T				
	12T				
Boundary Scan/Joint Test Access Group (JTAG)					

Table 1 I/O Signals (cont'd)

Pin No.	Ball No.	Name	Pin Type	Buffer Type	Function
	P6	$\overline{\text{TRS}}$	I	PD	**Test Reset** For Boundary Scan (active low). If not connected, an internal pull-up transistor ensures high input level. If the JTAG boundary scan is not used, this pin must be connected to $\overline{\text{RES}}$ or V_{SS}.
	M9	TDI		PU	**Test Data Input** For Boundary Scan. If not connected an internal pull-up transistor ensures high input level.
	M8	TMS			**Test Mode Select** For Boundary Scan. If not connected an internal pull-up transistor ensures high input level.
	R9	TCK			**Test Clock** For Boundary Scan. If not connected an internal pull-up transistor ensures high input level.
	R10	TDO	O	–	**Test Data Output** For Boundary Scan

Note: oD = open drain output PU = input or input/output comprising an internal pull-up device To override the internal pull-up by an external pull-down, a resistor value of 22 kΩ is recommended. The pull-up devices are activated during reset, this means their state is undefined until the reset signal has been applied. Unused pins containing pull-ups can be left open.

2.3 Pin Strapping

Some pins are used for selection of functional modes of the OctalLIU™:

Table 2 Overview about the Pin Strapping

PIN	Pin Strapping is used	Pin Strapping Function
IM(1:0)	Always	Defines the used micro controller interface
A(5:0)	Only in SCI interface mode	Defines the six Lisps of the SCI source address, see **Chapter 3.5.2.1**
D(15:5)	Only in SCI or SPI interface mode	Programs the parameters N and M of the PLL in the master clocking unit instead of registers GCM5 and GCM6, see **Chapter 3.5.5**: - D(15:11) values programs PLL dividing factor M - D(10:5) values programs PLL dividing factor N Programming by pin strapping is equivalent to programming by register bits GCM5.PLL_M(4:0) and GCM6.PLL_N(5:0) which is used in asynchronous micro controller modes.

3 Functional Description

3.1 Hardware

The OctalLIU™ always requires two supply voltages, 1.8 V and 3.3 V.

3.2 Software

The OctalLIU™ device contains analog and digital function blocks that are configured and controlled by an external microprocessor or micro controller, using either the asynchronous interface, SPI bus or SCI bus.

The register address range is 11 bit wide.

3.3 Functional Overview

The main interfaces are

- Receive and transmit line interface
- Asynchronous Microprocessor interface with two modes: Intel or Motorola
- SPI Bus interface
- SCI Bus interface
- Framer interface
- Boundary scan interface

As well as several control lines for reset, mode and clocking purpose.

The main internal functional blocks are

- Analog line receiver with equalizer network and clock/data recovery
- Analog line driver with programmable pulse shaper and line build out
- Master clock generation unit
- Dual elastic buffers for receive and transmit direction, controlled by the appropriate jitter attenuators
- Receive line decoding, alarm detection and PRBS monitoring
- Transmit line encoding, alarm and PRBS generation
- Receive jitter attenuator
- Transmit jitter attenuator
- Available test loops: Local loop, remote loop and payload loop
- Boundary scan control

3.4 Block Diagram

Figure 5 shows the block diagram of the OctalLIU™.

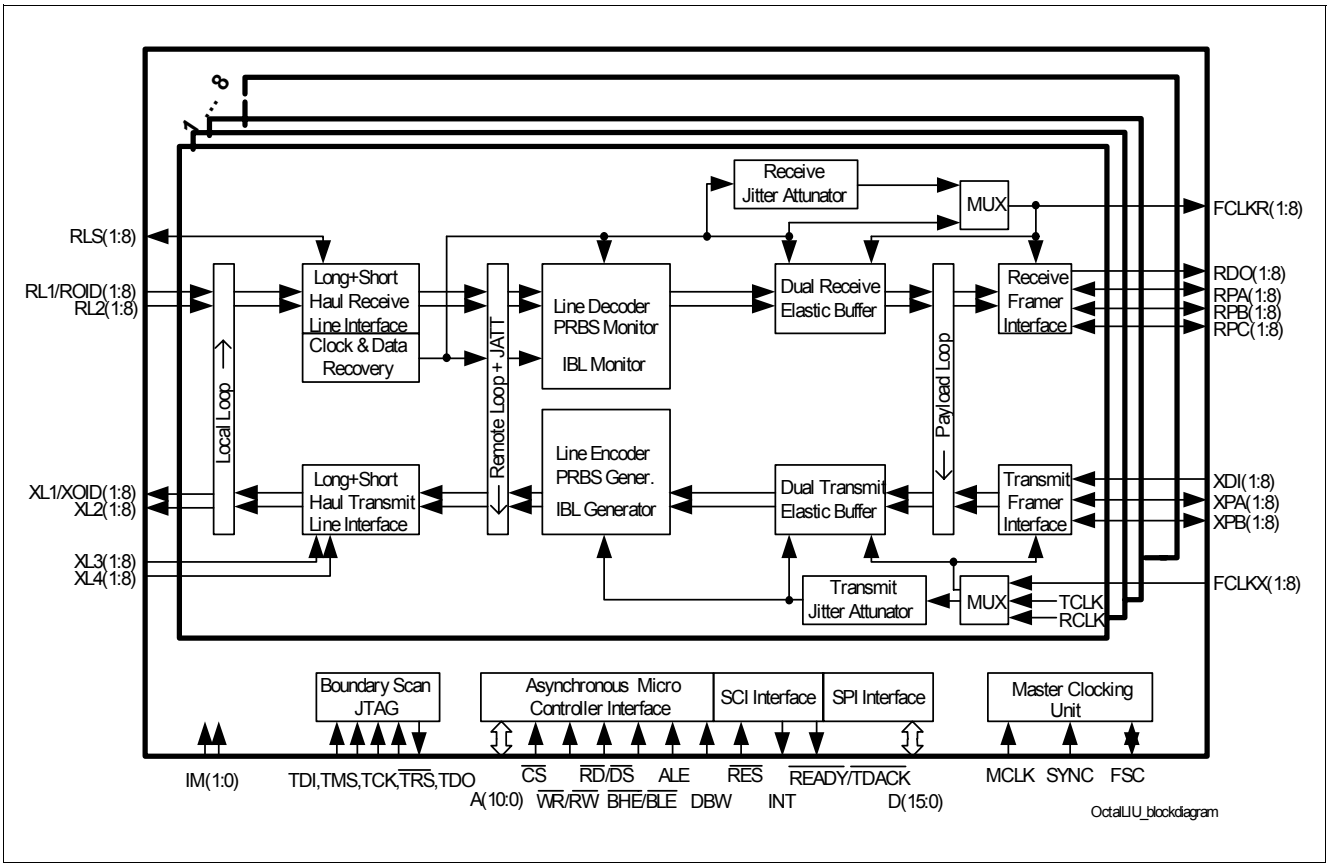


Figure 5 Block Diagram

3.5 Functional Blocks

The four possible micro controller interface modes - two asynchronous modes (Intel, Motorola) and two serial interface modes (SPI bus or SCI bus) - are selected by using the interface mode selection pins IM(1:0). This selection is valid immediately after reset becomes inactive.

After changing of the interface mode by IM(1:0), a hardware reset must be applied.

3.5.1 Asynchronous Micro Controller Interface (Intel or Motorola mode)

The asychronous micro controller interface is selected if IM(1:0) is strapped to ´00B´ (Intel mode) or ´01B´ (Motorola mode).

An handshake signal (data acknowledge $\overline{\text{DTACK}}$ for Motorola- and READY for Intel-mode) is provided indicating successful read or write cycle. By using $\overline{\text{DTACK}}$ or READY respectively no counter is necessary in the micro controller to finish the access, see also timing diagrams **Figure 43** ff.

The generation of READY is asynchronous:

In Intel mode read access READY will be set to low by the OctalLIU™ after the data output is stable at the OctalLIU™. After the rising edge of RD (which is driven by the micro controller), READY is low for a “hold time”, before it will be set to high by the OctalLIU™.

In the Intel mode write access READY will be set to low by the OctalLIU™ after the falling edge of WR (which is driven by the micro controller). After WR is high and data are written successfully into the registers of the OctalLIU™, READY will be set to high by the OctalLIU™.

The general timing diagrams are shown in **Figure 43** to **Figure 48**.

The communication between the external micro controller and the OctalLIU™ is done using a set of directly accessible registers. The interface can be configured as Intel or Motorola type with a selectable data bus width of 8 or 16 bits.

The external micro controller transfers data to and from the OctalLIU™, sets the operating modes, controls function sequences, and gets status information by writing or reading control and status registers. All accesses can be done as byte or word accesses if enabled. If 16-bit bus width is selected, access to lower/upper part of the data bus is determined by address line A0 and signal BHE / $\overline{\text{BLE}}$ as shown in **Table 3** and **Table 4**.

Table 5 shows how the ALE (**A**ddress **L**atch **E**nable) line is used to control the bus structure and interface type. The switching of ALE allows the OctalLIU™ to be directly connected to a multiplexed address/data bus.

3.5.1.1 Mixed Byte/Word Access

Reading from or writing to the internal registers can be done using a 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. Randomly mixed byte/word access is allowed without any restrictions.

Table 3 Data Bus Access (16-Bit Intel Mode)

$\overline{\text{BHE}}$	A0	Register Access	OctalLIU™ Data Pins Used
0	0	Register word access (even addresses)	D(15:0)
0	1	Register byte access (odd addresses)	D(15:8)
1	0	Register byte access (even addresses)	D(7:0)
1	1	No transfer performed	None

Table 4 Data Bus Access (16-Bit Motorola Mode)

$\overline{\text{BLE}}$	A0	Register Access	OctalLIU™ Data Pins Used
0	0	Register word access (even addresses)	D(15:0)
0	1	Register byte access (odd addresses)	D(7:0)
1	0	Register byte access (even addresses)	D(15:8)
1	1	No transfer performed	None

Table 5 Selectable asynchronous Bus and Microprocessor Interface Configuration

ALE	IM(1:0)	Asynchronous Microprocessor Interface Mode	Bus Structure
Constant level	01	Motorola	De-multiplexed
	00	Intel	De-multiplexed
Switching	00	Intel	Multiplexed

The assignment of registers with even/odd addresses to the data lines in case of 16-bit register access depends on the selected asynchronous microprocessor interface mode:

Intel	(Address n + 1)		(Address n)	
Motorola	(Address n)		(Address n + 1)	
	↑		↑	
	↓		↓	
Data lines	D15	D8	D7	D0

n: even address

3.5.2 Serial Micro Controller Interfaces

Two serial interfaces are included to enable device programming and controlling:- Slave Serial Control Interface (SCI) - Slave Serial Peripheral Interface (SPI)

By using the SCI Interface, the OctalLIU™ can be easily connected to Infineon interworking devices plus Infineon SHDSL- and ADSL-PHYs so that implementation of different line transmission technologies on the same line card easily is possible. The SCI interface is a three-wire bus and optionally replaces the parallel processor interface to reduce wiring overhead on the PCB, especially if multiple devices are used on a single board. Data on the bus is HDLC encapsulated and uses a message-based communication protocol.

If SCI interface with multipoint to multipoint configuration is used, address pins A(5:0) are used for SCI source (slave) address pin strapping, see **Table 2**.

Note that after a reset writing into or reading from OctalLIU™ registers using the SCI- or SPI-Interface is not possible until the PLL is locked: If the SCI-Interface is used no acknowledge message will be sent by the OctalLIU™. If the SPI-Interface is used pin SDO has high impedance (SDO is pulled up by external resistor). To trace if the SPI interface is accessible, the micro controller should poll for example the register DSTR so long as it read no longer the value ´F_H´.

3.5.2.1 SCI Interface

The Serial Control Interface (SCI) is selected if IM(1:0) is strapped to ´11_H´.

The OctalLIU™ SCI interface is always a slave.

Figure 49 shows the timing diagram of the SCI interface, **Table 56** gives the appropriate values of the timing parameters.

Figure 6 shows a first application using the SCI interfaces of some OctalLIU™s where point to point full duplex connections are realized between every OctalLIU™ and the micro controller. Here the data out pins of the SCI interfaces (SCI_TXD) of the OctalLIU™s must be configured as push-pull (PP), see configuration register bit PP in **Table 8**.

Figure 7 shows an application with Multipoint to multipoint connections between the OctalLIU™s and the micro controller (half duplex). Here the data out pin of the SCI interfaces (SCI_TXD) of all OctalLIU™s must be configured as an open Drain (oD), see configuration register bit PP in **Table 8**. The data out and data in pins (SCI_RXD, SCI_TXD) of each OctalLIU™ are connected together to form a common data line. Together with a common pull up resistor for the data line, all open Drain data out pins are building a wired And.

The Infineon proprietary Daisy-Chain approach is not supported

The group address of the SCI interface is ´00_H´ after reset. Recommendation for configuring is ´$C4_H$´ to be different to the group addresses of all other Infineon devices.

In case of multipoint to multipoint applications the 6 MSBs of the SCI source address will be defined by pinstrapping of the address pins A5 to A0. The two LSBs of the SCI source address are constant ´10B´, see **Table 8**. The SCI source address can be overwritten by a write command into the SCI configuration register. For applications with point to point connections for the SCI interface the source address is not valid.

Because 14 bits are used for the register addresses in the SCI interface macro the two MSBs of the 16 bit wide register addresses are set fixed to zero.

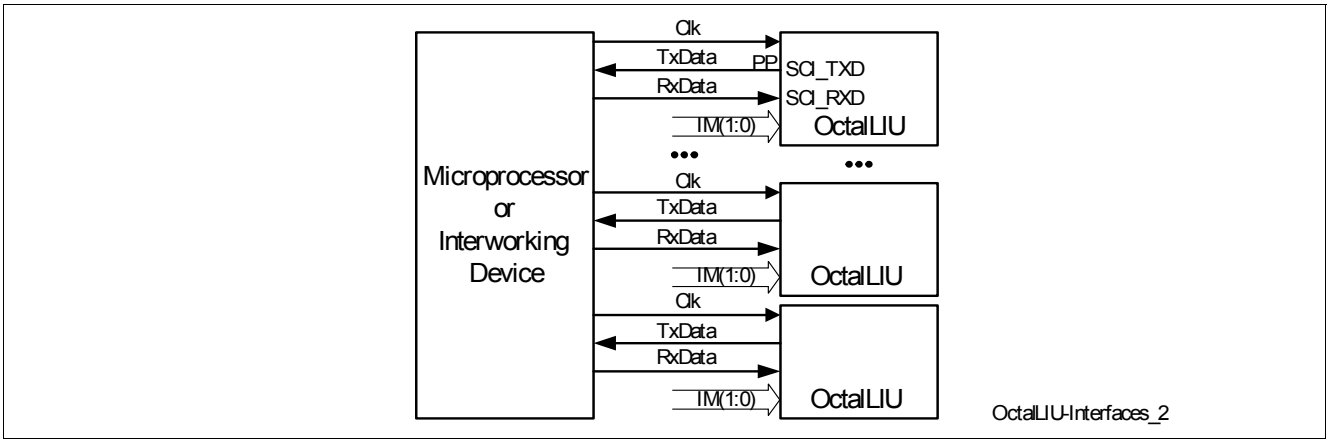


Figure 6 SCI Interface Application with Point To Point Connections

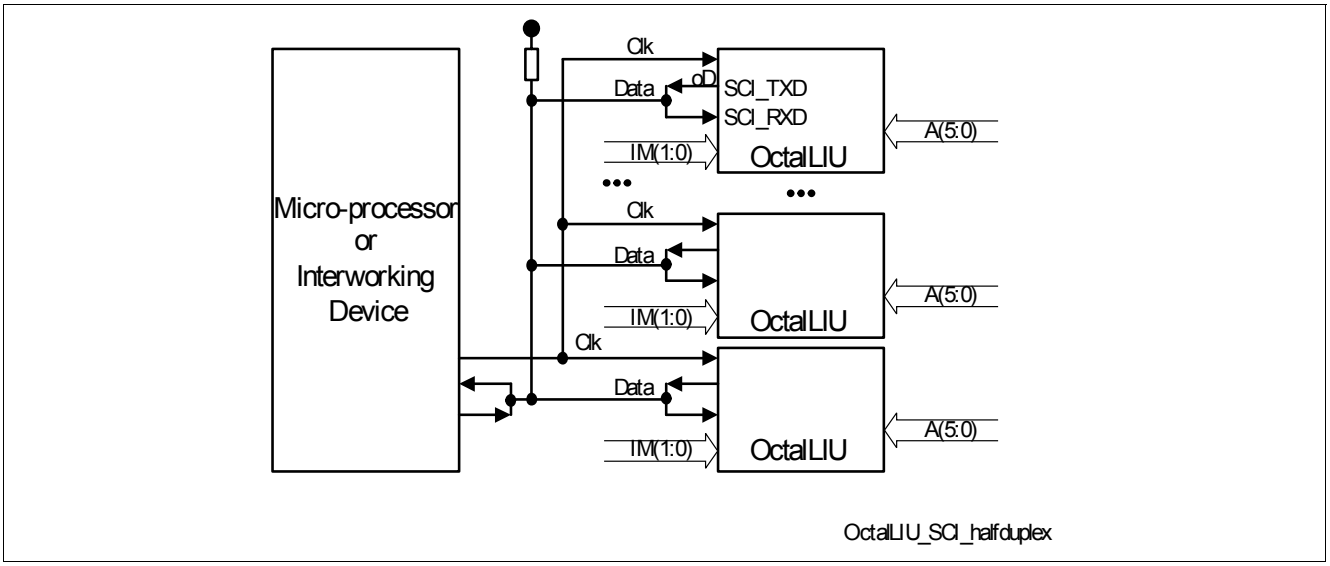


Figure 7 SCI Interface Application with Multipoint To Multipoint Connection

The following configurations of the SCI interface of the OctalLIU™ can be set by the micro controller by a write command into the SCI configuration register (control bits ´10_B´, see **Table 8**, SCI register address is ´0000_H´, see **Table 3** and **Figure 9**):

- Half duplex/full duplex (reset value: Half duplex), bit DUP.
- OpenDrain/push-pull (configuration of output pin to openDrain/push-pull is in general independent of the duplex mode and must be set appropriately in application) (reset value: open Drain), bit PP.
- CRC for transmit and receive on/off (reset value: off), bit CRC_EN.
- Automatic acknowledgement of CMD messages on/off (reset value: off), bit ACK_EN.
- Clock edge rising/falling (reset value: falling), bit CLK_POL.
- Clock gating (reset value: off), bit CLK_GAT.

The following SCI configurations are fixed and cannot be set by the micro controller:

- Interrupt feature is disabled, bit INT_EN = ´0_B´.
- Arbitration always made with LAPD (only SCI applications like in **Figure 6** and **Figure 7** are possible), bit ARB = ´0_B´.

The maximum possible SCI clock frequency is 6 MHz for point to point applications (full duplex) and about 2 MHz for multipoint to multipoint applications, dependent on the electrical capacity of the bus lines of the PCB.

Figure 8 shows the message structure of the OctalLIU™. The SCI interface uses HDLC frames for communication. The HDLC flags mark beginning and end of all messages.

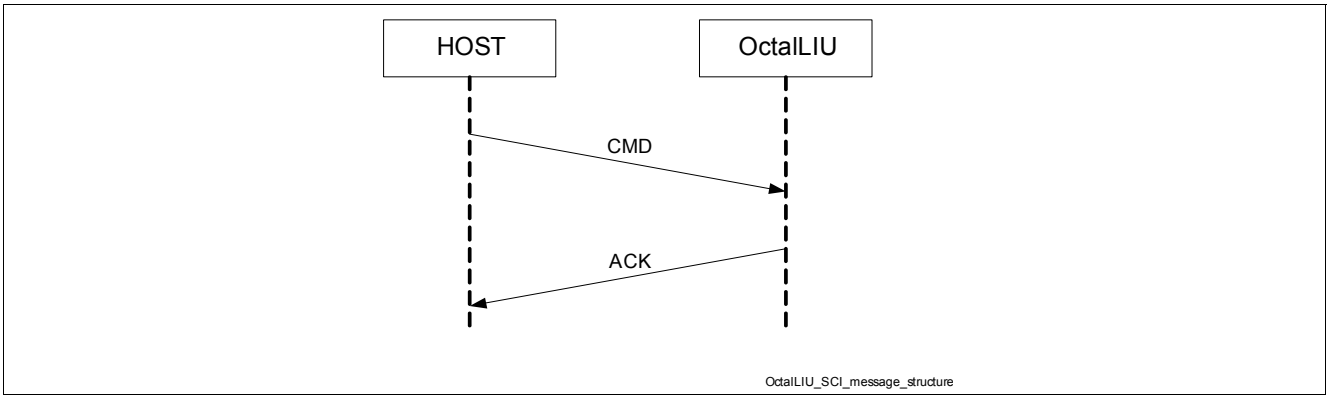


Figure 8 SCI Message Structure of OctalLIU™

Every write into or read from a register of the OctalLIU™ is initiated by a command message CMD from the Host (micro con roller) and is then confirmed by an acknowledge message ACK from the OctalLIU™ if in the SCI configuration automatic acknowledgement is set (bit ACK_EN, see **Table 8**).

The frame structure of this messages are shown in **Figure 9**.

In general the LSB of every byte is transmitted first and lower bytes are transmitted before higher bytes (regarding the register address)

Source and destination addresses are 8 bits long. Only the first 6 bits are really used for addressing. The bit C/R (Command/Response) distinguishes between a command and a response. The bit MS (Master/Slave) is ´0_B´ for all Slaves and ´1_B´ for all masters, see **Table 8** and **Figure 9**

The source address is defined by pinstrapping of A5 to A0 after reset, but other values can be configured by programming of the SCI configuration register.

The payload of the write CMD includes two control bits (MSBs of the payload), which distinguish between the different kind of commands, see **Table 7**, the 14 bit wide register address and the 8 bit wide data whereas the read CMD payload includes only the control bits and the register address. Register addresses can be either OctalLIU™ register addresses or SCI configuration register addresses. Because of the address space of the OctalLIU™, really 11 LSBs of the 14 bit address are used in the OctalLIU™. The 3 MSBs are ignored

The Frame Check Sequence FCS has16 bits

The Read Status Byte RSTA of the acknowledge message shows the status of the received message and is built by the SCI interface of the OctalLIU™, see **Figure 11** and **Table 6**.

The destination address in the ACK message is always the source address of the corresponding CMD (the address of the micro controller), see **Figure 10**, because no CMD messages will be sent by the OctalLIU™ SCI interface

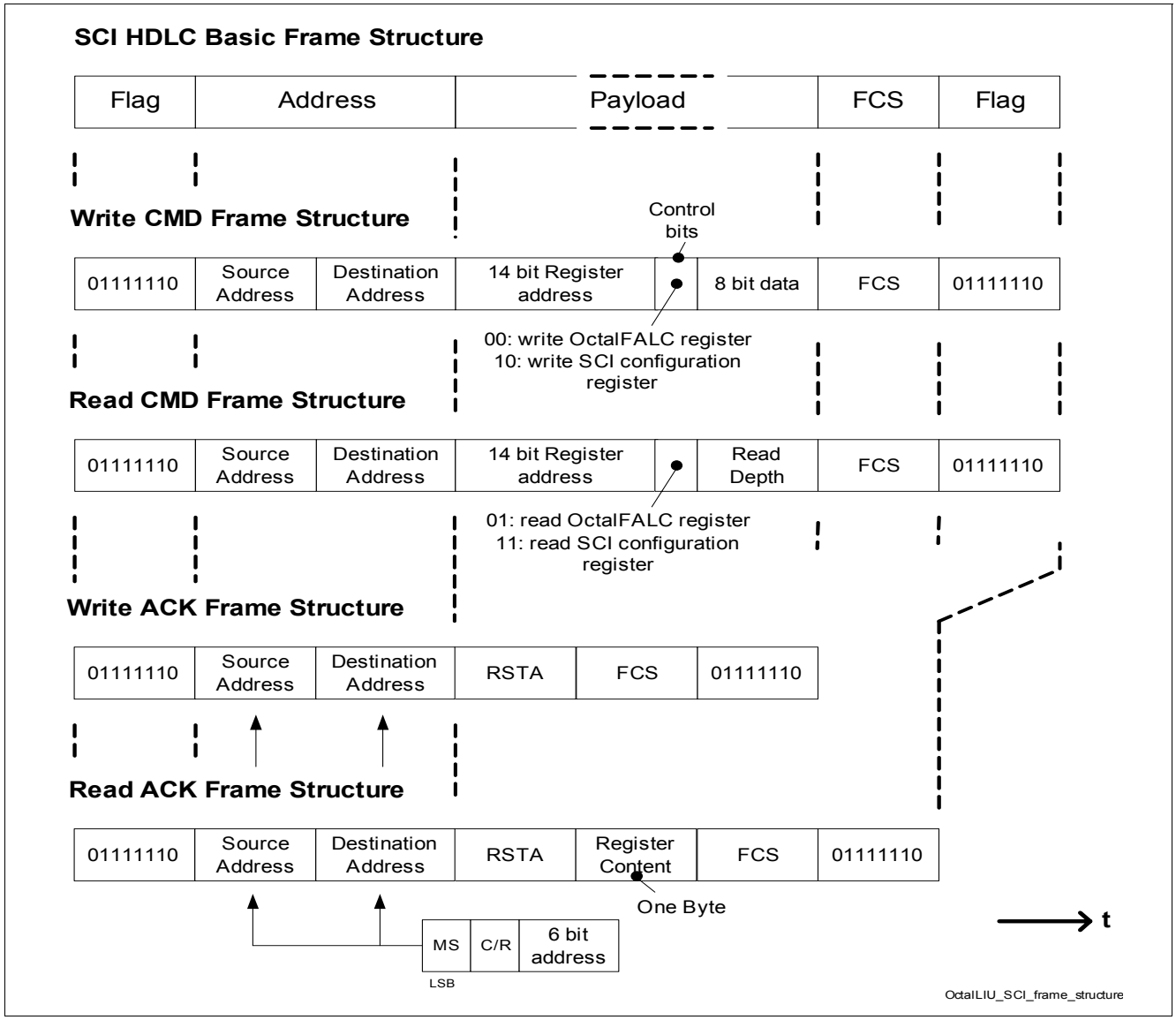


Figure 9 Frame Structure of OctalLIU™ SCI Messages

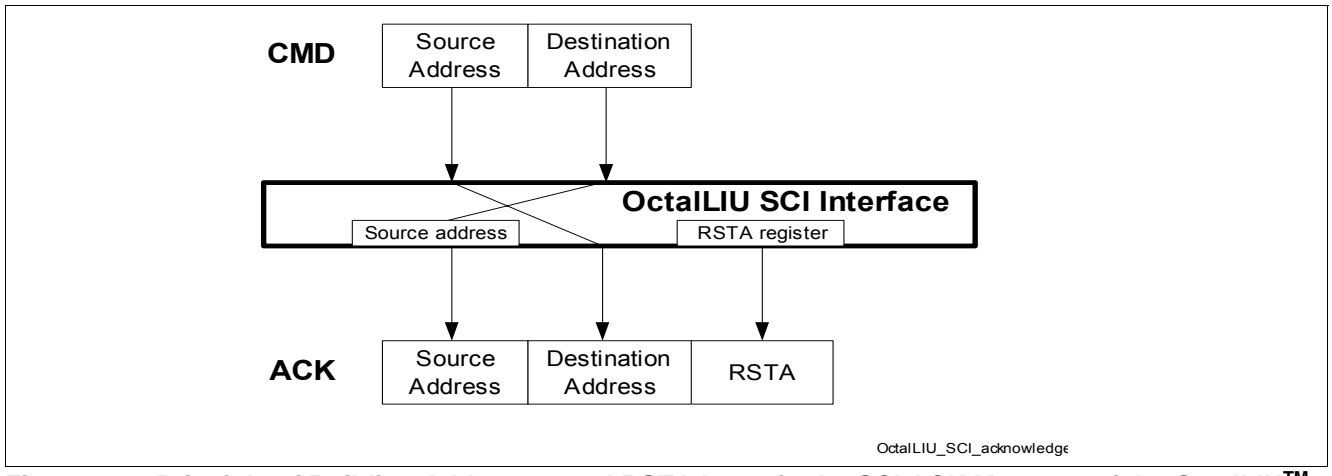


Figure 10 Principle of Building Addresses and RSTA bytes in the SCI ACK Message of the OctalLIU™

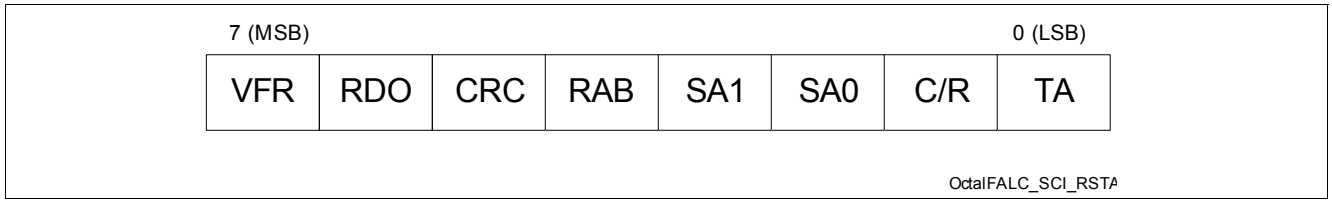


Figure 11 Read Status Byte (RSTA) byte of the SCI Acknowledge (ACK)

Table 6 Read Status Byte (RSTA) Byte of the SCI Acknowledge (ACK)

Field	Bit	Description
VFR	7	Valid Frame. Indicates whether a valid frame has received. 0_B: Received frame is invalid. 1_B: Received frame is valid.
RDO	6	Reserved
CRC	5	CRC compare check. Indicates whether a CRC check is failed or not. 0_B: CRC error check failed on the received frame. 1_B: Received frame is free of CRC errors.
RAB	4	Received message aborted. CMD message abortion is declared. The receive message was aborted by the HOST. A sequence of 7 consecutive ´1´ was detected before closing the flag. Note that ACK message and therefore RAB will not be send before destination address was received. 0_B: Data reception is in progress. 0_B: Data reception has been aborted.
SA1	3	Reserved
SA0	2	Reserved
C/R	1	Reserved
TA	0	Reserved

Table 7 Definition of Control Bits in Commands (CMD)

Control Bits (MSB LSB)	Command type
01	Read OctalLIU™ registers
00	Write OctalLIU™ register1
10	Write SCI configuration register
11	Read SCI configuration register

Table 8 SCI Configuration Register Content

Address	Bit 7 (MSB)	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
´0000_H´	PP	CLK_POL	CLK_GAT	ACK_EN	INT_EN	CRC_EN	ARB	DUP
´0001_H´	1	Destination Address					1 (=C/R)	0 (=MS)
´0002_H´	0	Group Address					1 (=C/R)	0 (=MS)

3.5.2.2 SPI Interface

The Serial Peripheral Interface (SPI) is selected if IM(1:0) is strapped to ´10_H´.

The SPI interface of the OctalLIU™ is always a slave.

Figure 12 and Figure 13 show the read and the write operation respectively. The start of a read or write operation is marked by the falling edge of the chip select signal CS whereas the end of the operations is marked by the rising edge of CS. Because of CS the SPI interface has no slave address.

The first bit of the serial data in (SDI) is ´1´ for a read operation and ´0´ for a write operation. The first four bits of the 15-bit address are not valid for the OctalLIU™.

In read operation the OctalLIU™ delivers the 8 bit wide content of the addressed register at the serial data out (SDO).

In general SPI data are driven with the negative edge of the serial clock (SCLK) and sampled with the positive edge of SCLK. Figure 50 shows the timing of the SPI interface and Table 57 the appropriate timing parameter values.

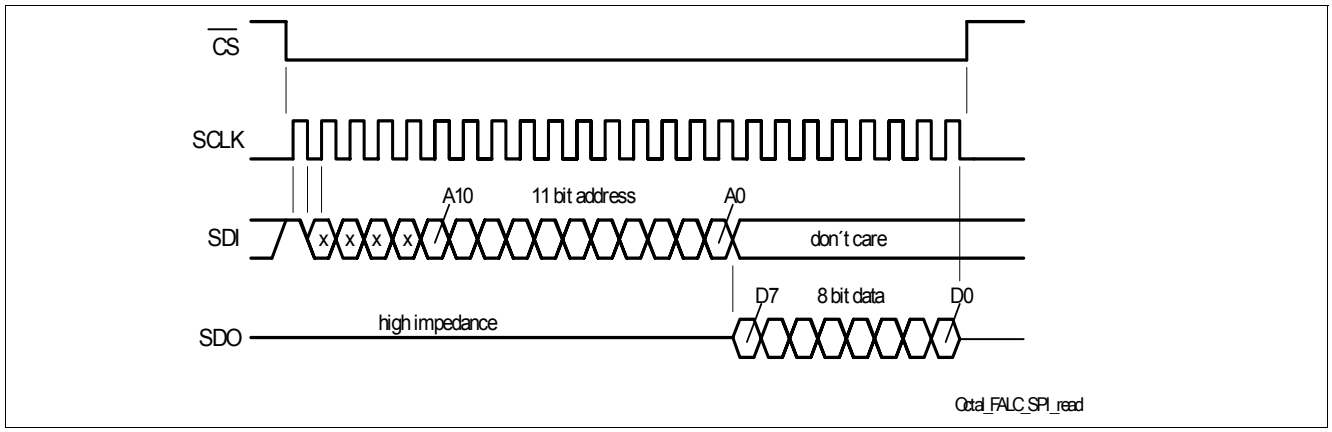


Figure 12 SPI Read Operation

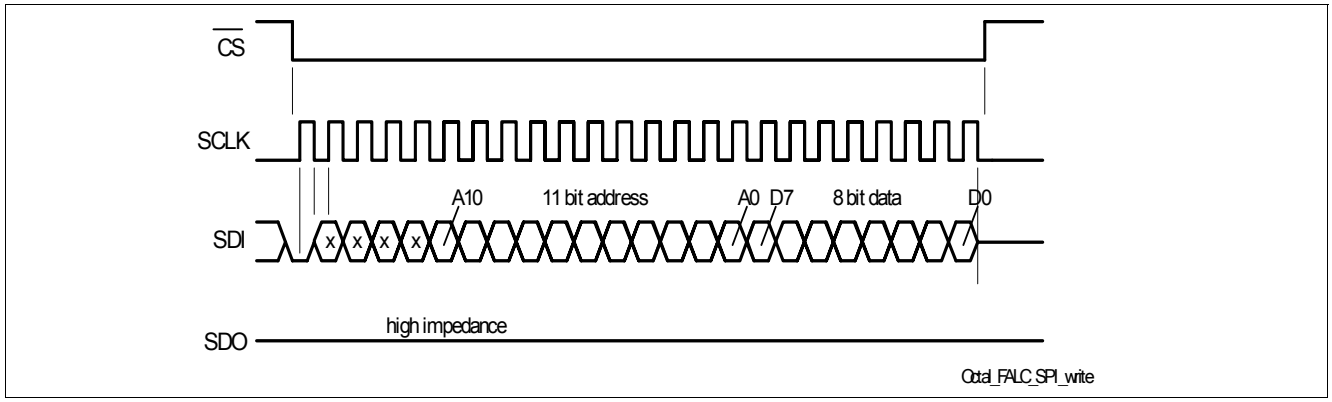


Figure 13 SPI Write Operation

3.5.3 Interrupt Interface

Special events in the OctalLIU™ are indicated by means of an interrupt output INT, which requests the external micro controller to read status information from the OctalLIU™, or to transfer data from/to the OctalLIU™. The electrical characteristics (open drain or push-pull) is programmed defined by the register bits IPC.IC(1:0), see IPC.

The OctalLIU™ has a single interrupt output pin INT with programmable characteristics (open drain or push-pull, defined by registers IPC) too.

Since only one INT request output is provided, the cause of an interrupt must be determined by the external micro controller by reading the OctalLIU™'s interrupt status registers (GIS, ISR(1:4), ISR6 and ISR7). The interrupt on pin INT and the interrupt status bits are reset by reading the interrupt status registers. The interrupt status registers ISR are of type “clear on read“ (“rsc”).

The structure of the interrupt status registers is shown in Figure 14.

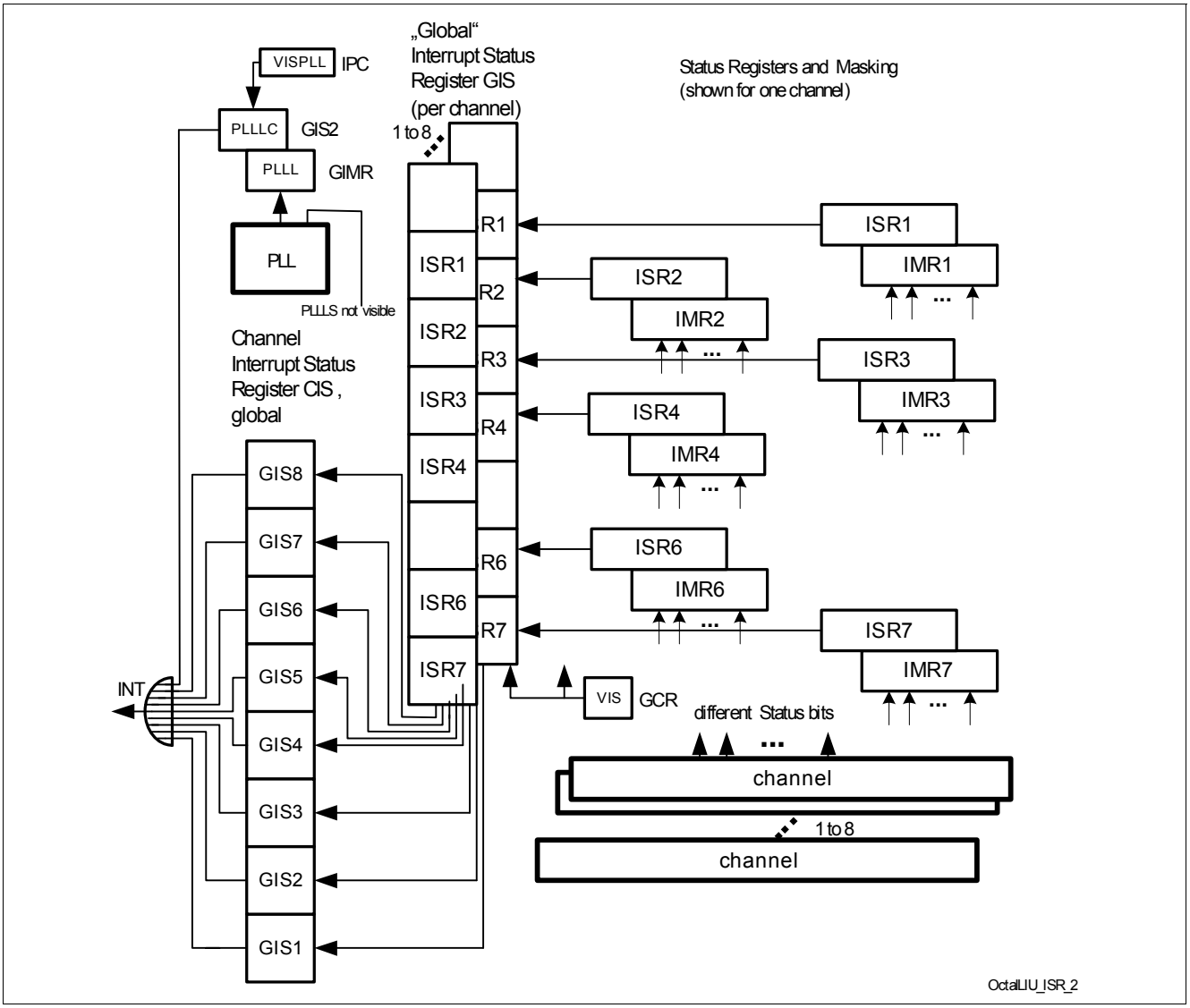


Figure 14 Interrupt Status Registers

Each interrupt indication bit of the registers ISR can be selectively masked by setting the corresponding bit in the corresponding mask registers IMR. If the interrupt status bits are masked they neither generate an interrupt at INT nor are they visible in ISR. **All reserved bits in the mask registers IMR must not be written with the value ´0´.**

GIS, the non-maskable “Global” Interrupt Status Register per channel, serves as pointer to pending interrupts sourced by registers ISR(1:4), ISR6 and ISR7.

The non-maskable Channel Interrupt Status Register CIS serves as channel pointer to pending interrupts sourced by registers GIS.

After the OctalLIU™ has requested an interrupt by activating its INT pin, the external micro controller should first read the register CIS to identify the requesting interrupt source channel. Then it should read the Global Interrupt Status register GIS to identify the requesting interrupt source register ISR of that channel.

After reading the assigned interrupt status registers ISR(1:4), ISR6 and ISR7, the pointer bit in register GIS is cleared or updated if another interrupt requires service. After all bits ISR(7:0) of a register GIS are cleared, the assigned bit in register CIS is cleared. After all bits in register CIS are cleared the INT pin will be deactivated.

If **all** pending interrupts are acknowledged by reading (GIS is reset), pin INT goes inactive.

Updating of interrupt status registers ISR(1:4), ISR6 and ISR7 and GIS is only prohibited during read access.

Masked Interrupts Visible in Status Registers

- The “Global” Interrupt Status register (GIS) indicates those interrupt status registers with active interrupt indications (bits GIS.ISR(7:0)).
- An additional interrupt mode can be selected per port via bit GCR.VIS (**GCR**). In this mode, masked interrupt status bits neither generate an interrupt on pin INT nor are they visible in GIS, **but are displayed in the corresponding interrupt status registers ISR(1:4), ISR6 and ISR7.**

PLL Interrupt Status Register

- The bit n (n = 1 to 8) of the register CIS pointers an interrupt on channel n.
- The Global Interrupt Status register GIS2 indicates the lock status of the (global) PLL. Masking can be done by the register GIMR.
- An additional interrupt mode can be selected per port via bit IPC.VISPLL (**IPC**) where the masked interrupt status bit GIS2.PLLLS does not generate an interrupt on pin INT, **but is displayed in the corresponding interrupt status register bit GIS2.PLLLC**.

The additional interrupt mode is useful when some interrupt status bits are to be polled in the individual interrupt status registers.

Table 9 Interrupt Modes

GCR.VIS; IPC.VISPLL	Appropriate Mask bit	Interrupt active	Visibility in ISR(1:4), ISR(6:7) and GIS2
0	0	yes	yes
0	1	no	no
1	0	yes	yes
1	1	no	yes

Note:

1. *In the visible mode, all active interrupt status bits, whether the corresponding actual interrupt is masked or not, are reset when the interrupt status register is read. Thus, when polling of some interrupt status bits is desired, care must be taken that unmasked interrupts are not lost in the process.*
2. *All unmasked interrupt statuses are treated as before.*

Please note that whenever polling is used, all interrupt status registers concerned have to be polled individually (no “hierarchical” polling possible), since GIS only contains information on actually generated, i.e. unmasked interrupts.

3.5.4 Boundary Scan Interface

In the OctalLIU™ a **T**est **A**ccess **P**ort (TAP) controller is implemented. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes of the boundary scan. Both, TAP controller and boundary scan, meet the requirements given by the JTAG standard IEEE 1149.1-2001. **Figure 15** gives an overview, **Figure 41** shows the timing diagram and **Table 52** gives the appropriate values of the timing parameters.

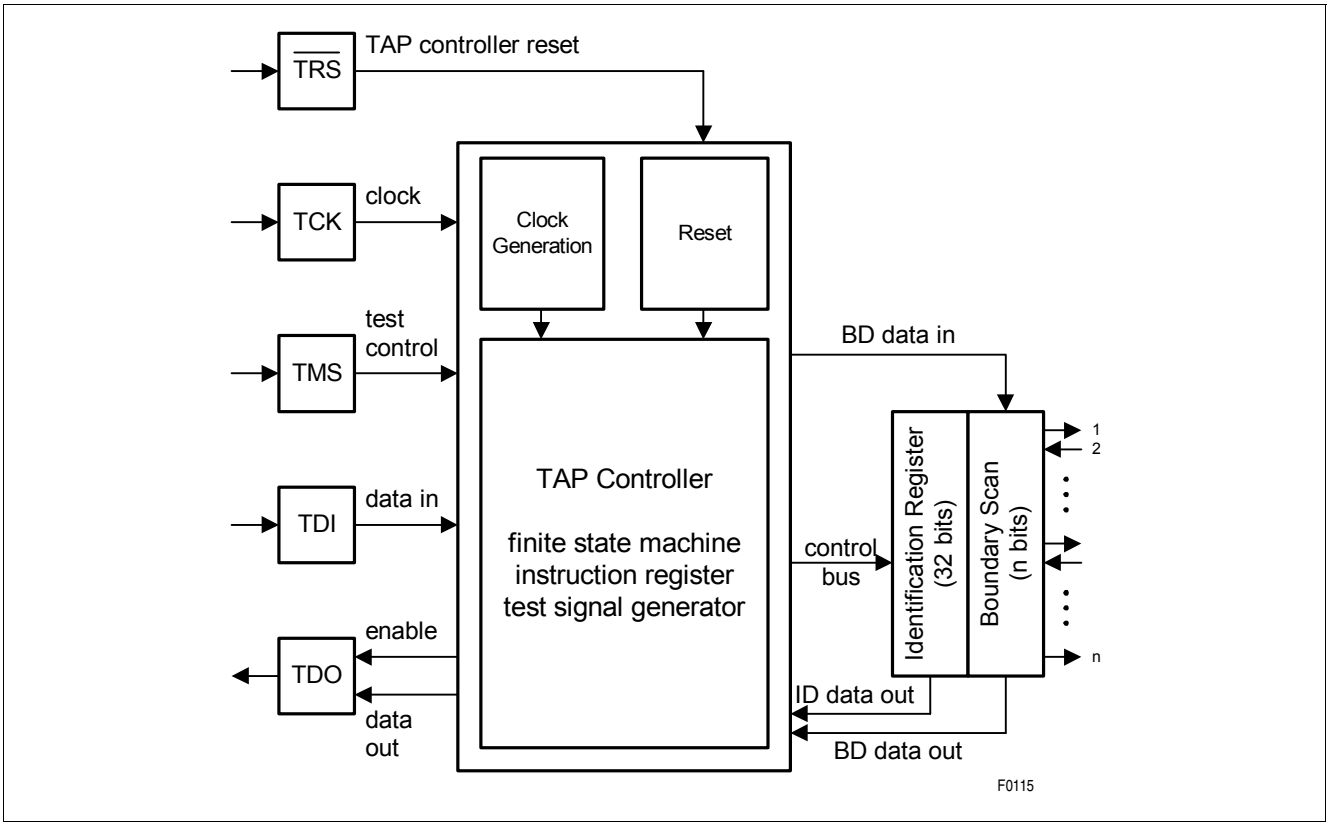


Figure 15 Block Diagram of Test Access Port and Boundary Scan

After switching on the device (power-on), a reset signal has to be applied to $\overline{TRS}$, which forces the TAP controller into test logic reset state.

For normal operation without boundary scan access, the boundary reset pin $\overline{TRS}$ can be tied to the device reset pin $\overline{RES}$.

The boundary length is 247.

If no boundary scan operation is used, $\overline{TRS}$ has to be connected to $\overline{RST}$ or V_{SS}. TMS, TCK and TDI do not need to be connected since pull-up transistors ensure high input levels in this case.

Test handling (boundary scan operation) is performed using the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input) and TDO (Test Data Output) when the TAP controller is not in its reset state, that means $\overline{TRS}$ is connected to V_{DD} or it remains unconnected due to its internal pull up. Test data at TDI is loaded with a clock signal connected to TCK. "1" or "0" on TMS causes a transition from one controller state to another; constant "1" on TMS leads to normal operation of the chip.

An input pin (I) uses one boundary scan cell (data in), an output pin (O) uses two cells (data out and enable) and an I/O-pin (I/O) uses three cells (data in, data out and enable). Note that most functional output and input pins of the OctalLIU™ are tested as I/O pins in boundary scan, hence using three cells.

The desired test mode is selected by serially loading a 8-bit instruction code into the instruction register through TDI (LSB first), see **Table 10**. The test modes are:

EXTEST

Extest is used to examine the interconnection of the devices on the board. In this test mode at first all input pins capture the current level on the corresponding external interconnection line, whereas all output pins are held at constant values ("0" or "1"). Then the contents of the boundary scan is shifted to TDO. At the same time the next scan vector is loaded from TDI. Subsequently all output pins are updated according to the new boundary scan contents and all input pins again capture the current external level afterwards, and so on.

SAMPLE

Is a test mode which provides a snapshot of pin levels during normal operation.

IDCODE

A 32-bit identification register is serially read out on pin TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to "1".

The ID code field is set to (MSB to LSB): ´0001 0000 0000 1101 1110 0000 1000 0011_B´.

Version number (first 4 bits) = ´0001_B´

Part Number (next 16 bits) = ´0000 0000 1101 1110_B´

Manufacturer ID (next 11 bits) =´0000 1000 001_B´

LSB fixed to ´1´.

BYPASS

A bit entering TDI is shifted to TDO after one TCK clock cycle.

An alphabetical overview of all TAP controller operation codes is given in **Table 10**.

Table 10 TAP Controller Instruction Codes

TAP Instruction	Instruction Code
BYPASS	11111111
EXTEST	00000000
IDCODE	00000100
SAMPLE	00000001
Reserved for device test	01010011

3.5.5 Master Clocking Unit

The OctalLIU™ provides a flexible clocking unit, which references to any clock in the range of 1.02 to 20 MHz supplied on pin MCLK, see **Figure 16**.

The clocking unit has two different modes:

- In the so called “flexible master clocking mode” (GCM2.VFREQ_EN = ´1´, **CMR2**) the clocking unit has to be tuned to the selected reference frequency by setting the global clock mode registers GCM(8:1) accordingly, see formulas in **GCM6**. All eight ports can work in E1 or T1 mode individually. After reset the clocking unit is in “flexible master clocking mode”.
- In the so called “clocking fixed mode” (GCM2.VFREQ_EN = ´0´) the tuning of the clocking unit is done internally so that no setting of the global clock mode registers GCM(8:1) is necessary. All eight ports must work together either in E1 or in T1 mode.

For the calculation for the appropriate register settings see **GCM6**. Calculation can be done easy by using the flexible Master Clock Calculator which is part of the software support of the OctalLIU™, see **Chapter 8.3**.

All required clocks for E1 or T1/J1 operation are generated by this circuit internally. The global setting depends only on the selected master clock frequency and is the same for E1 and T1/J1 because both clock rates are provided simultaneously.

To meet the E1 requirements the MCLK reference clock must have an accuracy of better than ± 32 ppm. The synthesized clock can be controlled on pins RCLK and FCLKR.

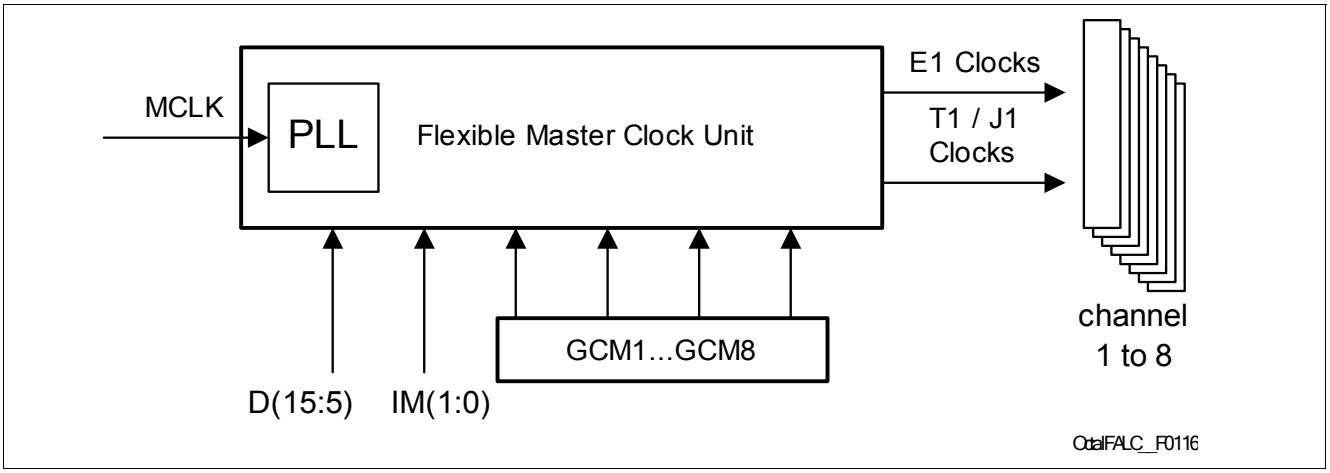


Figure 16 Flexible Master Clock Unit

3.5.5.1 PLL (Reset and Configuring)

If the (asynchronous) micro controller interface mode is selected by IM(1:0) the PLL must be configured

- By programming of the registers GCM5 and GCM6 in “flexible master clocking mode”. Every change of the contents of these registers - the divider factors N and M of the PLL - causes a reset of the PLL. Switching between E1 and T1 modes in arbitrary channels causes a reset of the clock unit but not of the PLL itself.
- Or by enabling of the ”fixed mode”: GCM2.VFREQ_EN = ´0´ (**GCM2**). Programming of registers GCM5 and GCM6 is not necessary. Any programming of GCM5 and GCM6 does NOT cause a reset of the PLL. Switching between E1 and T1 modes (for all channels) causes a reset of the clock unit but not of the PLL itself.

The SPI and SCI are synchronous interfaces and therefore need defined clocks immediately after reset, before any configuration is done. So to enable access to serial interfaces, the clock MCLK must be active and must have a defined frequency before reset becomes inactive. Dependent on the MCLK frequency the internal PLL must be configured if the SCI- or SPI-Interface mode is selected by IM(1:0)

- By strapping of the pins D(15:5) if “fixed mode” is not enabled (GCM2.VFREQ_EN = ´1´), see also **Table 2**. Because “fixed mode” is not enabled after reset, pinstrapping at D(15:5) is always necessary! Every new value at this pins causes a reset of the PLL. Configuring by the registers GCM5 and GCM6 is not taken into account and causes not a reset of the PLL
- Or by enabling of the ” fixed mode”.This is only allowed if the values of N and M defined by pinstrapping are identical to that values which are internally used for the “fixed mode”. That avoids changing of N and M by switching into the ”fixed mode” and therefore a new reset of the PLL. (A new reset of the PLL can cause a hang up of the whole system!) In ”fixed mode” the values are: N = ´33_{10}´, M = ´0_{10}´ so that the pinstrapping must be: D(10:5) = ´HLLLLH´, D(15:11) = ´LLLLL´. In ”fixed mode” programming of registers GCM1 to GCM8 is no longer necessary and values at the pins D(15:5) are no longer taken into account and causes NOT a reset of the PLL. A switching between E1 and T1 modes causes a reset of the clock unit but not of the PLL itself.

The configuration of the PLL by pinstrapping (see **Table 2**) in case of serial interface modes is done in the same way as by using the registers GCM5 and GCM6 if asynchronous micro controller interface mode (Intel or Motorola) is selected. So calculation of the pinstrapping values can be done also by using the formulas in **GCM6** or by using the “flexible Master Clock Calculator” which is part of the software support of the OctalLIU™, see **Chapter 8.3**. If the serial interfaces are selected, pinstrapping of D(15:5) configure the PLL directly, so changes causes always a reset of the PLL.

The conditions to trigger a reset of the central clock PLL are listed in **Table 11**. Every reset of the PLL causes a reset of the clock system.

Table 11 Conditions for a PLL Reset

Reset Pin	GCM2.VFREQ_EN	Used controller interface	A PLL reset is made if ...
Active	X (will be set to ´1´ by reset)	X	Always
Inactive	1	Asynchron (Motorola or Intel)	If GCM5 or GCM6 are written and their values N or M change
		SPI or SCI	If pinstrapping values change
	0	Asynchron (Motorola or Intel)	Never
		SPI or SCI	If pinstrapping values change
	0 -> 1 or 1 -> 0	Asynchron (Motorola or Intel)	If actual values of N or M in GCM5 or GCM6 are different to internal settings of the “clocking fixed mode”
		SPI or SCI	If pinstrap values are different to internal settings of the “clocking fixed mode”; That is not allowed!

3.6 Line Coding and Framer Interface Modes

An overview of the coding at the line interface and the Modes at the framer interface is given in **Table 12**.

Table 12 Line Coding and Framer Interface Modes

Line Code, Framer IF Mode	Register Bits		Signals at Pins			
	FMR0.RC, LIM3.DRR	FMR0.XC, LIM3.DRX	RDON (RPC)	RDO	XDI	XDIN (XPB)
AMI, single rail	10 0	10 0	Pos and neg	AMI error	Pos, via encoder	Neg, via encoder
AMI, dual rail	10 1	10 1	Pos	Neg	Pos, encoder bypass	Neg, encoder bypass
HDB3/B8ZS, single rail	11 0	11 0	Decoded data	Violation	Via encoder	(HDB3/B8ZS coding)
HDB3/B8ZS, dual rail	11 1	11 1	Pos	Neg	Via encoder	(HDB3/B8ZS coding)
NRZ, single rail	00 0	00 0	Pos	´0´	NRZ, via encoder	Frame marker
NRZ, dual rail	00 1	00 1	Pos	Neg	NRZ	Frame marker
CMI, single rail	01 0	01 0	Decoded data	Violation	Via encoder	(CMI coding)
CMI, dual rail	01 1	01 1	Pos	Neg	Via encoder	(CMI coding)

Table 12 Line Coding and Framer Interface Modes (cont'd)

Line Code, Framer IF Mode	Register Bits		Signals at Pins			
	FMR0.RC, LIM3.DRR	FMR0.XC, LIM3.DRX	RDON (RPC)	RDO	XDI	XDIN (XPB)
	0 -> 1 or 1 -> 0	Asynchron (Motorola or Intel)	If actual values of N or M in GCM5 or GCM6 are different to internal settings of the "clocking fixed mode"			
		SPI or SCI	If pinstrap values are different to internal settings of the "clocking fixed mode"; That is not allowed!			

3.7 Receive Path

An overview about the receive path of one channel of the OctalLIU™ is given in **Figure 17**.

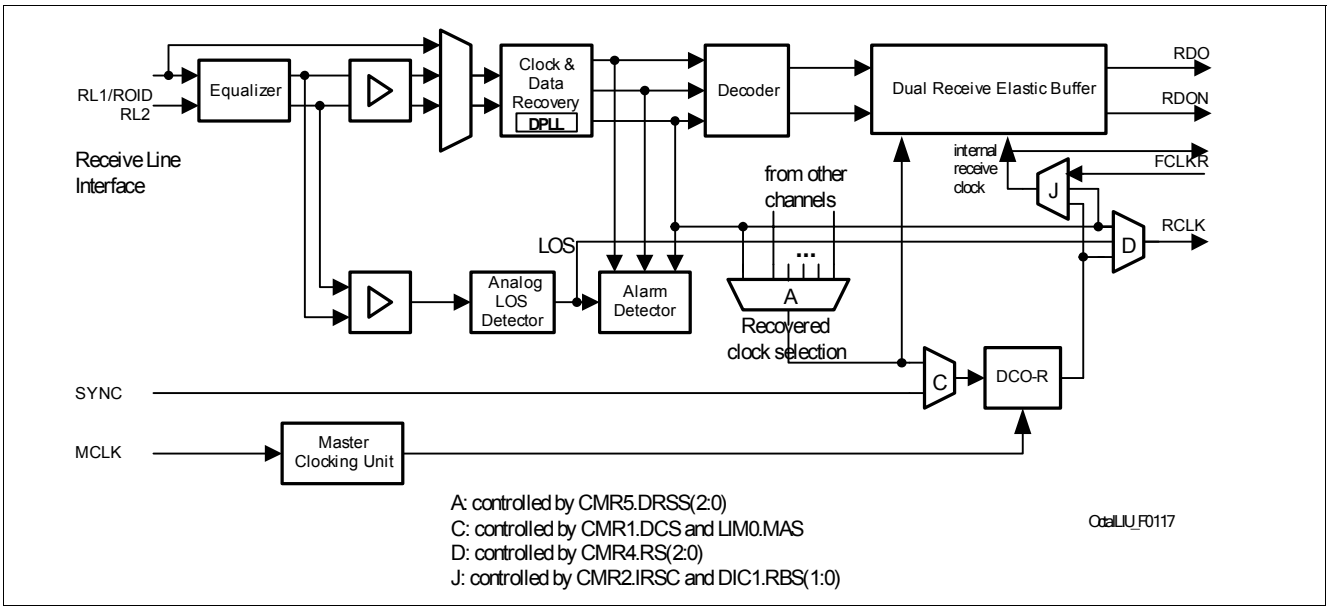


Figure 17 Receive System of one channel

The recovered clock selection of **Figure 17** (multiplexer "A") is shown in more detail in **Figure 18**.

The multiplexer "C" in **Figure 17** selects the mode of the receive jitter attenuator, see chapter **Chapter 3.7.9**.

The multiplexer "D" in **Figure 17** selects if the receive clock RCLK of a channel is sourced by the recovered route clock or by the DCO-R (see above). The appropriate control register bits are CMR4.RS(2:0) (**CMR4**). These register bits selects also different DCO-R output frequencies.

The sources of the receive clock output pins of the OctalLIU™ (RCLK(8:1)), can be selected out of the receive clocks of the channels:

The source of each of the eight receive clock pins of the OctalLIU™ (RCLK(8:1)) can be independently selected out of each of the eight receive clocks of the channels by programming the registers bits GPC(2:6).RS(2:0) (**GPC2**), see cross connection "B" in **Figure 18**.

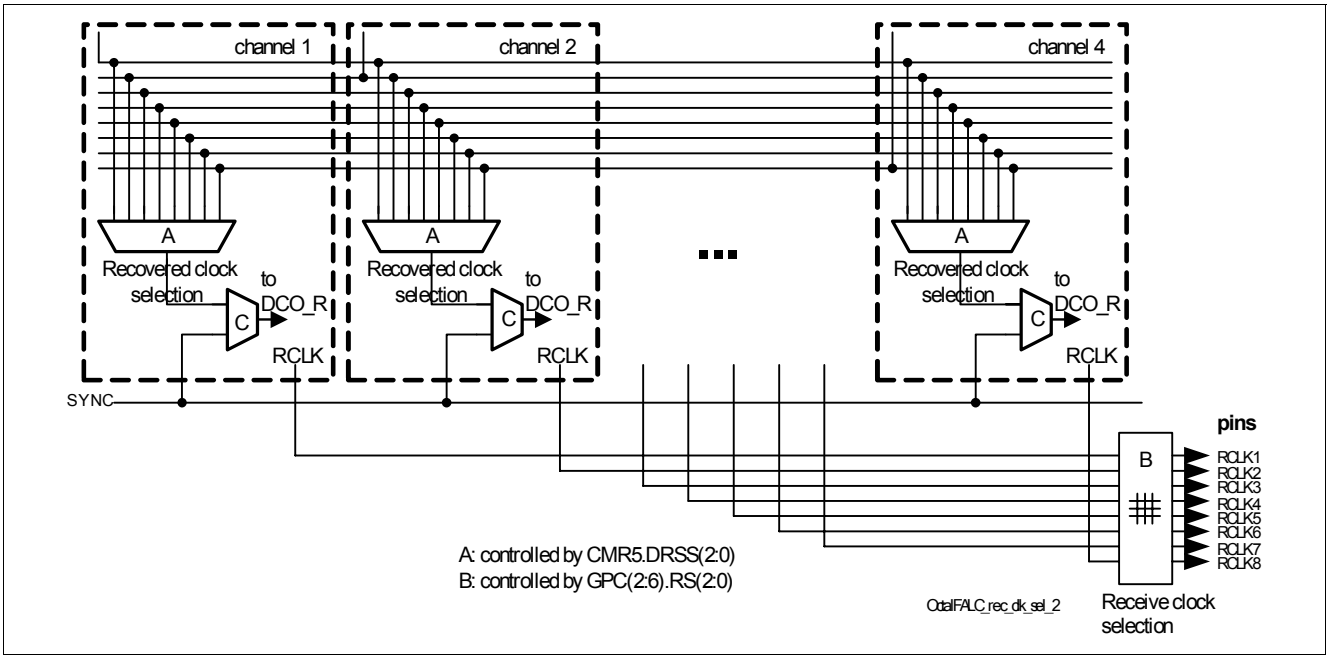


Figure 18 Recovered and Receive Clock Selection

3.7.1 Receive Line Interface

For data input, two different data types are supported (see also **Table 12**):

- Ternary coded signals received at pins RL1 and RL2 from 0 dB downto -43 dB for E1 or downto -36 dB for T1/J1 ternary interface. The ternary interface is selected if LIM1.DRS is cleared.
- Unipolar data (CMI code) on pin ROID received from an optical interface. The optical interface is selected if LIM1.DRS is set and MR0.RC(1:0) = ´01_b´.

3.7.2 Receive Line Coding

In E1 applications, HDB3 line code and AMI coding is provided for the data received from the ternary interface. In T1/J1 mode, B8ZS and AMI code is supported. Selection of the receive line code is done with register bits MR0.RC(1:0) (**MR0**). In case of the optical interface the CMI Code (1T2B) with HDB3 or AMI postprocessing is provided. If CMI code is selected the receive route clock is recovered from the data stream. The CMI decoder does not correct any errors. The HDB3 code is used along with double violation detection or extended code violation detection (selectable by MR0.EXZE)). In AMI code all code violations are detected. The detected errors increment the code violation counter (16 bits length).

The signal at the ternary interface is received at both ends of a transformer.

An overview of the receive line coding is given in **Table 12**.

3.7.3 Receive Line Termination (Analog Switch)

In general the E1 line impedance operating modes with 75 Ω (used with coaxial cable) or with 120 Ω (used with twisted pair cable) line termination are selectable by switching resistors in parallel or using special transformers with different transfer ratios in one package (using center tap). These two options both provide only one analog front end circuitry for both transmission media types.

The OctalLIU™ supports a software selectable generic E1/T1/J1 solution without the need for external hardware changes by using the integrated analog switch and two external resistors for line impedance matching, see application example in **Figure 19**. By default the analog switch is off.

This allows, for example, to switch between 100 W (T1/E1 twisted pair) and 75 W (E1 coax) termination resistance using the external resistors R_{E1} = 100 Ω and R_{E2} = 300 Ω, see **Table 13**. The analog switch can be controlled by access to the register bit LIM0.RTRS (**LIM0**) and by hardware using the receive Multi Function Ports. For that, only

one (but not more) of the receive Multi Function Ports must be configured as Receive Line Termination (RLT) input. For controlling of the analog switch a logical equivalence is build out of RLT and the register bit LIM0.RTRS if RLT is configured at one multi function port.

If the analog switched is not used in an application, the pin RLS can be left open.

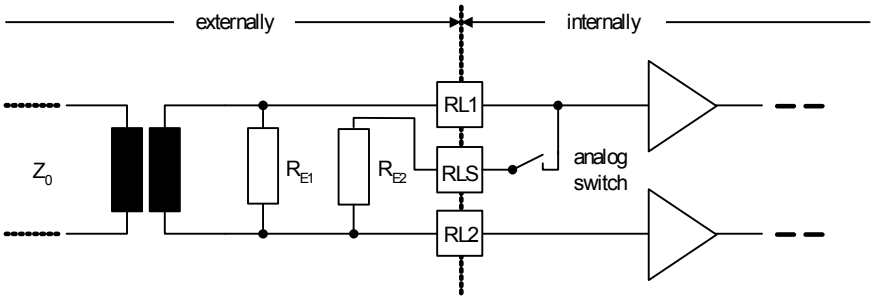


Figure 19 Receiver Configuration with Integrated Analog Switch for Receive Impedance Matching

Table 13 Receiver Configuration Examples

Line Impedance Z_0	External Resistor R_{E1}	External Resistor R_{E2}	Internal Analog Switch	LIM0.RTRS; RLT
120 Ω	100 Ω (for common E1/T1/J1 applications)	300 Ω (for common E1/T1/J1 applications)	Off	If RLT is configured: (LIM0.RTRS equivalent RLT) = ´0´ If RLT is not configured: LIM0.RTRS = ´0´
100 Ω			Off	
75 Ω			On	If RLT is configured: (LIM0.RTRS equivalent RLT) = ´1´ If RLT is not configured: LIM0.RTRS = ´1´

3.7.4 Receive Line Monitoring Mode

For short-haul applications like shown in **Figure 20**, the receive equalizer can be switched into receive line monitoring mode (LIM0.RLM = ´1´). One channel is used as a short-haul receiver while the other is used as a short-haul monitor. In this mode the receiver sensitivity is increased to detect an incoming signal of -20 dB resistive attenuation. The required resistor values are given in **Table 14**.

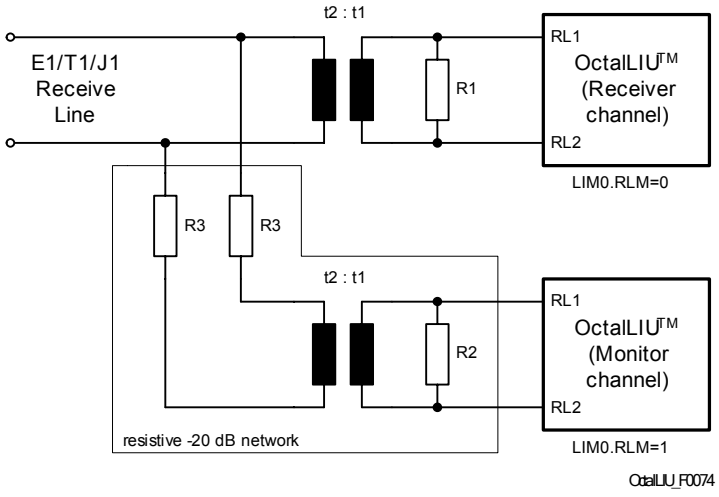


Figure 20 Receive Line Monitoring RLM (shown for one line)

Table 14 External Component Recommendations (Monitoring)

Parameter[1]	Characteristic Impedance (Ohm)		Characteristic Impedance (Ohm)	
	E1		T1	J1
	75	**120**	**100**	**110**
R_1 (±1 %) (Ω)	75	120	100	110
R_2 (±1 %) (Ω)	75	120	100	110
R_3 (±1 %) (Ω)	330	510	430	470
$t_2 : t_1$	1 :1	1 :1	1 : 1	1 : 1

1) This includes all parasitic effects caused by circuit board design.

Using the receive line monitor mode and the hardware tristate function of transmit lines XL1/2 on the line side and the tristate functions on the framer side, the OctalLIU™ supports applications connecting two channels to one receive and transmission line. In these kind of applications both channels are working in parallel for redundancy purpose (see **Figure 21**). While one of them is driving the line, the other one must be switched into transmit line tristate mode. If both channels are configured identically and supplied with the same system data and clocks, the transmit path can be switched from one channel to the other without causing a synchronization loss at the remote end.

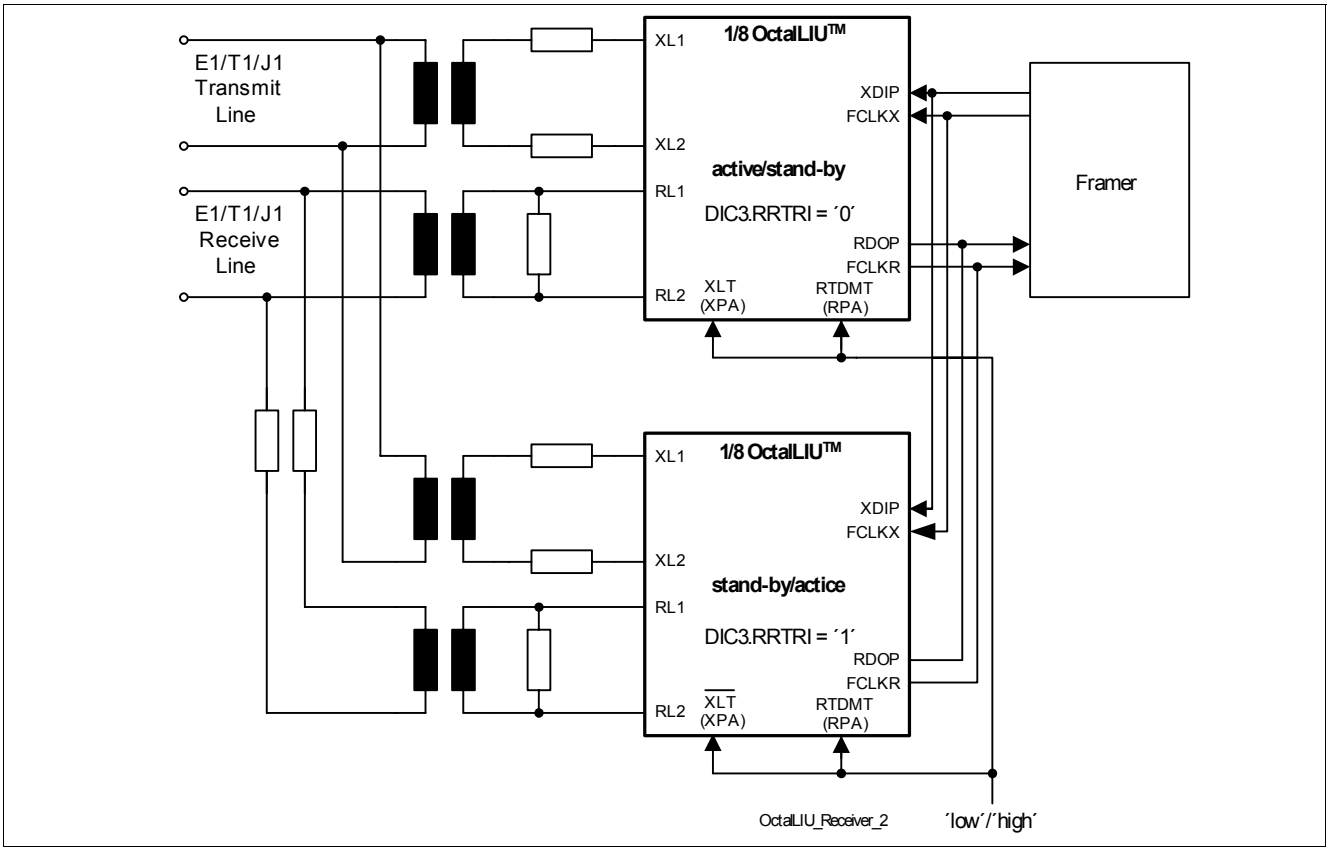


Figure 21 Redundancy Application using RLM (shown for one line)

RDOP and FCLKR can be set into tristate mode constantly for redundancy applications using the register bit DIC3.RRTRI (**DIC3**) and - if the RTDMT function is selected on one of the multi function port - by RTDMT, see **Chapter 3.12**. If the RTDMT function is selected the values of RTDMT and DIC3.RRTRI are logically exored. This enables an easy redundancy application using only one signal for switching between two devices. If the RTDMT function is not selected DIC3.RRTRI = ´1´ set the pins into tristate mode constantly. In this mode “tristate” means high impedance against V_{DD} and V_{SS}: No pull up or pull down resistor is active.

An overview about the tristate configurations of RDOP and RCLK is given in Table 15.

Table 15 Tristate Configurations for the RDO and RCLK pins

DIC3.RRTRI / DIC3.RRTRI exor RTDMT if RTDMT is selected on multi function port	DIC3.RTRI	Pin RDOP	Pin FCLKX
1	X	Constant tristate (without pull up and pull down resistor)	Constant tristate (without pull up and pull down resistor)
0	0	Never tristate	Never tristate
0	1	Tristate during inactive channel phases (with pull up resistor	Never tristate

Switching between both channels can be done on the line side in transmit direction by a hardware signal if the multi function pin XPA is configured as tristate input XLT by the register bits PC1.XPC1 = ´1000_B´, see PC1. If one pin XPA is programmed as low active (PC1.XPC1 = ´1110_B´) and the one of the other channel as high active (PC1.XPC1 = ´1000_B´), no external inverter is necessary as shown in Figure 21. So switching between both channels on line side is possible using only one signal.

Switching can also be done on the line side in transmit direction by software, if setting the register bit XPM2.XLT. The register bit value XPM2.XLT and the pin value of XPA are logically OR´d. (That means if XPA is configured as low active then tristate = XPM2.XLT or not($\overline{XPA}$).

Because the register bit XPM2.XLT and the multi function pin XPA exist individually for every channel, switching on the line side in transmit direction can be done between channels of different or of the same OctalLIU™ device

Switching between both channels can be done on the system side in receive direction by using the register bit DIC3.RRTRI and with or without selection of the multi function port as RTDMT. If the RTDMT function is selected the values of RTDMT and DIC3.RRTRI are logically exored. If in one of the both channels DIC3.RRTRI is set, RTDMT is low active because of the logical exor, and if in the other channel DIC3.RRTRI is cleared, RTDMT is low active because of the logical exor. So switching between both channels on system (framer) side in receive direction is possible using only one signal.

By using the XLT, $\overline{XLT}$ and RTDMT function of the multi function ports and do the appropriate programming of the bits DIC3.RRTRI (DIC3), switching between both channels can be done on the system and the line side together with only one common signal, connected to XPA (XLT, $\overline{XLT}$) and RPA (RTDMT), as shown in Figure 21 and Table 16: If this signal has low-level channel 1 is active and channel 2 is in stand-by, if it has high level channel 1 is in stand-by and channel 2 is active.

Table 16 Redundancy Application using RLM, switching with only one signal

Configuration	Register Bits	Channel 1 (active)	Channel 2 (stand-by)
XLT, $\overline{XLT}$	PC1.XPC1(3:0)	1000	1110
RTDMT	PC1.RPC1(3:0)	1101	1101
Receive system interface	DIC3.RRTRI	0	1
RLM mode	LIM0.RLM	0	1

Figure 22 shows a redundancy application for long haul mode using the internal analog switch. With the configuration shown in Table 17, switching between both channels is possible using only one board signal which is connected to XLT, $\overline{XLT}$, RLT and RTDMT. Because the OctalLIU™ builds the logical equivalence out of RLT and LIM0.RTRS, the analog switches of both channels are controlled by these signal.

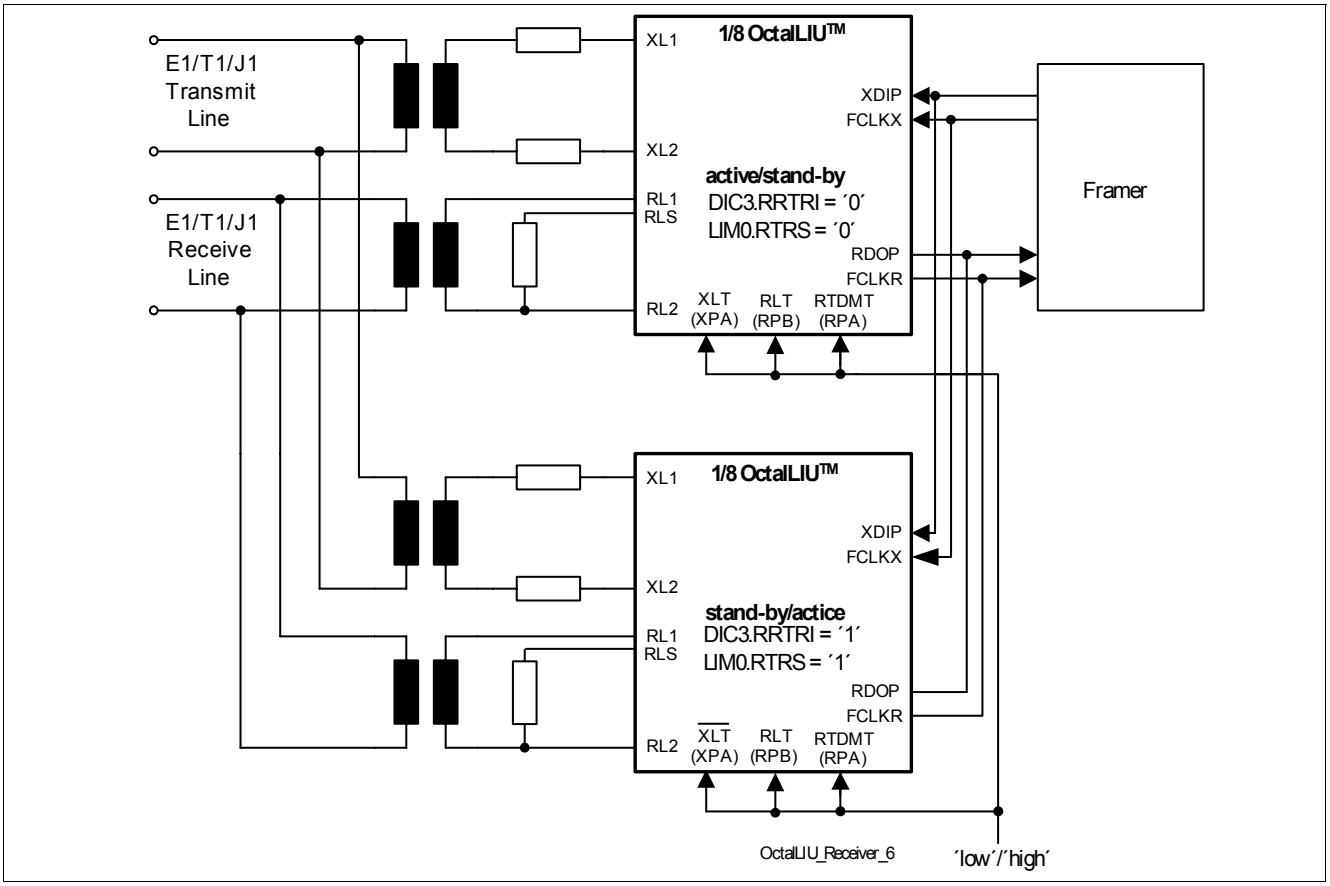


Figure 22 Long Haul Redundancy Application using the Analog Switch (shown for one line)

Table 17 Redundancy Application using the Analog Switch, switching with only one board signal

Configuration	Register Bits	Channel 1 (active/stand-by)	Channel 2 (stand-by/active)
XLT, $\overline{\text{XLT}}$	PC1.XPC1(3:0)	1000	1110
RTDMT	PC1.RPC1(3:0)	1101	1101
Receive framer interface	DIC3.RRTRI	0	1
RLT	PC2.RPC2(3:0)	1000	1000
Receive line termination	LIM0.RTRS	0	0

3.7.5 Loss-of-Signal Detection

There are different definitions for detecting Loss-Of-Signal (LOS) alarms in the ITU-T G.775 and ETS 300233. The OctalLIU™ covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally a LOS status change interrupt is programmable by using register GCR.SCI.

- Detection: An alarm is generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. A pulse with an amplitude less than Q dB below nominal is the criteria for “no pulse” in the analog receive interface (LIM1.DRS = ´0´) (**LIM1**). The receive signal level Q is programmable by three control bits LIM1.RIL(2:0) see **Table 50**. The number N can be set by an 8-bit register (PCD). The contents of the PCD register is multiplied by 16, which results in the number of pulse periods, i.e. the time which has to suspend until the alarm has to be detected. The programmable range is 16 to 4096 pulse periods. ETS300233 requires detection intervals of at least 1 ms. This time period results always in a LFA (Loss of Frame Alignment) before a LOS is detected.

- Recovery: In general the recovery procedure starts after detecting a logical one (digital receive interface) or a pulse (analog receive interface) with an amplitude more than Q dB (defined by LIM1.RIL(2:0)) of the nominal pulse. The value in the 8-bit register PCR defines the number of pulses (1 to 255) to clear the LOS alarm.

If a loss-of-signal condition is detected in long-haul mode, the data stream can optionally be cleared automatically to avoid bit errors before LOS is indicated. The Selection is done by LIM1.CLOS = ´1´.

3.7.6 Receive Equalization Network

The OctalLIU™ automatically recovers the signals received on pins RL1 and RL2 in a range of up to -43 dB for E1 or -36 dB for T1/J1. The maximum reachable length with a 22 AWG twisted pair cable is about 1500 m for E1 and about 2000m (~6560 ft) for T1. The integrated receive equalization network recovers signals with up to -43 dB for E1 or -36 dB for T1/J1 of cable attenuation automatically. Noise filters eliminate the higher frequency part of the received signals. The incoming data is peak-detected and sliced to produce the digital data stream. The slicing level is software selectable in four steps (45%, 50%, 55%, 67%), see **Table 50**. For typical E1 applications, a level of 50% is used. The received data is then forwarded to the clock & data recovery unit.

Each of the OctalLIU™ line receivers use parameters which are internally stored in a ROM. With these parameters the maximum receiver sensitivity is only 33 dB in E1 mode.

It is also possible to use parameters stored in an internal RAM instead of those stored in the internal ROM. The RAM parameters must be loaded before activation of the lines. The RAM is accessible over the micro controller interface in the same way as the OctalLIU™ registers by using a special RAM access mode. All interface modes (Motorola, Intel, SPI or SCI) can be used for RAM access.

The activation of the RAM access mode, the load procedure of the RAM, the values of the RAM parameters and the deactivation of the RAM access mode to have access to the registers again are not described in the data sheet of the OctalLIU™.

The source code for loading the optimal parameters into the RAM is available on request. Use of these optimal parameters improves the maximum receiver sensitivity to 43 dB in E1 mode.

3.7.7 Receive Line Attenuation Indication

Status register RES reports the current receive line attenuation

- For E1 in a range from 0 to -43 dB in 25 steps of approximately 1.7 dB each.
- For T1/J1 in a range from 0 to -36 dB in 25 steps of approximately 1.4 dB each.

The least significant 5-bits of this register indicate the cable attenuation in dB. These 5-bits are only valid in combination with the most significant two bits (RES.EV(1:0) = ´01_b´).

3.7.8 Receive Clock and Data Recovery

The analog received signal on pins RL1 and RL2 is equalized and then peak-detected to produce a digital signal. The digital received signal on pins RDIP and RDIN is directly forwarded to the clock & data recovery. The so called DPLL (digital PLL) of the receive clock & data recovery extracts the route clock from the data stream received at the RL1/2 or ROID lines. The clock & data recovery converts the data stream into a dual-rail, unipolar bit stream. The clock and data recovery uses an internally generated high frequency clock out of the master clocking unit based on MCLK.

The intrinsic jitter generated in the absence of any input jitter is not more than 0.035 UI.

3.7.9 Receive Jitter Attenuator

The receive jitter attenuator is based on the DCO-R (digital clock oscillator, receive) in the receive path. Jitter attenuation of the received data is done in the dual receive elastic buffer. The working clock is an internally generated high frequency clock based on the clock provided on pin MCLK. The jitter attenuator meets the E1 requirements of ITU-T I.431, G. 736 to 739, G.823 and ETSI TBR12/13 and the T1 requirements of AT&T PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431, G.703 and G. 824.

The internal PLL circuitry DCO-R generates a "jitter-free" output clock which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock. The receive jitter attenuator can be synchronized

either on the extracted receive clock RCLK or on a 2.048 MHz/8 kHz or 1.544 MHz/8 kHz clock provided on pin SYNC (8 kHz in master mode only). The jitter attenuated DCO-R output clock can be output on pin RCLK and FCLKR. Optionally an 8 kHz clock is provided on pin SEC/FSC.

For jitter attenuation the received data is written into the receive elastic buffer with the recovered clock sourced by the clock & data recovery and are read out with the de-jittered clock sourced by DCO-R.

If the receive elastic buffer is read out directly with the recovered receive clock, no jitter attenuation is performed.

If the receive elastic buffer is read out with the receive framer clock FCLKR, the receive elastic buffer performs a clock adoption from the recovered receive clock to FCLKR.

The DCO-R circuitry attenuates the incoming jittered clock starting at its corner frequency with 20 dB per decade fall-off. Wander with a jitter frequency below the corner frequency is passed unattenuated. The intrinsic jitter in the absence of any input jitter is < 0.02 UI.

The corner frequency of the DCO-R can be configured in a wide range, see **Table 18** and **Figure 23**. The jitter attenuator PLL in the transmit path, so called as DCO-X, is equivalent to the DCO-R so that the principle for its configuring is the same.

Table 18 Overview DCO-R (DCO-X) Programming

CMR6.DCOCOMPN	CMR2.ECFAR (CMR2.ECFAX)	LIM2.SCF (CMR6.SCFX)	CMR3.CFAR(3:0) (CMR3.CFAX(3:0))	CMR4.IAR(3:0) (CMR5.IAX(4:0))	Corner-frequencies of DCO-R (DCO-X) E1 / T1
X	0	0	Not used	Not used	2 Hz / 6 Hz
X	0	1	Not used	Not used	0.2 Hz / 0.6 Hz
0	1	X	7_H´ ´4_H´	Not used	0.2 Hz / 0.6 Hz 2 Hz / 6 Hz
1	1	X	´0_H´ ...´F_H´ , used as proportional parameter ´9_H´ ´8_H´ ´6_H´ ´4_H´	´00_H´ ...´$1F_H$´ used as integral parameter ´19_H´ ´13_H´ ´12_H´ ´$0F_H$´	Range 0.2 Hz ... 20 Hz 0.2 Hz 0.6 Hz 2 Hz 6Hz

After reset the corner frequencies are 2 Hz in E1 and 6 Hz in T1/J1 mode and can be switched to 0.2 Hz in E1 mode or 0.6 Hz n T1 mode by setting the register bit LIM2.SCF for the DCO-R or the register bit CMR5.SCFX for the DCO-X respectively. A logical table builds the integral (I) and proportional (P) parameter for the PI filter of the DCO-R or DCO-X, see **Figure 23**.

If the register bits CMR2.ECFAR or CMR2.ECFAX are set for the DCO-R or the DCO-X respectively, the corner frequencies can be configured in a range between 2 Hz and 0.2 Hz using the register bits CMR3.CFAR(3:0) or CMR3.CFAX(3:0) respectively, see **CMR3**, **CMR4** and **CMR5**. A logical table builds the integral and proportional parameter for the PI filter of the DCO-R or DCO-X out of the settings in CMR3.CFAR(3:0) or CMR3.CFAX(3:0) respectively.

If additionally to CMR2.ECFAR or CMR2.ECFAX the bit CMR6.DCOCOMPN (**CMR6**) is set, which is valid for the DCO-R and the DCO-X, the corner frequencies and attenuation factors can be programmed in a wide range using the register bits CMR3.CFAR(3:0) and CMR4.IAR(4:0) for the DCO-R and CMR3.CFAX(3:0) and CMR5.IAX(4:0) for the DCO-X. The settings in CMR3.CFAR(3:0)/CFAX(3:0) build the proportional parameter, the settings in CMR4.IAR(4:0) and CMR5.IAX(4:0) build the integral parameter for the PI filters, independent from another.

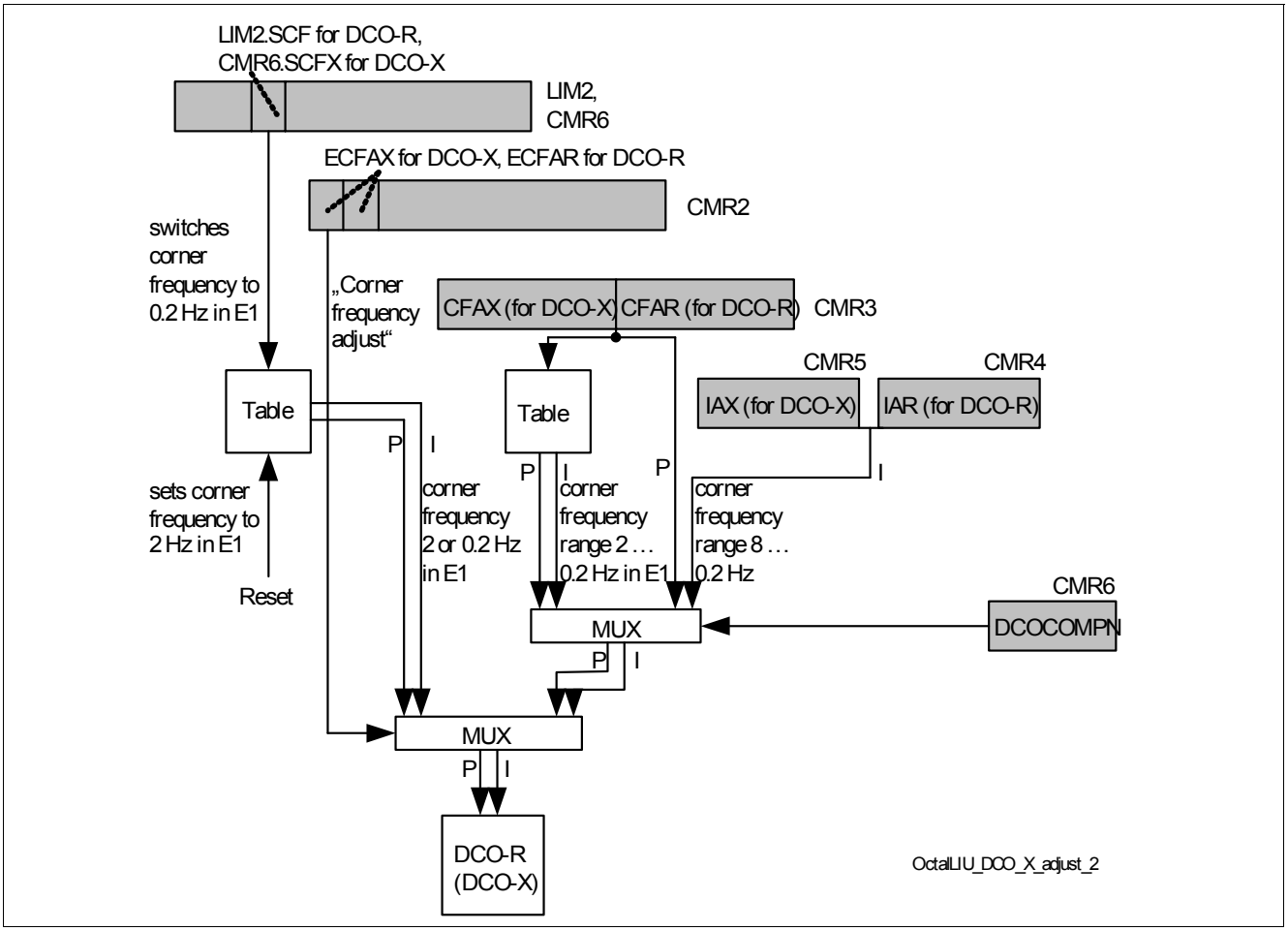


Figure 23 Principle of Configuring the DCO-R and DCO-X Corner Frequencies

The DCO-R reference clock is watched: If one, two or three clock periods of the 2.048 MHz (1.544 MHz in T1/J1 mode) clock at pin SYNC or RCLKI (in single rail digital line interface mode) are missing the DCO-R regulates it´s output frequency. If four or more clock periods are missing

- The DCO-R circuitry is automatically centered to the nominal bit rate if the center function of DCO-R is enabled by CMR2.DCF = ´0´.
- The actual DCO-R output frequency is “frozen” if the center function of DCO-R is disabled by CMR2.DCF = ´1´.

The receive jitter attenuator works in two different modes, selected by the multiplexer “C” in **Figure 17**:

- Slave mode: In slave mode (LIM0.MAS = ´0´) the DCO-R is synchronized on the recovered route clock. In case of loss of signal (LOS) the DCO-R switches automatically to Master mode. The frequency at the pin SYNC must be 2.048 MHz (1.544 MHz). If bit CMR1.DCS is set automatic switching from the recovered route clock to SYNC is disabled.
- Master mode: In master mode (LIM0.MAS = ´1´) the DCO-R is in free running mode if no clock is supplied on pin SYNC. If an external clock on the SYNC input is applied, the DCO-R synchronizes to this input. The external frequency can be 2.048 MHz (1.544 MHz) for IPC.SSYF = ´0´ or 8.0 kHz for IPC.SSYF = ´1´.

The following table **Table 19** shows this modes with the corresponding synchronization sources.

Table 19 Clocking Modes of DCO-R

Mode	Internal LOS Active	SYNC Input	System Clocks generated by DCO-R
Master	Independent	Fixed to V_{DD}	DCO-R centered, if CMR2.DCF = ´0´. (CMR2.DCF should not be set), see also **CMR2**
Master	Independent	2.048 MHz (E1) or 1.544 MHz (T1)	Synchronized to SYNC input (external 2.048 MHz or 1.544 MHz, IPC.SSYF = ´0´), see also **IPC**
Master	Independent	8.0 kHz	Synchronized to SYNC input (external 8.0 kHz, IPC.SSYF = ´1´, CMR2.DCF = ´0´)
Slave	No	Fixed to V_{DD}	Synchronized to recovered line clock
Slave	No	2.048 MHz (E1) or 1.544 MHz (T1)	Synchronized to recovered line clock
Slave	Yes	Fixed to V_{DD}	CMR1.DCS = ´0´: DCO-R is centered, if CMR2.DCF = ´0´. (CMR2.DCF should not be set)
			CMR1.DCS = ´1´: Synchronized on recovered line clock
Slave	Yes	2.048 MHz	CMR1.DCS = ´0´: Synchronized to SYNC input (external 2.048 MHz or 1.544 MHz)
			CMR1.DCS = ´1´: Synchronized on recovered line clock

The receive clock output RCLK of every channel can be switched between 2 sources, see multiplexer “D” in **Figure 17**:

- If the DCO-R is the source of RCLK the following frequencies are possible: 1.544, 3.088, 6.176, and 12.352 in T1/J1 mode and 2.048, 4.096, 8.192, and 16.384 MHz in E1 mode. Controlling of the frequency is done by the register bits CMR4.RS(1:0).
- If the recovered clock out (of the clock and data recovery) is the source of RCLK (see multiplexer “D” in **Figure 17**), only 2.048 MHz (1.544 MHz) is possible as output frequency.

3.7.9.1 Receive Jitter Attenuation Performance

For E1 the jitter attenuator meets the jitter transfer requirements of the ITU-T I.431 and G.735 to 739 (refer to **Figure 24**)

For T1/J1 the jitter attenuator meets the jitter transfer requirements of the PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431 and G.703 (refer to **Figure 25**).

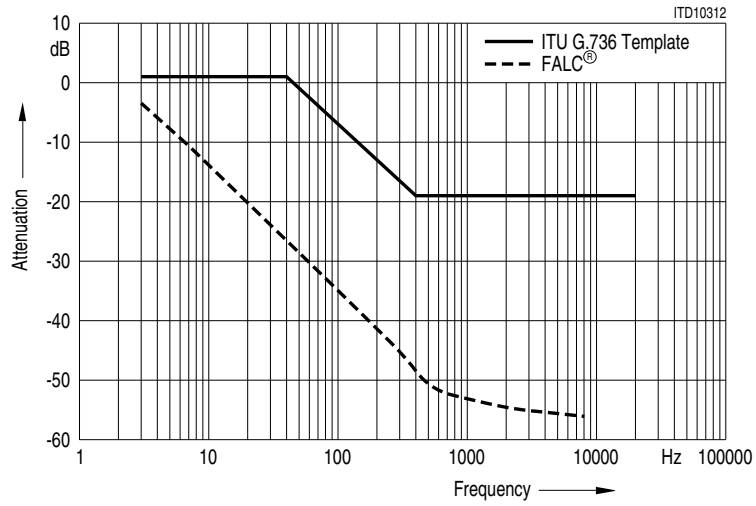


Figure 24 Jitter Attenuation Performance (E1)

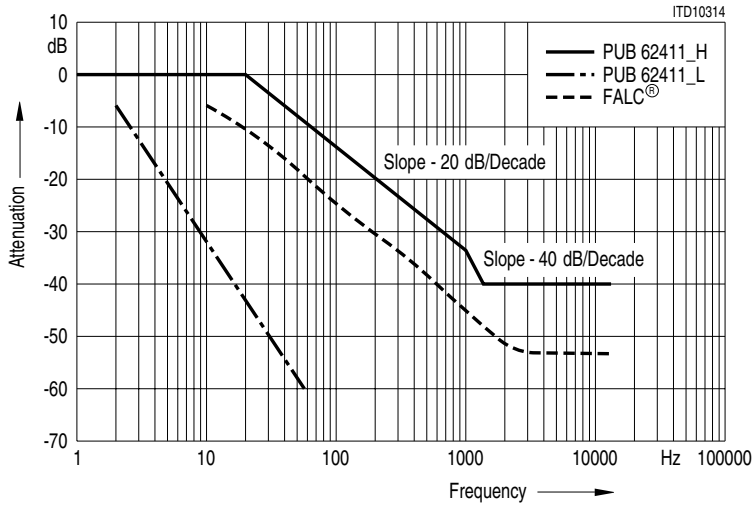


Figure 25 Jitter Attenuation Performance (T1/J1)

Also the requirements of ETSI TBR12/13 are satisfied. Insuring adequate margin against TBR12/13 output jitter limit with 15 UI input at 20 Hz the DCO-R circuitry starts jitter attenuation at about 2 Hz.

3.7.9.2 Jitter Tolerance (E1)

The OctalLIU™ receiver's tolerance to input jitter complies with ITU for CEPT applications.

Figure 26 and **Figure 27** shows the curves of different input jitter specifications stated below as well as the OctalLIU™ performance.

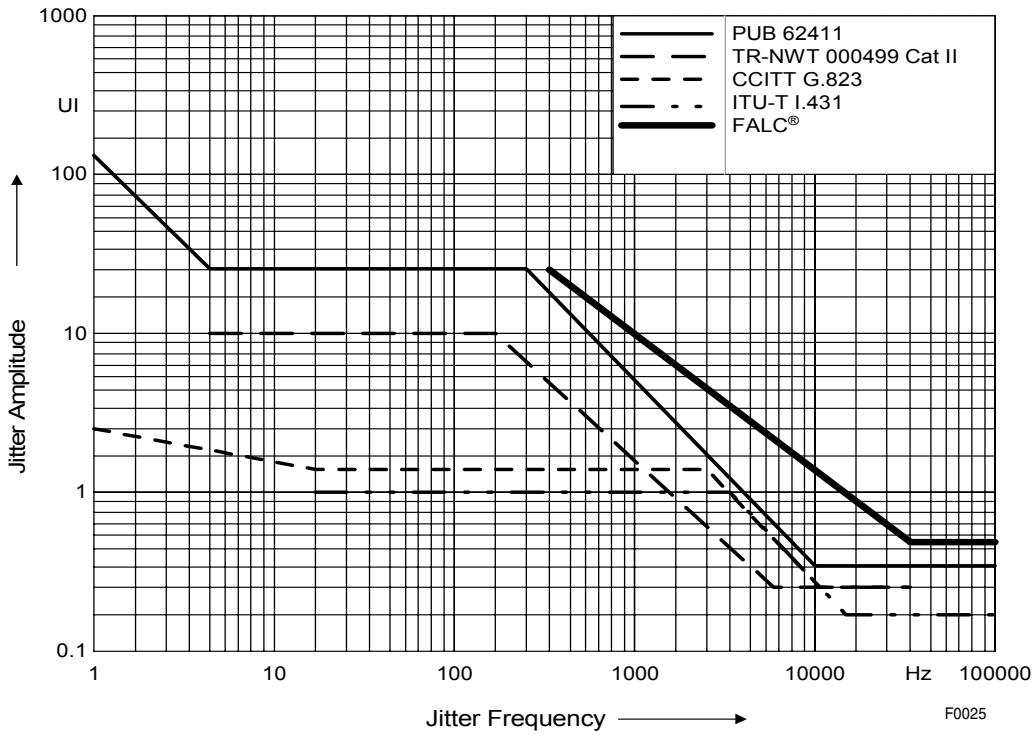


Figure 26 Jitter Tolerance (E1)

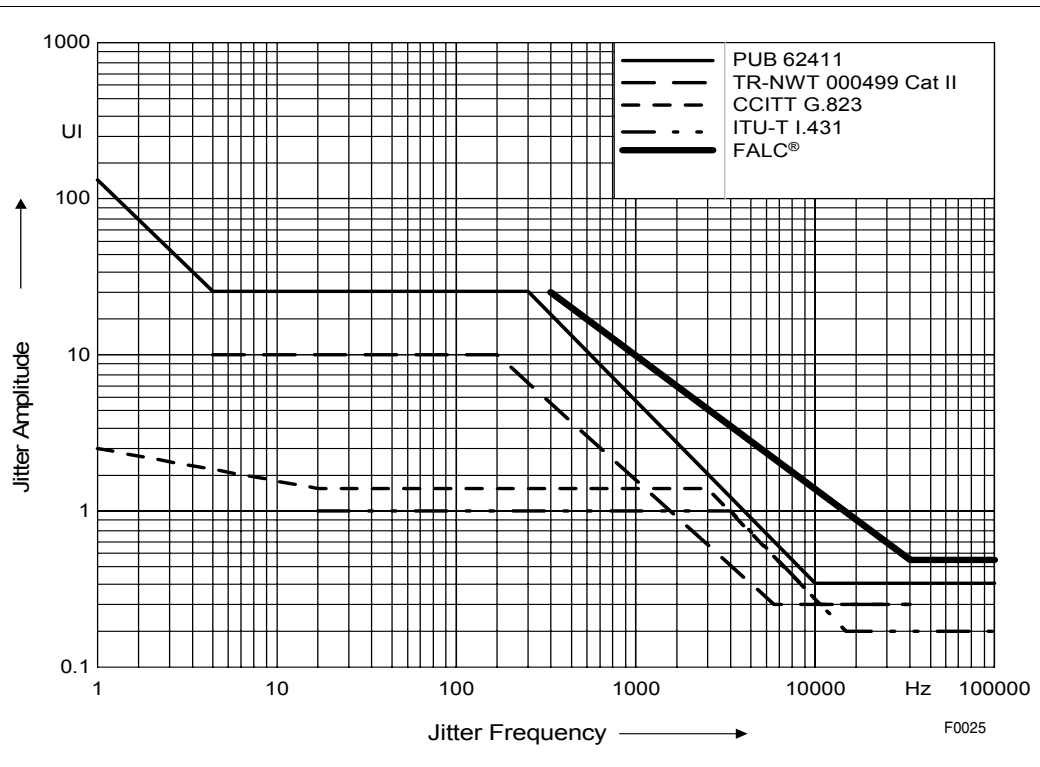


Figure 27 Jitter Tolerance (T1/J1)

3.7.9.3 Output Jitter

In the absence of any input jitter the OctalLIU™ generates the intrinsic output jitter, which is specified in the**Table 20** below.

Table 20 Output Jitter (E1)

Specification	Measurement Filter Bandwidth		Intrinsic Output Jitter (UI peak to peak)
	Lower Cutoff	Upper Cutoff	
ITU-T I.431	20 Hz	100 kHz	< 0.015
	700 Hz	100 kHz	< 0.015
ETSI TBR 12	40 Hz	100 kHz	< 0.11
PUB 62411	10 Hz	8 kHz	< 0.015
	8 Hz	40 kHz	< 0.015
	10 Hz	40 kHz	< 0.015
	Broadband		< 0.02

3.7.10 Dual Receive Elastic Buffer

For jitter attenuation the received data is written into the receive elastic buffer with the recovered clock sourced by the clock & data recovery and are read out with the de-jittered clock sourced by DCO-R, see **Figure 17**.

If the receive elastic buffer is read out directly with the recovered receive clock, no jitter attenuation is performed.

If the receive elastic buffer is read out with the receive framer clock FCLKR of the framer interface (FCLKR is input), the receive elastic buffer performs a clock adoption from the recovered receive clock to FCLKR.

The receive elastic buffer can buffer two data streams so that dual rail mode is possible at the receive framer interface (RDOP/RDON). In case of single rail mode on the receive framer interface, the bipolar violation signal BPV is buffered in the same way as the single rail signal and is supported at multi function pin RDON.

The size of the elastic buffer can be configured independently for the receive and transmit direction. Programming of the receive buffer size is done by DIC1.RBS(1:0), of the transmit buffer size by DIC1.XBS(1:0) see **Table 21**:

Table 21 Receive (Transmit) Elastic Buffer Modes

DIC1.RBS(1:0)	(DIC1.XBS(1:0))	Mode	Frame buffer size (bits)	Maximum of wander (UI = 648 ns)	Average delay after performing a slip	Slip Performance
00	10	E1	512	190	256	Yes
		T1/J1	396	140	193	
01	01	E1	256	100	128	
		T1/J1	193	74	96	
10	11 (short buffer mode)	E1	96	38	48	
		T1/J1				
11	00	E1	Bypass of the receive (transmit) elastic buffer			No
		T1/J1	Bypass of the receive (transmit) elastic buffer			

The functions are:

- Clock adoption between framer receive clock (FCLKR input) and internally generated route clock (recovered line clock), see **Chapter 3.7.9**.
- Compensation of input wander and jitter.
- Reporting and controlling of slips

In “one frame” or short buffer mode the delay through the receive buffer is reduced to an average delay of 128 or 46 bits. In bypass mode the time slot assigner is disabled. Slips are performed in all buffer modes except the bypass mode. After a slip is detected the read pointer is adjusted to one half of the current buffer size.

Figure 28 gives an idea of operation of the dual receive elastic buffer: A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the read pointer is within the slip limits (S +, S –). If a slip condition is detected, a negative slip (one frame or one half of the current buffer size is skipped) or a positive slip (one frame or one half of the current buffer size is read out twice) is performed at the system interface, depending on the difference between RCLK and the current working clock of the receive backplane interface. I.e. on the position of pointer R and W within the memory. A positive/negative slip is indicated in the interrupt status bits ISR3.RSP and ISR3.RSN.

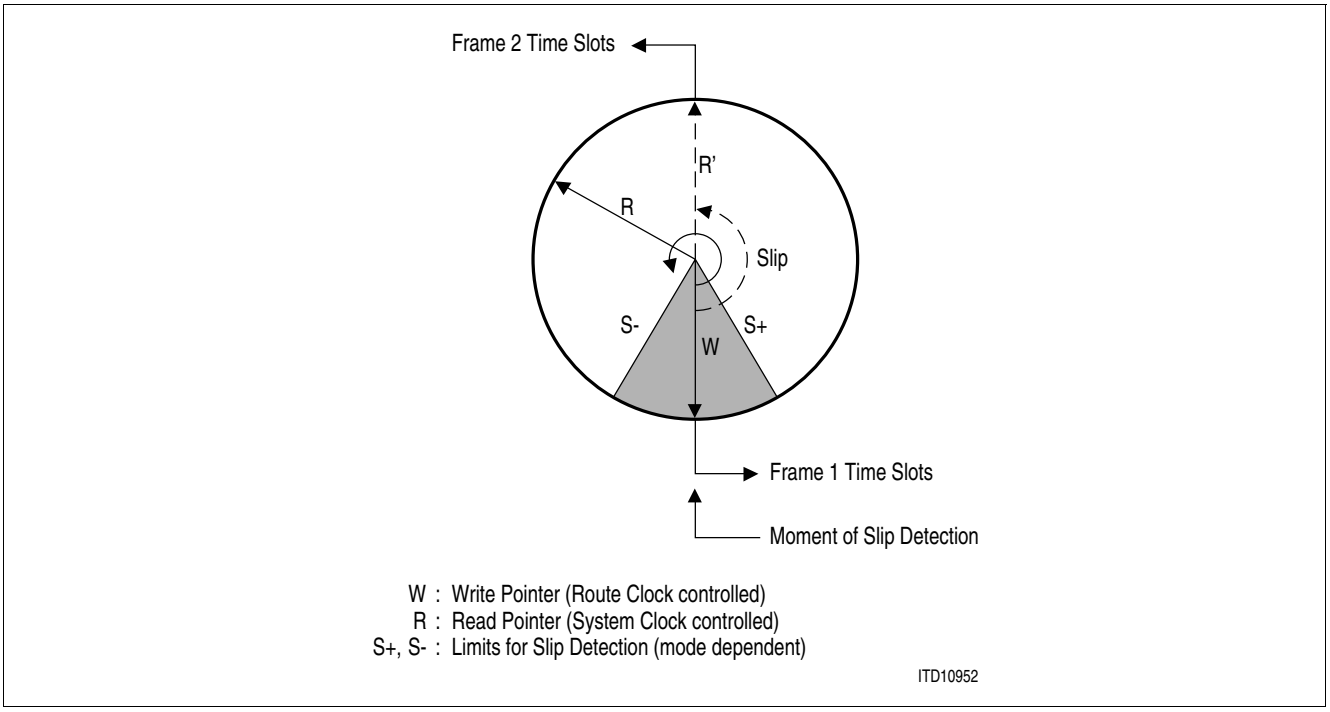


Figure 28 The Receive Elastic Buffer as Circularly Organized Memory

3.8 Additional Receiver Functions

3.8.1 Error Monitoring and Alarm Handling

The following error monitoring and alarm handling is supported by the OctalLIU™:

- Loss-Of-Signal: Detection and recovery is flagged by bit LSR0.LOS and ISR2.LOS.
- Transmit Line Shorted: Detection and release is flagged by bit LSR1.XLS and ISR1.XLSC
- Transmit Ones-Density: Detection and release is flagged by bit LSR1.XLO and ISR1.XLSC

Table 22 Summary of Alarm Detection and Release

Alarm	Detection Condition	Clear Condition
Loss-Of-Signal (LOS)	No transitions (logical zeros) in a programmable time interval of 16 to 4096 consecutive pulse periods. Programmable receive input signal threshold	Programmable number of ones (1 to 256) in a programmable time interval of 16 to 4096 consecutive pulse periods. A one is a signal with a level above the programmed threshold.
Transmit Line Short (XLS)	More than 3 pulse periods with highly increased transmit line current on XL1/2	Transmit line current limiter inactive, see also **Chapter 3.9.7**
Transmit Ones-Density (XLO)	32 consecutive zeros in the transmit data stream on XL1/2	Cleared with each transmitted pulse

3.8.2 Automatic Modes

The following automatic modes are performed by the OctalLIU™:

- Automatic clock source switching (see also: In slave mode (LIM0.MAS = ´0´) the DCO-R synchronizes to the recovered route clock. In case of loss-of-signal (LOS) the DCO-R switches to Master mode automatically. If bit CMR1.DCS is set, automatic switching from the recovered route clock to SYNC is disabled. See also **Table 19**.
- Automatic transmit clock switching, see **Chapter 3.9.3**.
- Automatic local and remote loop switching based on In-Band loop codes, see **Chapter 3.11.2**.

3.8.3 Error Counter

The OctalLIU™ offers two error counters where each of them has a length of 16 bit:

- Code Violation Counter, status registers CVCL and CVCH
- PRBS error counter, status registers BECL and BECH

The error counters are buffered. Buffer updating is done in two modes:

- One-second accumulation
- On demand by handshake with writing to the DEC register

In the one-second mode an internal/external one-second timer updates these buffers and resets the counter to accumulate the error events in the next one-second period. The error counter cannot overflow. Error events occurring during an error counter reset are not lost.

3.8.4 One-Second Timer

A one-second timer interrupt can be generated internally to indicate that the enabled alarm status bits or the error counters have to be checked. The one-second timer signal is output on port SEC/FSC if configured by GPC1.CSFP(1:0) (**GPC1**). Optionally synchronization to an external second timer is possible which has to be provided on pin SEC/FSC. Selecting the external second timer is done with GCR.SES.

3.9 Transmit Path

The transmit path of the OctalLIU™ is shown in **Figure 29**.

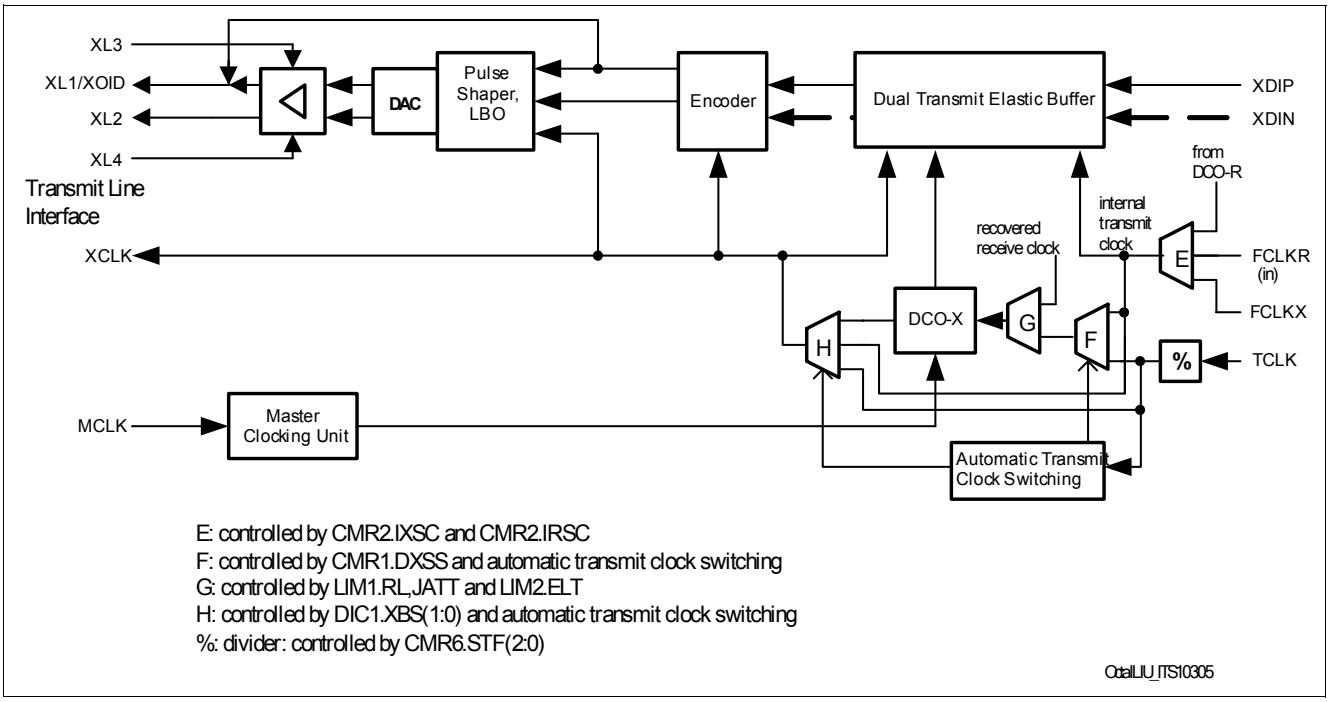


Figure 29 Transmit System of one Channel

The serial transmit bit stream (single rail or dual rail) is processed by the transmitter which has the following functions:

- AIS generation (blue alarm)
- Generation of In-band loop-up/-down code

3.9.1 Transmit Line Interface

The principle transmit line interface is shown in **Figure 30**. Two application modes are possible:

- For non-generic applications pins XL3 and XL4 can be left open. The serial resistance R_{SER} is dependent on the operation mode (E1/T1/J1) as shown in **Table 23**.
- For generic E1/T1/J1 applications with optimized return loss the transmit output resistance is configured by using the pins XL3 and XL4 as shown in **Figure 30**. The operation mode (E1/T1/J1) is selected by software (register bit PC6.TSRE) without the need for external hardware changes: Here R_{SER} is always 2 Ω, see **Table 23**.

In E1 mode the value of R_{SER} in **Table 23** is valid for both characteristic line impedances Z_0 = 120 Ω and Z_0 = 75 Ω.

Shorts between XL1 and XL2 cannot be detected, see **Chapter 3.9.7**.

The analog transmitter transforms the unipolar bit stream to ternary (alternate bipolar) return to zero signals of the appropriate programmable shape. The unipolar data is provided on pin XDI and the digital transmitter.

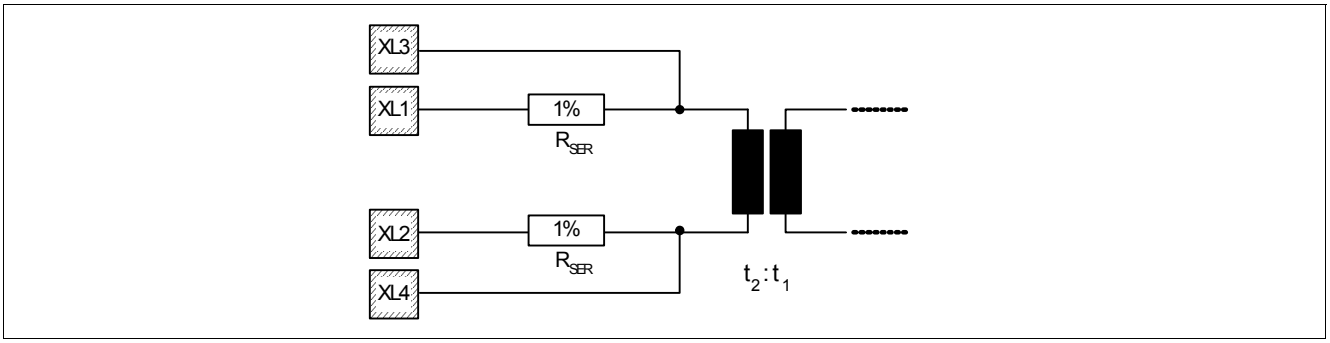


Figure 30 Transmit Line Interface

Table 23 Recommended Transmitter Configuration Values

R_{SER} (Ohm), accuracy +/- 1 %	Application Mode	PC6.TSRE	XL3, XL4	Operation Mode
2[1)]	Generic	1	Connected to R_{SER} and Xformer junction	E1
2		0		T1/J1
7.5	Non generic	0	Left open	E1
2		0	Left open	T1/J1

1) The values in this column refers to an ideal transformer without any parasitics. Any transformer resistance or other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

Similar to the receive line interface two different data types are supported:

- Ternary Signal: Single-rail data is converted into a ternary signal which is output on pins XL1 and XL2. Selection between B8ZS or simple AMI coding is provided.
- Unipolar data on port XOID is transmitted in CMI code with or without (DIC3.CMI) preprocessed by B8ZS coding or HDB3 precoding (MR3.CMI) to a fiber-optical interface. Clocking off data is done with the rising edge of the transmit clock XCLK (1544 kHz) and with a programmable polarity. Selection is done by MR0.XC1 = ´0´ and LIM1.DRS = ´1´.

An overview of the transmit line coding is given in **Table 12**.

3.9.2 Transmit Clock TCLK

The transmit clock input TCLK (multi function port) of the OctalLIU™ can be configured for 1.544, 3.088, 6.176, 12.352 and 24.704 MHz input frequency in T1/J1 mode and 2.048, 4.096, 8.192, 16.384 and 32.768 MHz input frequency in E1 mode. Frequency selection is done by the register bits CMR6.STF(2:0) (**CMR6**). See divider “%” in **Figure 29**.

3.9.3 Automatic Transmit Clock Switching

The transmit clock output XCLK can be derived from TCLK

- Directly. In this case the TCLK frequency must be 32.768 MHz in E1 or 24.704 MHz in T1/J1 mode. or
- With using the DCO-X, were the DCO-X reference is TCLK.

If TCLK fails, the transmit clock output XCLK will also fail. To avoid this, a so called automatic transmit clock switching can be enabled by setting the register bit CMR6.ATCS (**CMR6**). Then FCLKX will be used instead of TCLK if TCLK is lost. The transmit elastic buffer must be active. Automatically switching between TCLK and FCLKX is done in the following both cases:

- If the TCLK input is used directly as source for the transmit clock XCLK, the output of the DCO-X is not used. The DCO-X reference clock is FCLKX. If loss of TCLK is detected, the transmit clock XCLK will be switched automatically (if CMR6.ATCS = ´1´) to the DCO-X output which is synchronous to FCLKX (see multiplexer “H” in **Figure 29**). If XCLK was switched to the DCO-X output and TCLK becomes active, switching of XCLK (back)

to TCLK is automatically performed if CMR6.ATCS = ´1´. All switchings of XCLK between TCLK and the DCO-X output are shown in the interrupt status bit ISR7.XCLKSS0 which is masked by IMR7.XCLKSS0. These kinds of switching cannot be done in general without causing phase jumps in the transmit clock XCLK. Additionally after loss of TCLK the transmit clock XCLK is also lost during the “detection time” for loss of TCLK and the transmit pulses are disturbed. If CMR6.ATCS is cleared, TCLK is used (again) as source for the transmit clock XCLK, independent if TCLK is lost or not. The interrupt status bit ISR7.XCLKSS0 will be set also.

- If the transmit clock XCLK is sourced by the DCO-X output and the DCO-X reference clock is TCLK, the DCO-X reference will be switched automatically (if CMR6.ATCS = ´1´) to FCLKX (see multiplexer “F” in **Figure 29**) after a loss of TCLK was detected. If the DCO-X reference was switched to FCLKX and TCLK becomes active, switching of the reference (back) to TCLK is automatically performed if CMR6.ATCS = ´1´. All switchings of the reference between TCLK and FCLKX are shown in the interrupt status bit ISR7.XCLKSS1 which is masked by IMR7.XCLKSS1. For these kinds of automatically switching, the transmit clock XCLK fulfills the jitter-, wander- and frequency deviation- requirements as specified for E1/T1 after the clock source of the DCO-X was changed. If CMR6.ATCS is cleared, TCLK is used (again) as reference for the DCO-X, independent if TCLK is lost or not. The interrupt status bit ISR7.XCLKSS1 will be set also.

The status register bits CLKSTAT.TCLKLOS and CLKSTAT.FCLKXLOS (**CLKSTAT**) show if the appropriate clock is actual lost or not, so together with ISR7.XCLKSS1 and ISR7.XCLKSS0 the complete information regarding the current status of the transmit clock system is provided.

3.9.4 Transmit Jitter Attenuator

The transmit jitter attenuator is based on the so called DCO-X (digital clock oscillator, transmit) in the transmit path. Jitter attenuation of the transmit data is done in the transmit elastic buffer, see **Figure 29**. The DCO-X circuitry generates a "jitter-free" transmit clock and meets the E1 requirements of ITU-T I.431, G. 736 to 739, G.823 and ETSI TBR12/13 and the T1 requirements of AT&T PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431, G.703 and G. 824. The DCO-X circuitry works internally with the same high frequency clock as the DCO-R. It synchronizes either to the working clock of the transmit system interface (internal transmit clock) or the clock provided on multi function pin TCLK or the receive clock RCLK (remote loop/loop-timed). The DCO-X attenuates the incoming jitter starting at its corner frequency with 20 dB per decade fall-off. With the jitter attenuated clock, which is directly depending on the phase difference of the incoming clock and the jitter attenuated clock, data is read from the transmit elastic buffer (512/386 bit) or from the JATT buffer (512/386 bit, remote loop), see **Figure 31**. Wander with a jitter frequency below the corner frequency is passed transparently.

The dual transmit elastic buffer can buffer two data streams so that dual rail mode is possible at the transmit framer interface (XDIP/XDIN).

The DCO-X is equivalent to the DCO-R so that the principle for its configuring is the same, see **Figure 23** and **CMR3**, **CMR4** and **CMR5**.

The DCO-X reference clock is monitored: If one, two or three clock periods of the 2.048 MHz (1.544 MHz in T1/J1 mode) clock at FCLKX are missing the DCO-X regulates it´s output frequency. If four or more clock periods are missing

- The DCO-X circuitry is automatically centered to the nominal frequency of 2.048 MHz (1.544 MHz in T1/J1) if the center function of DCO-X is enabled by CMR2.DCOXC = ´1´.
- The actual DCO-X output frequency is “frozen” if the center function of DCO-R is disabled by CMR2.DCOXC = ´0´.

The jitter attenuated clock is output on pin XCLK if the transmit jitter attenuator is enabled, see multiplexer “H” in **Figure 29**.

The transmit jitter attenuator can be disabled. In that case data is read from the transmit elastic buffer with the clock sourced on pin TCLK, see multiplexer “H” in **Figure 29**. Synchronization between FCLKX and TCLK has to be done externally.

In the loop-timed clock configuration (LIM2.ELT) the DCO-X circuitry generates a transmit clock which is frequency synchronized on RCLK, see **Figure 31** and multiplexers “G” and “F” in **Figure 29**. In this configuration the transmit elastic buffer has to be enabled.

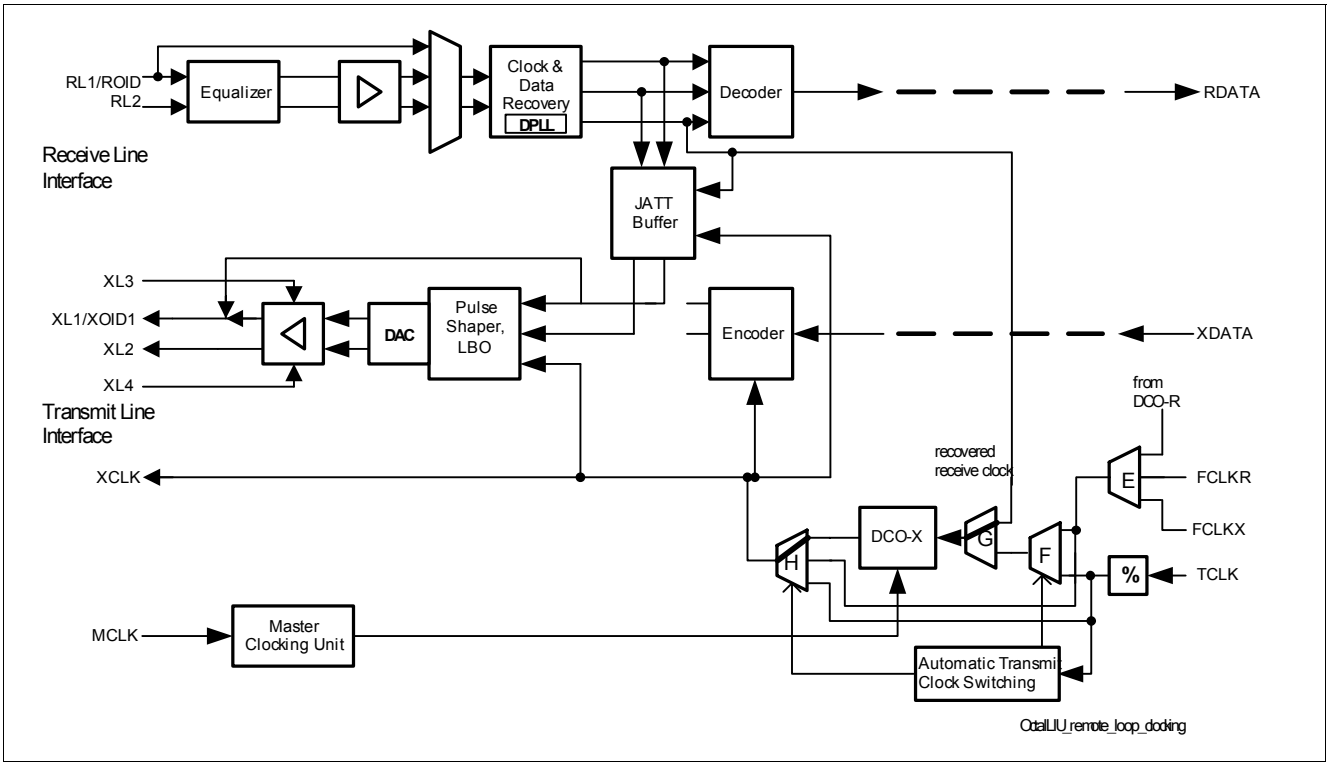


Figure 31 Clocking and Data in Remote Loop Configuration

3.9.5 Dual Transmit Elastic Buffer

The received single rail bit stream from pin XDI or dual rail bit stream from the pins XDIP and XDIN are optionally stored in the transmit elastic buffer, see **Figure 29**. The tansmit elastic buffer is organized as the receive elastic buffer. The functions are also equal to the receive side. Programming of the dual transmit buffer size is done by DIC1.XBS(1:0) in the same way as programming of the dual receive buffer size by DIC1.RBS(1:0), see **Table 21**:

The functions of the transmit buffer are:

- Clock adoption between framer transmit clock (FCLKX) and internally generated transmit route clock, see **Chapter 3.9.4**.
- Compensation of input wander and jitter.
- Reporting and controlling of slips

Writing of received data from XDIP/XDIN is controlled by the internal transmit clock. Selection of FCLKX or FCLKR is possible, see multiplexer “E” in **Figure 29**. (If the DCO-R output is selected, the DCO_R output is also output at FCLKR.)

Reading of stored data is controlled by the clock generated either by the DCO-X circuitry or the externally generated TCLK. With the de-jittered clock data is read from the dual transmit elastic buffer and are forwarded to the transmitter. Reporting and controlling of slips is done according to the receive direction. Positive/negative slips are reported in interrupt status bits ISR4.XSP and ISR4.XSN. If the transmit buffer is bypassed data is directly transferred to the transmitter.

3.9.6 Programmable Pulse Shaper and Line Build-Out

The transmitter includes a programmable pulse shaper to generate transmit pulse masks according to:

- For T1: FCC68; ANSI T1. 403 1999, figure 4; ITU-T G703 11/2001, figure 10 (for different cable lengths), see **Figure 56** and **Figure 33** for measurement configuration were R_{load} = 100 Ω
- For E1: ITU-T G703 11/2001, figure 15 (for 0 m cable length) see **Figure 55**; ITU-T G703 11/2001, figure 20 (for DCIM mode), see **Figure 32** for measurement configuration were R_{load} = 120 Ω or R_{load} = 75 Ω

The transmit pulse shape (U_{PULSE}) is programmed either

- By the registers XMP(2:0) compatible to the QuadLIU™, see **Table 24** and **Table 25**, if the register bit XPM2.XPDIS is cleared, see **XPM2**
- Or by the registers TXP(16:1), see **TXP1**, if the register bit XPM2.XPDIS is set, see **Table 26** and **Table 27**. For more details see chapter “Operational Description”

To reduce the crosstalk on the received signals in long haul applications the OctalLIU™ offers the ability to place a transmit attenuator (Line Build-Out, LBO) in the data path. This is used only in T1 mode. LBO attenuation is selectable with the values 0, -7.5, -15 or -22.5 dB (register bits **LIM2**.LBO(2:1)). ANSI T1. 403 defines only 0 to -15 dB.

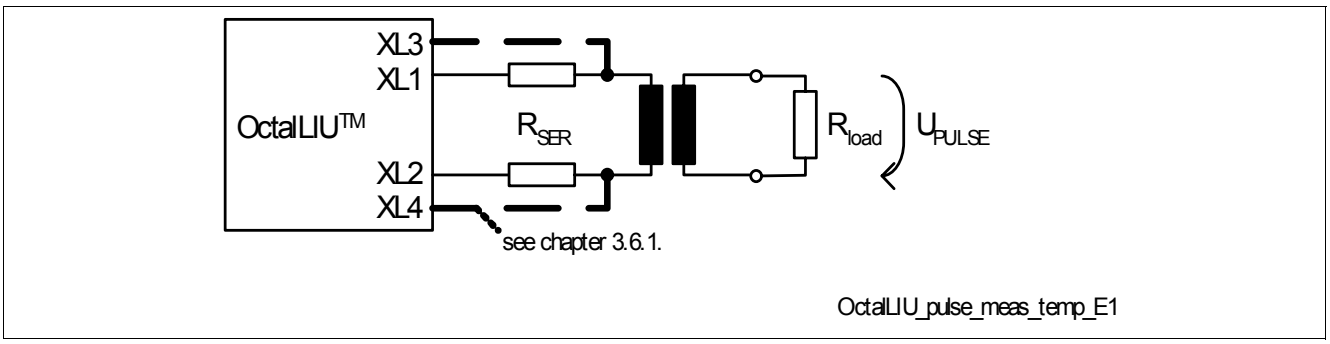


Figure 32 Measurement Configuration for E1 Transmit Pulse Template

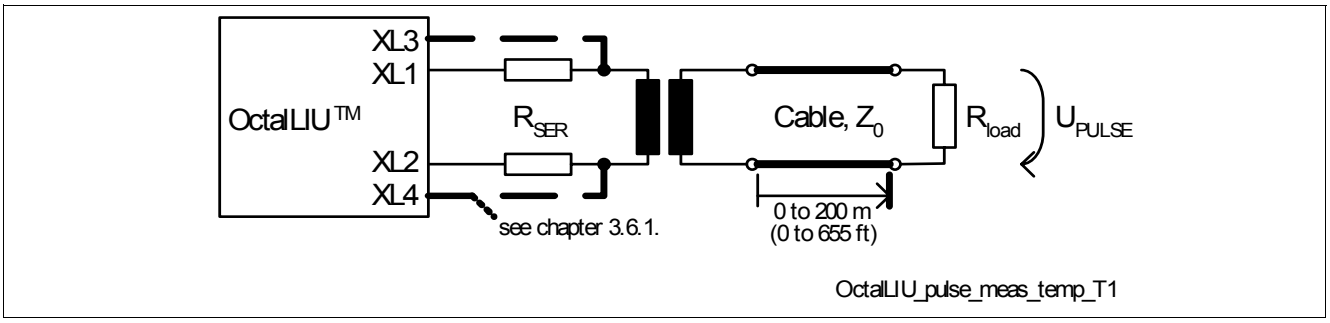


Figure 33 Measurement Configuration for T1/J1 Transmit Pulse Template

3.9.6.1 QuadLIU™ Compatible Programming

After reset XPM2.XPDIS is zero so that programming with XPM(2:0) is selected. The default setting after reset for the registers XMP(2:0) generates the E1 pulse shape, see **Table 25**, but with an unreduced amplitude. No reset value for T1 mode exists. So after switching into T1 mode, an explicit new programming like described in **Table 24** is necessary.

If LBO attenuation is selected, the programming of XPM(2:0) will be ignored. Instead the pulse shape programming is handled internally: The generated pulse shape before LBO filtering is the same as for T1 0 to 40 m.

The given values are optimized for transformer ratio: 1 : 2.4 and cable type AWG24 using transmitter configurations listed in **Table 23** and shown in **Figure 30**. The measurement configurations of **Figure 32** with R_{load} = 120 Ω and **Figure 33** with R_{load} = 100 Ω are used.

Table 24 Recommended Pulse Shaper Programming for T1/J1 with Registers XPM(2:0) (Compatible to QuadLIU)

LBO	Range	Range	XPM0	XPM1	XPM2
(dB)	(m)	(ft)	Hexadecimal		
0	0 to 40	0 to 133	D7	22	11
0	40 to 81	133 to 266	FA	26	11
0	81 to 122	266 to 399	3D	37	11

Table 24 Recommended Pulse Shaper Programming for T1/J1 with Registers XPM(2:0) (Compatible to QuadLIU (cont'd)**)**

LBO	Range	Range	XPM0	XPM1	XPM2
0	122 to 162	399 to 533	5F	3F	11
0	162 to 200	533 to 655	3F	CB	11
7.5	---		Are not taken into account: pulse shape generation is handled internally.		
15	---				
22.5	---				

Table 25 Recommended Pulse Shaper Programming for E1 with Registers XPM(2:0) (Compatible to OctalLIU™)

R_{SER}	Z_0	Transmit Line Interface Mode	XPM0	XPM1	XPM2
(Ω)	(Ω)		Hexadecimal		
7.5[1)]	120	Non generic	9C	03	00
7.5	75	Non generic	8D	03	00
---	Reset values		7B	03	40
7.5	DCIM Mode	Non generic	EF	BD	07

1) The values in this row refers to an ideal application without any parasitics. Any other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

3.9.6.2 Programming with TXP(16:1) Registers

By setting of register bit XPM2.XPDIS the pulse shape will be configured by the registers TXP(16:1) (**TXP1**). Every of these registers define the amplitude value of one sampling point in the symbol. A symbol is formed by 16 sampling points.

The default setting after reset for the registers TXP(16:1) generates also the E1 pulse shape (0m), but with an unreduced amplitude. (TXP(9:16) = ´00_H´; TXP(1:8) = ´38_H´= 56_D´) No reset value for T1 mode exists. So after switching into T1 mode, an explicit new programming like **Table 26** is necessary.

The pulse shape configuration will be done also by the registers TXP(16:1) if a LBO attenuation is selected. The pulse shape is then determined by both, the values of TXP(16:1) and the LBO filtering.

The given values in **Table 26** and **Table 27** are optimized for transformer ratio: 1 : 2.4; cable: AWG24 and configurations listed in **Table 23** and shown in **Figure 30**.

Table 26 Recommended Pulse Shaper Programming for T1 with registers TXP(16:1)

LBO	Range	Range	TXP values, decimal															
[dB]	[m]	[ft]	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0 to 40	0 to 133	46	46	46	44	44	44	44	44	16	-17	-14	-14	-4	-4	-4	-4
0	40 to 81	133 to 266	48	50	48	46	46	44	44	44	16	-17	-14	-14	-4	-4	-4	-4
0	81 to 122	266 to 399	56	58	54	52	48	48	48	48	16	-25	-17	-14	-4	-4	-4	-4
0	122 to 162	399 to 533	63	63	58	56	52	52	51	51	16	-34	-32	-17	-4	-4	-4	-4
0	162 to 200	533 to 655	63	63	63	58	50	50	50	50	50	-60	-26	-20	-12	-8	-6	-4
7.5	--	--	46	46	46	44	44	44	44	44	16	-17	-14	-14	-4	-4	-4	-4
155	--	--	46	46	46	44	44	44	44	44	16	-17	-14	-14	-4	-4	-4	-4
22.5	--	--	46	46	46	44	44	44	44	44	16	-17	-14	-14	-4	-4	-4	-4

Table 27 Recommended Pulse Shaper Programming for E1 with registers TXP(16:1)

R_{SER}	Z_0	Transmit Line Interface Mode	TXP values, decimal															
(Ω)	(Ω)		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
2[1)]	120	Generic	42	40	40	40	40	40	40	42	0	0	0	0	0	0	0	0
7.5	120	Non generic	63	57	57	57	57	57	57	57	-4	0	0	0	0	0	0	0
2	75	Generic	42	40	40	40	40	40	40	40	0	0	0	0	0	0	0	0
7.5	75	Non generic	60	58	58	58	58	58	58	58	0	0	0	0	0	0	0	0
--	Reset values		56	56	56	56	56	56	56	56	0	0	0	0	0	0	0	0
2	DCIM Mode	Generic	20	20	20	20	20	20	20	20	-20	-20	-20	-20	-20	-20	-20	-20
7.5	DCIM mode	Non generic	28	28	28	28	28	28	28	28	-28	-28	-28	-28	-28	-28	-28	-28

1) The values in this row refers to an ideal application without any parasitics. Any other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

3.9.7 Transmit Line Monitor

The transmit line monitor (see principle in **Figure 34**) compares the transmit line current on XL1 and XL2 with an on-chip transmit line current limiter. The monitor detects faults on the primary side of the transformer indicated by a highly increased transmit line current (more than 120 mA for at least 3 consecutive pulses sourced by VDDX) and protects the device from damage by setting the transmit line driver XL1/2 into high-impedance state automatically (if enabled by XPM2.DAXLT = ´0´, see **XPM2**). The current limiter checks the actual current value of XL1/2 and if the transmit line current drops below the detection limit the high-impedance state is cleared.

Two conditions are detected by the monitor:

- Transmit line ones density (more than 31 consecutive zeros) indicated by LSR1.XLO (**LSR1**).
- Transmit line high current indicated by LSR1.XLS.

In both cases a transmit line monitor status change interrupt is provided.

Shorts between XL1 or XL2 and V_{DD}, V_{DDC} or V_{DDP} are not detected.

Note that shorts between XL1 and XL2 were not detected. This way a short between XL1 and XL2 will not ham the device.

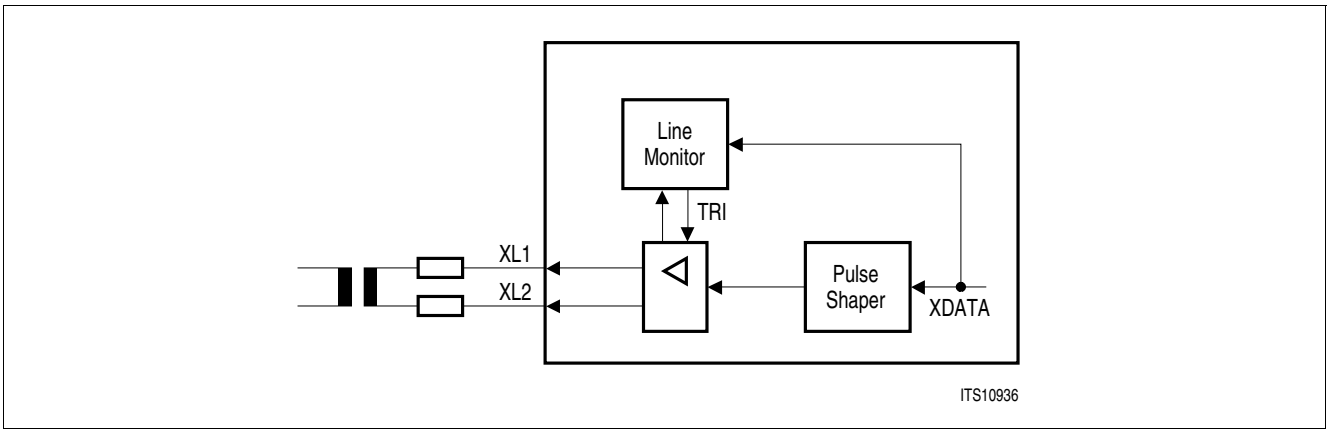


Figure 34 Transmit Line Monitor Configuration

3.10 Framer Interface

The framer interface of the OctalLIU™ is shown in **Figure 35**.

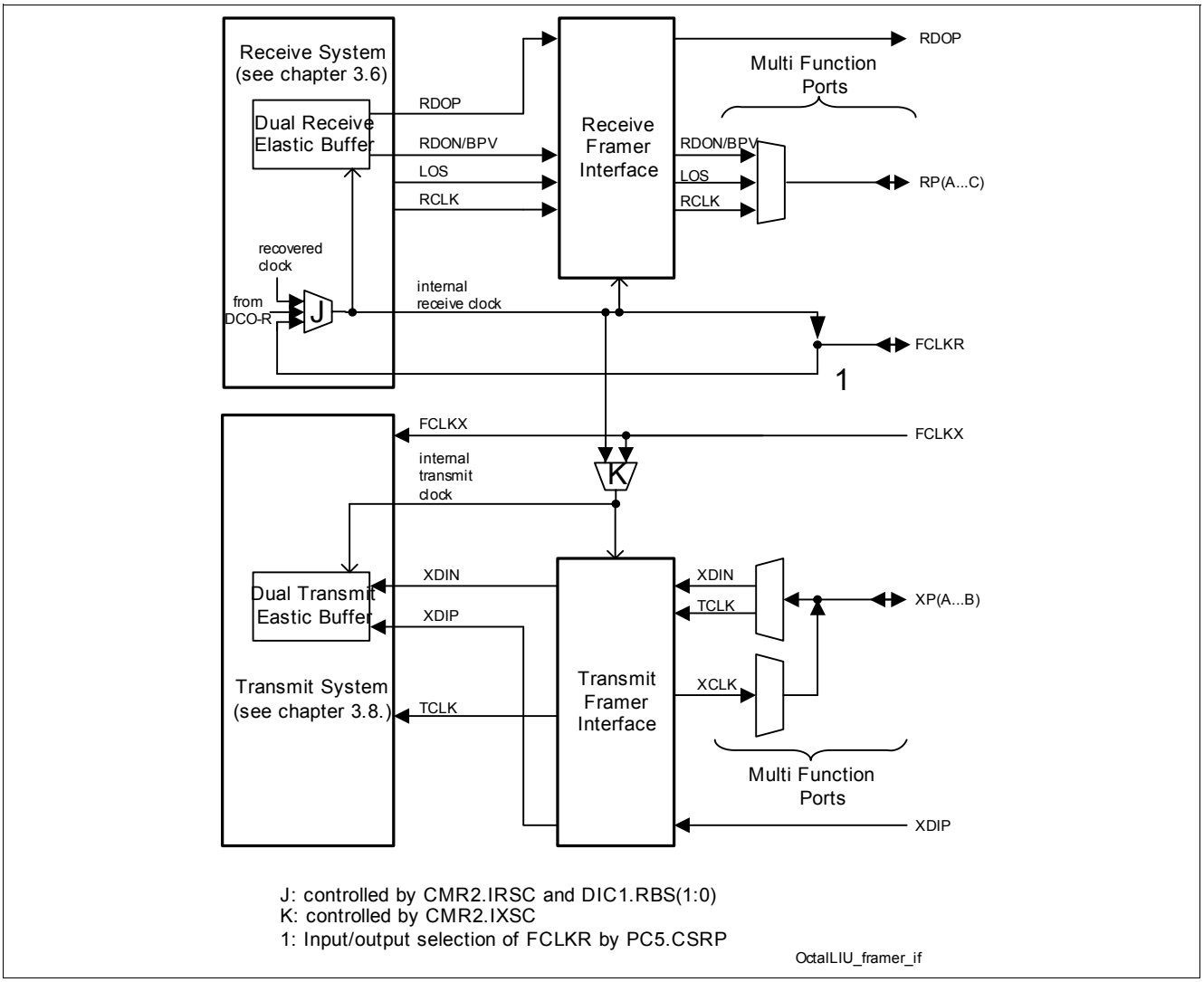


Figure 35 Framer Interface (shown for one channel)

Configuring of the framer interface consists on

- Configuration of the interface mode (single/dual rail)
- Configuration of the multi function ports, see **Chapter 3.12**

Selection of dual or single rail mode can be done in receive and transmit direction independent from each other.

In single rail mode of the receive direction (LIM3.DRR = ´0´, **LIM3**), the unipolar data is supported at RDOP and the bipolar violation (BPV) is supported at the receive multifunction pins. Therefore one of the three receive multifunction pins must be configured to RDON/BPV output (for example PC3.RPX3(3:0) = ´1110_B´), see**Table 29**, if BPV output is used exernally.

If dual rail mode is selected in receive direction by setting of register bit LIM3.DRR, the positive rail of the data is supported at RDOP and the negative rail of the data or is supported at the receive multi function pins. Therefore one of the three receive multifunction pins must be configured to RDON/BPV output, see**Table 29**.

Clocking of RDOP and RDON/BPV is done with the rising or falling edge of the internal receive clock, selected by DIC3.RESR. The internal receive clock can be sourced either

- By the receive clock RCLK of the receive system (CMR2.IRSC = ´1´, **CMR2**). To support the framer with these clock FCLKR output pin function must be selected by PC5.CSRP = ´1´ (**PC5**). or

- By the FCLKR input pin. In that case FCLKR input pin function must be selected by PC5.CSRP = ´0´ to use the receiver clock from the framer.

In single rail mode of the transmit direction (LIM3.DRX = ´0´, **LIM3**), the input for the unipolar data of the framer is XDIP.

If dual rail mode is selected in transmit direction by setting of register bit LIM3.DRX, the input for the positive rail of the data is XDIP and the input for the negative rail of the data is the multi function port XDIN. Therefore one of the both transmit multifunction ports must be configured to XDIN (for example PC1.XPX1(3:0) = ´1101_B´), see**Table 29**.

Clocking (sampling) of XDIP and XDIN is done with the rising or falling edge of the internal transmit clock, selected by DIC3.RESX. The internal transmit clock can be sourced either

- By the internal receive clock of the receive system (CMR2.IXSC = ´1´). To support the framer with these clock FCLKR output pin function must be selected by PC5.CSRP = ´1´. or
- By the FCLKX input pin (CMR2.IXSC = ´0´). In that case FCLKX is supported by the framer.

3.11 Test Functions

The following chapters describe the different test function of the OctalLIU™.

3.11.1 Pseudo-Random Binary Sequence Generation and Monitor

All bits of all slots in a E1T1/J1 frame are used for PRBS.

The OctalLIU™ has the ability to generate and monitor pseudo-random binary sequences (PRBS). The generated PRBS pattern is transmitted to the remote end on pins XL1/2 and can be inverted optionally. Generating and monitoring of PRBS pattern is done according to ITU-T O.150 and ITU-T O.151.

The PRBS monitor senses the PRBS pattern in the incoming data stream. Synchronization is done on the inverted and non-inverted PRBS pattern. The current synchronization status is reported in status and interrupt status registers. Enabled by bit LCR1.EPRM each PRBS bit error increments an error counter BEC (**BECL**). Synchronization is reached within 400 ms with a probability of 99.9% at a bit error rate of up to 10^{-1}.

The PRBS pattern (polynomials) can be selected to be 211-1, 215-1, 220-1or 223-1 by the register bits TPC0.PRP(1:0) and LCR1.LLBP (**LCR1**), see **Table 28**. For definition of this polynomials see the Standards ITU-T O.150, O.151. and TR62441. The polynomials 211-1 and 223-1 can be selected only if TPC0.PRM unequal ´00_B´.

Transmission of PRBS pattern is enabled by register bit LCR1.XPRBS. With the register bit LCR1.FLLB switching between not inverted and inverted transmit pattern can be done.

The receive monitoring of PRBS patterns is enabled by register bit LCR1.EPRM. In general, depending on bit LCR1.EPRM the source of the interrupt status bit ISR1.LLBSC changed, see register description. The type of detected PRBS pattern in the receiver is shown in the status register bits PRBSSTA.PRS. Every change of the bits PRS in PRBSSTA sets the interrupt bit ISR1.LLBSC if register bit LCR1.EPRM is set. No pattern is also detected if the mode “alarm simulation” is active.

The detection of all_zero or all_ones pattern is done over 12, 16, 21 or 24 consecutive bits, depending on the selected PRBS polynomial (211-1, 215-1, 220-1or 223-1 respectively). The detection of all_zero or all_ones is independent on LCR1.FLLB.

The distinction between all-ones and all-zeros pattern is possible by combination of.

- The information about the first reached PRBS status after the PRBS monitor was enabled (“PRBS pattern detected” or “inverted PRBS pattern detected”) with
- The status information “all-zero pattern detected” or “all-ones pattern detected”

If an “all-one” or an “all-zero” pattern is detected by the PRBS monitor, the interrupt status bit ISR1.LLBSC in E1 mode, or ISR3.LLBSC in T1/J1 mode respectively, is set not only once, but is set permanent.

Therefore, after reading of the interrupt status bit ISR1.LLBSC (E1 mode) or ISR3.LLBSC (T1/J1 mode), the appropriate interrupt routine should set the interrupt mask bits IMR1.LLBSC (E1 mode) or IMR3.LLBSC (T1/J1 mode) to ´1´, after an “all-one” or an “all-zero” pattern was indicated, to avoid permanent interrupts issued by the OctalLIU™. The PRBS status register bits PRBSSTA.PRS should be polled to detect changes in the pattern, for

example once per second, using the ISR3.SEC interrupt. In case PRBSSTA.PRS(2:1) is unequal ´11_B´, the interrupt mask bits should be cleared to return to normal operation.

Because every bit error in the PRBS sequence increments the bit error counter BEC, no special status information like “PRBS detected with errors” is given here.

Table 28 Supported PRBS Polynomials

TPC0.PRP(1:0)	TPC0.PRM	LCR1.LLBP	Kind of Polynomial	Comment
00	01 or 11	X	2^{11} -1	
01	01 or 11	X	2^{15} -1	
10	01 or 11	X	2^{20} -1	
11	01 or 11	X	2^{23} -1	
XX	00	0	2^{15} -1	SW compatible to QuadLIU
XX	00	1	2^{20} -1	

3.11.2 In-Band Loop Generation, Detection and Loop Switching

Detection and generation of In-band Loop code is supported by the OctalLIU™ on the line side and on the framer side independent from another.

The OctalLIU™ generates and detects unframed In-band codes where the complete data stream is used by the In-band signaling information.The so called loop-up code (for loop activation) and loop-down code (for loop deactivation) are recognized.

The maximum allowed bit error rate within the loop codes can be up to 10^{-2} for proper detection of the loop codes. One “In-band loop sequence” consists of a bit sequence of 51200 consecutive bits. The In-band loop code detection is based on the examination of such “In-band loop sequences”.

The following In-band loop code functionality is performed by the OctalLIU™:

- The necessary reception time of In-band loop codes until an automatic loop switching is performed is configured for the system side by the register bits INBLDTR.INBLDT(1:0) (**INBLDTR**). Configuring for the line side is done by INBLDTR.INBLDR(1:0). If for example INBLDTR.INBLDR(1:0) = ´00_B´ a time of 16 “In-band loop sequences” (16 x 51200 bits) is selected for the line side.
- The interrupt status register bits ISR6.(3:0) reflects the type of detected In-band loop code. Masking can be done by IMR6(3:0). The status bits are set after one “In-band loop sequence” is detected (no dependency on INBLDTR).
- Transmission of In-Band loop codes is enabled by programming MR3.XLD/XLU in E1 mode or MR5.XLD/XLU in T1/J1 mode. Transmission of codes is done by the OctalLIU™ lasting for at least 5 seconds.
- The OctalLIU™ also offers the ability to generate and detect flexible In-band loop-up and loop-down patterns (LCR1.LLBP = ´1´) (**LCR1**). Programming of these patterns is done in registers LCR2 and LCR3 (**LCR2**). The pattern length is individually programmable in length from 2 to 8 bits by LCR1.LAC(1:0) and LCR1.LDC(1:0). A shorter pattern can be inplemented by configuring a repeating pattern in the LCR2 and LCR3.
- Automatic loop switching (activation and deactivation, for remote loop, see **Chapter 3.11.3** and local loop, see **Chapter 3.11.4**) based on In-band Loop codes can be done. Two kinds of line loop back (LLB) codes are defined in ANSI-T1.403, 1999 in chapter 9.4.1.1 and 9.4.1.2. respectively. Automatic loop switching must be enabled through configuration register bits ALS.SILS for the In-Band Loop codes coming from the system side and ALS.LILS for the In-Band Loop codes coming from the line side respectively. Masking of ISR6.(3:0) for interrupt can be done by register bits IMR6.(3:0). The interrupt status register bits ISR6.(3:0) (**ISR6**) will be set to ´1´ if an appropriate In-Band code were detected, independent if automatic loop switching is enabled. (Because the controller knows if automatic loop switching is enabled, it knows if a loop is activated or not.) Code detection status only for the line side is displayed in E1 mode in status register bits LSR2.LLBDD / LLBAD and in T1/J1 mode in LSR1.LLBDD / LLBAD.

Only unframed In-Band loop code can be generated and detected.

Automatic loop switching is logically OR´d with the appropriate loop switching by register bits.

If a remote loop is activated by an automatic loop switching the register bit LIM0.JATT controls also if the jitter attenuator is active or not, see also **Figure 31**.

If ALS.LILS is set (**ALS**), the remote loop is activated after an activation In-Band loop code (see ANSI T1 404, chapter 9.4.1.1.) was detected from the line side and if the local loop is not activated by LIM0.LL = ´1´. The remote loop is deactivated after a deactivation In-Band loop code (see ANSI T1 404, chapter 9.4.1.2.) was detected from the line side. (But if the remote loop is additionally activated by LIM0.RL = ´1´ the remote loop is still active, because automatic loop switching is logically OR´d with the appropriate loop switching by register bits.).

If ALS.SILS is set, the local loop is activated after an activation In-Band loop code (see ANSI T1 404, chapter 9.4.1.1.) was detected from the system side. The local loop is deactivated after a deactivation In-Band loop code (see ANSI T1 404, chapter 9.4.1.2.) was detected from the system side. (But if the local loop is additionally activated by LIM0.LL = ´1´ the local loop is still active, because automatic loop switching is logically OR´d with the appropriate loop switching by register bits.).

ALS.SILS and ALS.LILS both must not be set to ´1´ simultaneous.

If ALS.SILS or ALS.LILS are set after an In-Band loop code was detected, no automatic loop switching is performed.

If ALS.LILS is cleared, an automatic activated remote loop is deactivated.

If ALS.SILS is cleared, an automatic activated local loop is deactivated.

The kind of detected In-Band loop codes is shown in the interrupt status register bits ISR6.(3:0).

To avoid deadlocks in the OctalLIU™ an activation of the remote loop is not possible by In-band loop codes if the local loop (see **Chapter 3.11.4**) is closed (LIM0.LL is set).

3.11.3 Remote Loop

In the remote loop-back mode the clock and data recovered from the line inputs RL1/2 or ROID are routed back to the line outputs XL1/2 or XOID through the analog or digital transmitter, see **Figure 36** and **Figure 31**. As in normal mode they are also sent to the framer interface. The remote loop-back mode is activated by

- Control bit LIM1.RL or
- After detection of the appropriate In-band loop code, if enabled by ALS.LILS and if LIM0.LL = ´0´ (**LIM0**) (to avoid deadlocks), see **Chapter 3.11.2**.

Received data can be looped with or without the jitter attenuator (JATT buffer) dependent on LIM1.JATT (**LIM1**).

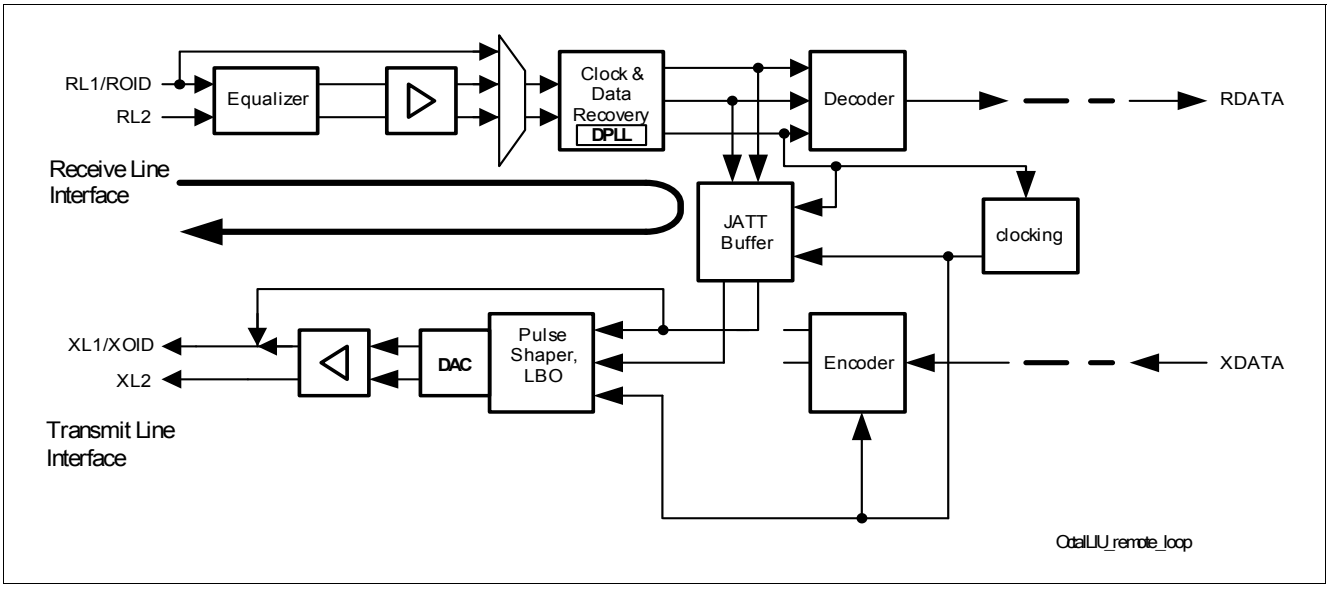


Figure 36 Remote Loop

3.11.4 Local Loop

The local loop-back is activated by

- The control bit LIM0.LL (**LIM0**).
- After detection of the appropriate In-band loop code, if enabled by ALS.SILS, see **Chapter 3.11.2**.

The local loop-back mode disconnects the receive lines RL1/2 or ROID from the receiver. Instead of the signals coming from the line the data provided by the framer interface is routed through the analog receiver back to the framer interface. However, the bit stream is transmitted undisturbed on the line at XL1/2. However, an AIS to the distant end can be enabled by setting MR1.XAIS = ´1´ without influencing the data looped back to the framer interface.

The signal codes for transmitter and receiver have to be identical.

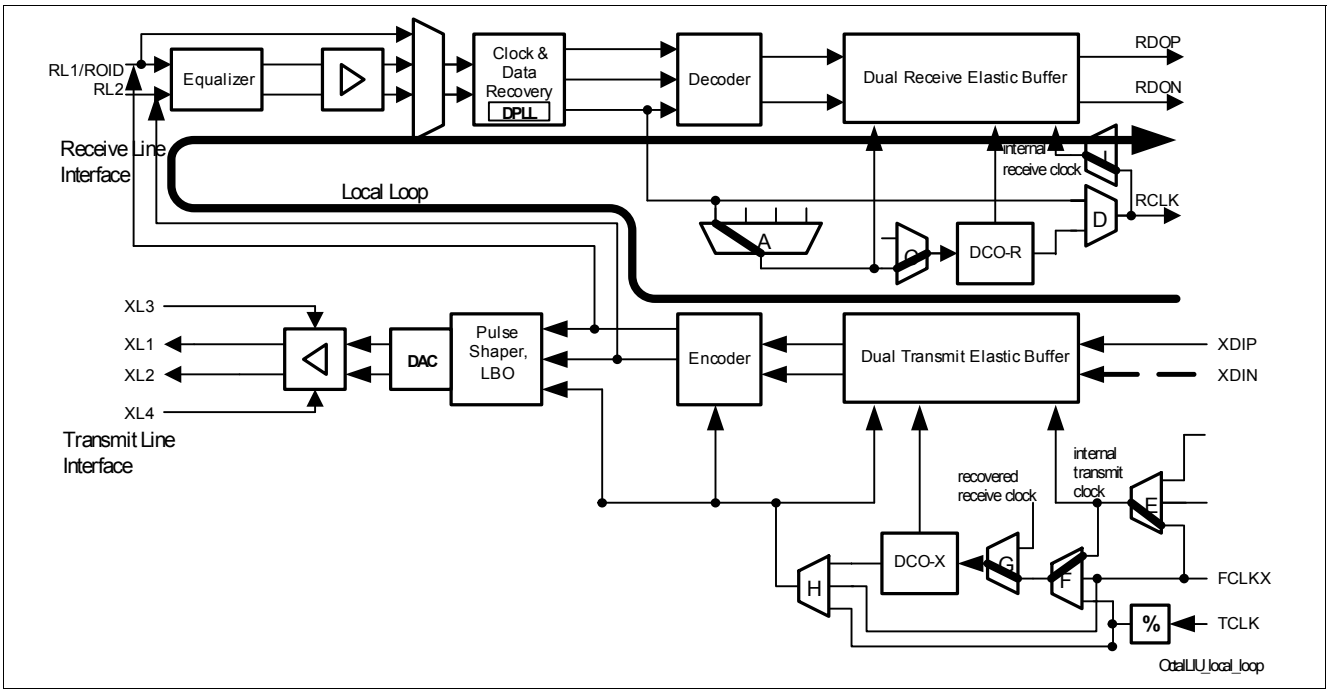


Figure 37 Local Loop

3.11.5 Payload Loop-Back

The payload loop-back is activated by setting MR2.PLB (**MR2**).

During activated payload loop-back the data stream is looped from the receiver section back to transmitter section. The looped data passes the complete receiver including the wander and jitter compensation in the receive elastic buffer and is output on pin RDO. Instead of the data an AIS signal (MR2.SAIS) can be sent to the framer interface.

If the PLB is enabled the transmitter and the data on pins XL1/2 or XDOP/XDON are clocked with FCLKR instead of FCLKX. All the received data is processed normally.

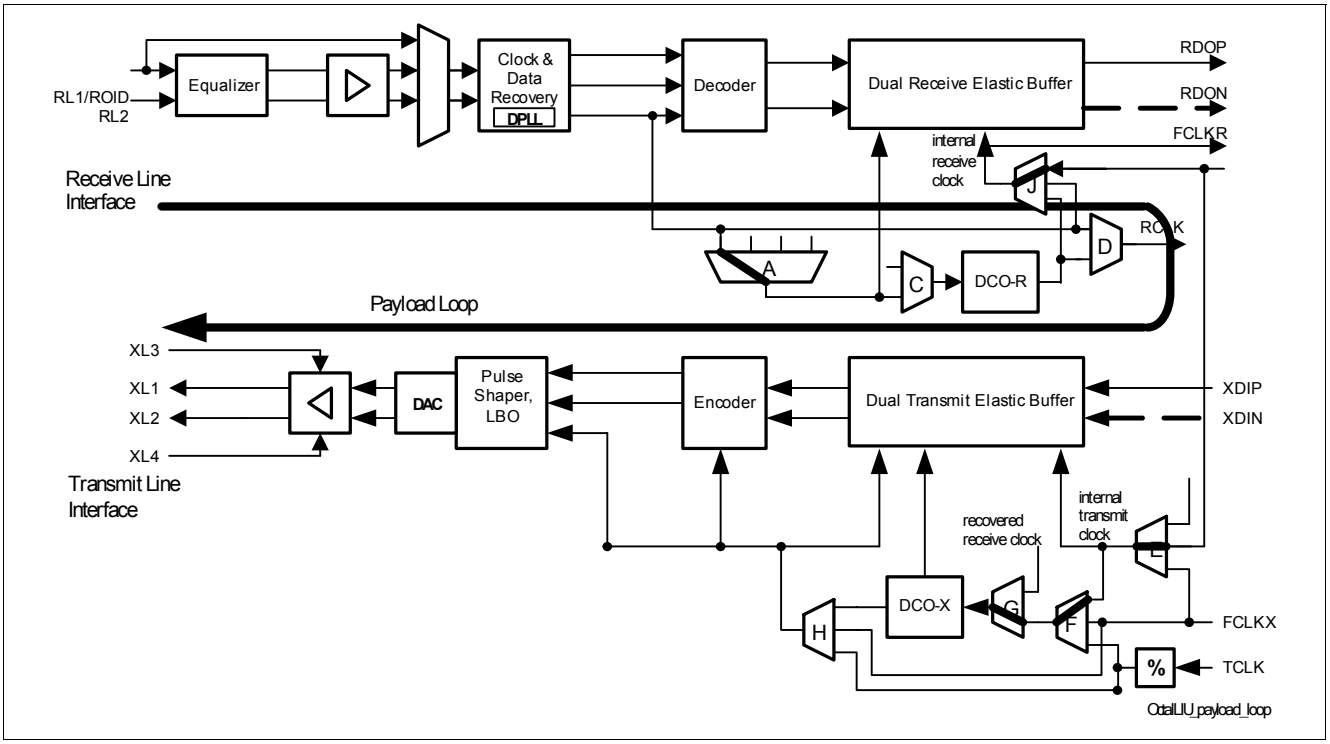


Figure 38 Payload Loop

3.11.6 Alarm Simulation

Alarm simulation does not affect the normal operation of the device. However, possible *real* alarm conditions are not reported to the micro controller or to the remote end when the device is in the alarm simulation mode.

The alarm simulation and setting of the appropriate status bists is initiated by setting the bit MR0.SIM. For details (differences between E1 and T1/J1 mode) see description in **MR0**. The following alarms are simulated:

- Loss-Of-Signal (LOS)
- Alarm Indication Signal (AIS)
- Code violation counter (HDB3 Code)

Error counting and indication occurs while this bit is set. After it is reset all simulated error conditions disappear, but the generated interrupt statuses are still pending until the corresponding interrupt status register is read. Alarms like AIS and LOS are cleared automatically. Interrupt status registers and error counters are automatically cleared on read.

3.12 Multi Function Ports

Several signals are available on the multi function ports, see **Table 29** and **PC1**. After reset, input function is selected (´0000_B´) with exception of the ports RPC were RCLK output is selected: The register bits PC3.RPC2 have the reset value ´FH´. (Note that PC5.CRP must be set to ´1´ for an active RCLK output. After reset PC5.CRP is ´0´ and RCLK is pulled up.)

Three multi function ports (MFP) for RX - so called as RPA, RPB, RPC - and two MFPs for TX - so called as XPA, XPB - are implemented for every channel. The port levels are reflected in the appropriate bits of the register MFPI, see **MFPI**.

The functions of RPA, RPB and RPC are configured by PC1.RPC1(3:0) , PC2.RPC2(3:0) and PC3.RPC3(3:0) respectively.The functions of XPA and XPB are configured by PC1.XPC1(3:0) and PC2.XPC2(3:0) respectively.

The actual logical state of the 5 multifunction ports can be read out using the register MFPI. This function together with static output signal options in **Table 29** offers general purpose I/O functionality on unused multi function port pins.

If a port is configured as GPOH or GPOL the port level is set fix to high or low-level respectively.

Each of the input functions may only be selected once in a channel except for the GPI functionality. No input function must be selected twice or more.

If RLT is selected, it should be assigned to RPC.

Table 29 Multi Function Port Selection

Selection	RFP Signal	Available on port	RFP Function	XFP Signal	Available on port	XFP Function
0000	Reserved	A, B, C	Reserved	Reserved	A, B	Reserved
0001	Reserved	A, B, C	Reserved	Reserved	A, B	Reserved
0010	Reserved	A, B, C	Reserved	Reserved	A, B	Reserved
0011	Reserved	A, B, C	Reserved	TCLK	A, B	Transmit clock input
0100	Reserved	A, B, C	Reserved	Reserved	A, B	Reserved
0101	Reserved	A, B, C	Reserved	Reserved	A, B	Reserved
0110	Reserved	A, B, C	Reserved	Reserved	A, B	Reserved
0111	Reserved	A, B, C	Reserved	XCLK	A, B	Transmit clock output
1000	RLT	A, B, C	Receive line termination; logically OR´d with LIM0.RTRS	XLT	A, B	Transmit line tristate control, high active
1001	GPI	A, B, C	General purpose input	GPI	A, B	General purpose input
1010	GPOH	A, B, C	General purpose output high	GPOH	A, B	General purpose output high
1011	GPOL	A, B, C	General purpose output low	GPOL	A, B	General purpose output low
1100	LOS	A, B, C	Loss of signal indication output	Reserved	A, B	Reserved
1101	RTDMT	A, B, C	Receive framer interface tristate for pins RDOP and RCLK; logically OR´d with DIC3.RRTRI	XDIN	A, B	Transmit data negative input
1110	RDON	A, B, C	Receive data negative output or bipolar violation output	$\overline{\text{XLT}}$	A, B	Transmit line tristate control, low active
1111	RCLK	A, B, C	RCLK output	Reserved	A, B	Reserved

4 Register Description

To maintain easy readability this chapter is divided into separate control register and status register sections.

The higher address part of all global registers is ´00_H´, that of the port (channel) specific ones include the channel number 0 to 7 and is marked in the following tables with ´xx_H´. So ´xx_H´ has the values ´00_H´ up to ´07_H´.

Notes

1. *“RES” in the register schematics means reserved, not reset. If these bits are written then the value must be ´0´.*
2. *In all bit fields used in the register schematics and also in the table descriptions the most significant bit is the left one and the least significant bit is the right one. Sometimes in the text a bit field with the name “bitfieldname” is denoted as <bitfieldname>(MSB:LSB). For example: In register GPC2 the bit fiield FSS consists on MDS(2:0).*

4.1 Detailed Register Description

Table 30 Registers Address Space

Module	Base Address	End Address	Note
Channel xx	$xx00_H$	$xxFF_H$	xx = 00H ... 07H

Table 31 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
CMDR	Command Register	$xx02_H$	90
IMR1	Interrupt Mask Register 1	$xx15_H$	91
MR0	Mode Register 0	$xx1C_H$	93
MR1	Mode Register 1	$xx1D_H$	95
MR2	Mode Register 2	$xx1E_H$	95
LOOP	Loop-Back Register	$xx1F_H$	96
MR4	Mode Register 4	$xx20_H$	97
MR5	Framer Mode Register 5	$xx21_H$	97
RC0	Receive Control 0	$xx24_H$	98
XPM0	Transmit Pulse Mask0	$xx26_H$	99
XPM1	Transmit Pulse Mask1	$xx27_H$	100
XPM2	Transmit Pulse Mask2	$xx28_H$	100
CCB1	Clear Channel Register 1	$xx2F_H$	101
MR3	Mode Register 3	$xx31_H$	102
LIM0	Line Interface Mode 0	$xx36_H$	103
LIM1	Line Interface Mode 1	$xx37_H$	105
PCD	Pulse Count Detection Register	$xx38_H$	106
PCR	Pulse Count Recovery	$xx39_H$	106
LIM2	Line Interface Mode 2	$xx3A_H$	107
LCR1	Loop Code Register 1	$xx3B_H$	108
LCR2	Loop Code Register 2	$xx3C_H$	110
DIC1	Digital Interface Control 1	$xx3E_H$	111
DIC2	Digital Interface Control 2	$xx3F_H$	112
DIC3	Digital Interface Control 3	$xx40_H$	112
CMR4	Clock Mode Register 4	$xx41_H$	114
CMR5	Clock Mode Register 5	$xx42_H$	115
CMR6	Clock Mode Register 6	$xx43_H$	116
CMR1	Clock Mode Register 1	$xx44_H$	117
CMR2	Clock Mode Register 2	$xx45_H$	118
CMR3	Clock Mode Register 3	$xx48_H$	121
PC1	Port Configuration 1	$xx80_H$	121
PC5	Port Configuration 5	$xx84_H$	124
PC6	Port Configuration 6	$xx86_H$	125
TPC0	Test Pattern Control Register 0	$xxA8_H$	134

Table 31 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
TXP1	TX Pulse Template Register 1	$xxC1_H$	134
ALS	Automatic Loop Switching Register	$xxD9_H$	139
IMR7	Interrupt Mask Register 7	$xxDF_H$	139
LIM3	LIU Mode Register 3	$xxE2_H$	140
RBD	Receive Buffer Delay	$xx49_H$	140
RES	Receive Equalizer Status	$xx4B_H$	141
LSR0	Line Status Register 0	$xx4C_H$	142
LSR1	Line Status Register 1	$xx4D_H$	143
LSR3	Line Status Register 3	$xx4E_H$	144
LSR2	Line Status Register 2	$xx4F_H$	146
CVCL	Code Violation Counter Lower Byte	$xx52_H$	147
CVCH	Code Violation Counter Higher Byte	$xx53_H$	148
BECL	PRBS Bit Error Counter Lower Bytes	$xx58_H$	149
BECH	PRBS Bit Error Counter Higher Bytes	$xx59_H$	150
ISR1	Interrupt Status Register 1	$xx69_H$	151
ISR2	Interrupt Status Register 2	$xx6A_H$	152
ISR3	Interrupt Status Register 3	$xx6B_H$	152
ISR4	Interrupt Status Register 4	$xx6C_H$	153
GIS	Global Interrupt Status Register	$xx6E_H$	154
MFPI	Multi Function Port Input Register	$xxAB_H$	156
ISR6	Interrupt Status Register 6	$xxAC_H$	157
ISR7	Interrupt Status Register 7	$xxD8_H$	158
PRBSSTA	PRBS Status Register	$xxDA_H$	159
CLKSTAT	Clock Status Register	$xxFE_H$	160
IMR2	Interrupt Mask Register 2	$xx16_H$	92
IMR3	Interrupt Mask Register 3	$xx17_H$	92
IMR4	Interrupt Mask Register 4	$xx18_H$	92
IMR6	Interrupt Mask Register 6	$xx1A_H$	92
IMR7	Interrupt Mask Register 7	$xxDF_H$	92
PC2	Port Configuration Register 2	$xx81_H$	123
PC3	Port Configuration Register 3	$xx82_H$	123
TXP2	TX Pulse Template Register 2	$xxC2_H$	135
TXP3	TX Pulse Template Register 3	$xxC3_H$	135
TXP4	TX Pulse Template Register 4	$xxC4_H$	135
TXP5	TX Pulse Template Register 5	$xxC5_H$	135
TXP6	TX Pulse Template Register 6	$xxC6_H$	135
TXP7	TX Pulse Template Register 7	$xxC7_H$	135
TXP8	TX Pulse Template Register 8	$xxC8_H$	135
TXP9	TX Pulse Template Register 9	$xxC9_H$	135
TXP10	TX Pulse Template Register 10	$xxCA_H$	135
TXP11	TX Pulse Template Register 11	$xxCB_H$	135

Table 31 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
TXP12	TX Pulse Template Register 12	$xxCC_H$	135
TXP13	TX Pulse Template Register 13	$xxCD_H$	135
TXP14	TX Pulse Template Register 14	$xxCE_H$	135
TXP15	TX Pulse Template Register 15	$xxCF_H$	135
TXP16	TX Pulse Template Register 16	$xxD0_H$	135
IPC	Interrupt Port Configuration	0008_H	90
CCB2	Clear Channel Register 2	30_H	102
CCB3	Clear Channel Register 3	31_H	102
LCR3	Loop Code Register 3	$3D_H$	110
GCR	Global Configuration Register	0046_H	120
VSTR	Version Status Register	$004A_H$	141
CIS	Channel Interrupt Status Register	$006F_H$	155
GPC1	Global Port Configuration 1	0085_H	125
GPC2	Global Port Configuration Register 2	$008A_H$	126
GCM1	Global Clock Mode Register 1	0092_H	127
GCM2	Global Clock Mode Register 2	0093_H	127
GCM3	Global Clock Mode Register 3	0094_H	129
GCM4	Global Clock Mode Register 4	0095_H	129
GCM5	Global Clock Mode Register 5	0096_H	130
GCM6	Global Clock Mode Register 6	0097_H	131
GCM7	Global Clock Mode Register 7	0098_H	132
GCM8	Global Clock Mode Register 7	0099_H	133
GIMR	Global Interrupt Mask Register	$00A7_H$	133
GIS2	Global Interrupt Status 2	$00AD_H$	157
GPC3	Global Port Configuration Register 3	$00D3_H$	135
GPC4	Global Port Configuration Register 4	$00D4_H$	136
GPC5	Global Port Configuration Register 5	$00D5_H$	137
GPC6	Global Port Configuration Register 6	$00D6_H$	138
INBLDTR	In-Band Loop Detection Time Register	$00D7_H$	138

The register is addressed wordwise.

Table 32 Registers Access Types

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
Basic Access Types			
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read/write virtual	rwv	Physically, there is no new register in the generated register file. The real readable and writable register resides in the attached hardware.	Register is read and writable by SW (same as rw type register)
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by SW is ignored by HW; that is, SW may write any value to this field without affecting HW behavior
read only	ro	Same as r type register	Same as r type register
read virtual	rv	Physically, there is no new register in the generated register file. The real readable register resides in the attached hardware.	Value written by SW is ignored by HW; that is, SW may write any value to this field without affecting HW behavior (same as r type register)
write	w	Register is written by software and affects hardware behavior with every write by software.	Register is writable by SW. When read, the register does not return the value that has been written previously, but some constant value instead.
write virtual	wv	Physically, there is no new register in the generated register file. The real writable register resides in the attached hardware.	Register is writable by SW (same as w type register)
read/write hardware affected	rwh	Register can be modified by hardware and software at the same time. A priority scheme decides, how the value changes with simultaneous writes by hardware and software.	Register can be modified by HW and SW, but the priority SW versus HW has to be specified. SW can read the register.

4.1.1 Control Registers

Command Register

CMDR	Offset	Reset Value
Command Register	$xx02_H$	00_H

7	6	5	4	3	2	1	0
Res	**RRES**	Res	**XRES**	Res			
	w		w				

Field	Bits	Type	Description
RRES	6	w	**Receiver Reset** The receive line interface except the clock and data recovery unit (DPLL) is reset. However the contents of the control registers is not deleted. A receiver reset should be made after switching from power down to power up (GCR.PD = ´1´ -> ´0´).
XRES	4	w	**Transmitter Reset** The transmit framer and transmit line interface excluding the system clock generator and the pulse shaper are reset. However the contents of the control registers is not deleted.

Interrupt Port Configuration

See **Chapter 3.5.3** and **Table 9**.

IPC	Offset	Reset Value
Interrupt Port Configuration	0008_H	00_H

7	6	5	4	3	2	1	0
VISPLL	Res				**SSYF**	**IC**	
rw					rw	rw	

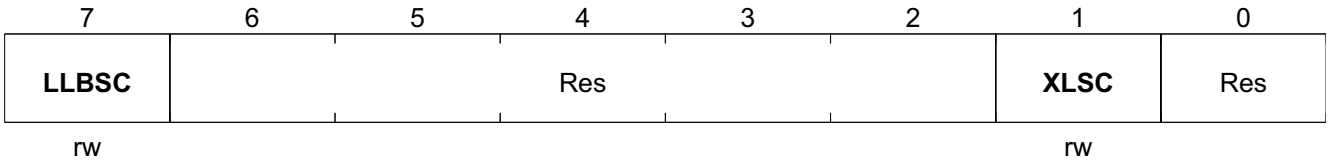
Field	Bits	Type	Description
VISPLL	7	rw	**Masked PLL Interrupts Visible** See also **Chapter 3.5.3** 0_B , Masked interrupt status bits PLLLC and PLLIC are not visible in register GIS2. 1_B , Masked interrupt status bits PLLLC and PLLIC are visible in GIS2, but they are not visible in registers GIS.

Field	Bits	Type	Description
SSYF	2	rw	**Select SYNC Frequency** Only applicable in master mode (LIM0.MAS = ´1´) and bit CMR2.DCF is cleared, see also Table 9. 0_B , Reference clock on port SYNC is 2.048 MHz 1_B , Reference clock on port SYNC is 8 kHz
IC	1:0	rw	**Interrupt Port Configuration** These bits define the function of the interrupt output pin INT. $X0_B$, Open drain output 01_B , Push/pull output, active low 11_B , Push/pull output, active high

Interrupt Mask Register 1

Each interrupt source can generate an interrupt signal on port INT (characteristics of the output stage are defined by register IPC). A “1” in a bit position of IMR(1:4), IMR(6:7) sets the mask active for the interrupt status in ISR(1:4), ISR(6:7). Masked interrupt statuses neither generate a signal on INT, nor are they visible in register GIS. Moreover, they are- not displayed in the interrupt status register if bit GCR.VIS is cleared- displayed in the interrupt status register if bit GCR.VIS is set, see **Chapter 3.5.3**.

IMR1	Offset	Reset Value
Interrupt Mask Register 1	**$xx15_H$**	**FF_H**



Field	Bits	Type	Description
LLBSC	7	rw	**Interrupt Mask Bit LLBSC** Each interrupt source can generate an interrupt signal on port INT. Characteristics of the output stage are defined by register IPC. A ´1´ in a bit position of IMR(7:0) sets the mask active for the interrupt status in the registers ISR. Mask interrupt statuses neither generate a signal on INT, not are they visible in register GIS. Moreover they are not displayed in the interrupt status register if bit GCR.VIS is cleared; they are displayed in the interrupt status register if bit GCR.VIS is set. The bit IMR1.LLBSC is only valid in E1 mode. For T1/J1 mode the equivalent bit is in IMR3.LLBSC.
XLSC	1	rw	**Interrupt Mask Bit XLSC**

Similar Registers

The other Interrupt Mask Registers have the same description.

The Offset Addresses are listed in **IMRn Overview**, for bit names and layout refer to **Interrupt Mask Registers**.

Table 33 IMRn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
IMR2	Interrupt Mask Register 2	$xx16_H$	
IMR3	Interrupt Mask Register 3	$xx17_H$	
IMR4	Interrupt Mask Register 4	$xx18_H$	
IMR6	Interrupt Mask Register 6	$xx1A_H$	
IMR7	Interrupt Mask Register 7	$xxDF_H$	

Table 34 Interrupt Mask Registers

Bit number	7	6	5	4	3	2	1	0
IMR1	LLBSC (E1 only)						XLSC	
IMR2					AIS	LOS		
IMR3		SEC			LLBSC (T1/J1 only)	LTC	RSN	RSP
IMR4	XSP	XSN						
IMR6							LILSU	LILSD
IMR7				XCLKSS1	XCLKSS0			

Mode Register 0

MR0	Offset	Reset Value
Mode Register 0	$xx1C_H$	00_H

7	6	5	4	3	2	1	0
XC		RC		EXZE	ALM	Res	SIM
rw		rw		rw	rw		rw

Field	Bits	Type	Description
XC	7:6	rw	**Transmit Code** Serial line code for the transmitter, independent of the receiver. After changing XC(1:0), a transmitter software reset is required (CMDR.XRES = 1). See **Chapter 3.9.1**. 00_B , Reserved 01_B , CMI (1T2B+HDB3), (optical interface) 10_B , AMI (ternary or digital dual-rail interface) 11_B , HDB3 Code in E1 or B8ZS code in T1/J1 mode (ternary or digital dual-rail interface)
RC	5:4	rw	**Receive Code** Serial line code for the receiver, independent of the transmitter. After changing RC(1:0), a receiver software reset is required (CMDR.RRES = ´1´). See **Chapter 3.7.2**. 00_B , Reserved 01_B , CMI (1T2B+HDB3), (optical interface) 10_B , AMI (ternary or digital dual-rail interface) 11_B , HDB3 Code in E1 or B8ZS code in T1/J1 mode (ternary or digital dual-rail interface)
EXZE	3	rw	**Extended HDB3 Error Detection, E1 only** Selects error detection mode in E1 mode. In T1/J1 mode this bit is reserved. 0_B , Only double violations are detected. 1_B , Extended code violation detection: 0000 strings are detected additionally. Incrementing of the code violation counter CVC is done after receiving four zeros. Errors are indicated by LSR1.EXZD = ´1´.

Field	Bits	Type	Description
ALM	2	rw	**Alarm Mode, E1 only** Selects the AIS alarm detection mode in E1 mode. In T1/J1 mode this bit is reserved. 0_B , The AIS alarm is detected according to ETS300233. Detection: An AIS alarm is detected if the incoming data stream contains less than 3 zeros within a period of 512 bits and a loss of frame alignment is indicated. Recovery: The alarm is cleared if 3 or more zeros within 512 bits are detected or the FAS word is found. 1_B , The AIS alarm is detected according to ITU-T G.775 Detection: An AIS alarm is detected if the incoming data stream contains less than 3 zeros in each doubleframe period of two consecutive doubleframe periods (1024 bits). Recovery: The alarm is cleared if 3 or more zeros are detected within two consecutive doubleframe periods.
SIM	0	rw	**Alarm Simulation, in E1 mode** SIM has to be held stable at high or low level for at least one receive clock period before changing it again. 0_B , Normal operation. 1_B , Initiates internal error simulation of AIS, loss-of-signal and code violations. **Alarm Simulation, in T1/J1 mode** Setting/resetting of SIM initiates internal error simulation of AIS (blue alarm), loss-of-signal (red alarm) and code violations. The error counter CVC is incremented.The selection of simulated alarms is done by the error simulation counter: LSR2.ESC(2:0) which is incremented with each setting of bit SIM. For complete checking of the alarm indications eight simulation steps are necessary (LSR2.ESC(2:0) = ´0´ after a complete simulation). SIM has to be held stable at high or low level for at least one receive clock period before changing it again.

Mode Register 1

MR1	Offset	Reset Value
Mode Register 1	$xx1D_H$	00_H

7	6	5	4	3	2	1	0
Res			**PMOD**	Res			**XAIS**
			rw				rw

Field	Bits	Type	Description
PMOD	4	rw	**PCM Mode** This bit decides between E1 and T1/J1 mode. Switching from E1 to T1 or vice versa the device needs up to 20 µs to settle up to the internal clocking. 0_B , PCM 30 or E1 mode. 1_B , PCM 24 or T1/J1 mode .
XAIS	0	rw	**Transmit AIS Towards Remote End** Sends AIS on ports XL1, XL2, XOID towards the remote end. The outgoing data stream which can be looped back through the local loop to the system interface is not affected.

Mode Register 2

MR2	Offset	Reset Value
Mode Register 2	$xx1E_H$	00_H

7	6	5	4	3	2	1	0
Res		**RTM**	**DAIS**	Res	**PLB**	Res	
		rw	rw		rw		

Field	Bits	Type	Description
RTM	5	rw	**Receive Transparent Mode, E1 only** For E1 mode this bit must be set to ´1´ for proper operation. 0_B , Reserved 1_B ,
DAIS	4	rw	**Disable AIS to Framer Interface** This bit must be set to ´1´for proper operation. 0_B , AIS is automatically inserted into the data stream to RDO if OctalLIU™ is in asynchronous state. 1_B , Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit MR2.SAIS.

Field	Bits	Type	Description
PLB	2	rw	**Payload Loop-Back** See **Chapter 3.11.5**. 0_B , Normal operation. Payload loop is disabled. 1_B , The payload loop-back loops the data stream from the receiver section back to transmitter section. Looped data is output on pin RDO. Data received on port XDI, XSIG, $\overline{SYPX}$ and XMFS is ignored. With XSP.TT0 = ´1´ time slot 0 is also looped back. If XSP.TT0 = 0 time slot 0 is generated internally. AIS is sent immediately on port RDO by setting the FMR2.SAIS bit. It is recommended to write the actual value of XC1 into this register once again, because a write access to register XC1 sets the read/write pointer of the transmit elastic buffer into its optimal position to ensure a maximum wander compensation (the write operation forces a slip).

Loop-Back Register

LOOP	Offset	Reset Value
Loop-Back Register	$xx1F_H$	00_H

7	6	5	4	3	2	1	0
Res	**RTM**	Res					
	rw						

Field	Bits	Type	Description
RTM	6	rw	**Receive Transparent Mode, T1 only** For T1/J1 mode this bit must be set to ´1´ for proper operation. 0_B , Reserved 1_B ,

Mode Register 4

MR4	Offset	Reset Value
Mode Register 4	$xx20_H$	00_H

7	6	5	4	3	2	1	0
Res	**TM**	Res					
	rw						

Field	Bits	Type	Description
TM	6	rw	**Transparent Mode, T1 only** For T1/J1 mode this bit must be set to ´1´ for proper operation. 0_B , Reserved 1_B ,

Mode Register 5

MR5	Offset	Reset Value
Mode Register 5	$xx21_H$	00_H

7	6	5	4	3	2	1	0
Res		**XLD/TT0**	**XLU**	Res	**XTM**	Res	
		rw	rw		rw		

Field	Bits	Type	Description
XLD/TT0	5	rw	**XLD, Transmit Line Loop-Back (LLB) Down Code, T1/J1 only** The equivalent bit in E1 mode is MR3.XLD. 0_B , Normal operation. 1_B , A one in this bit position causes the transmitter to replace normal transmit data with the LLB down (deactivate) Code continuously until this bit is reset. The LLB down code is overwritten by the framing/DL/CRC bits optionally. **TT0, Transmit Transparent Mode, E1 only** For proper operation this bit must be set to ´1´ in E1 mode.

Field	Bits	Type	Description
XLU	4	rw	**Transmit LLB Up Code, T1/J1 only** This bit is not valid in E1 mode. The equivalent bit in E1 mode is MR3.XLU. 0_B , Normal operation. 1_B , A one in this bit position causes the transmitter to replace normal transmit data with the LLB up (activate) code continuously until this bit is reset. The LLB up code is optionally overwritten by the framing/DL/CRC bits. For proper operation bit MR5.XLD must be cleared.
XTM	2	rw	**Transmit Transparent Mode** For proper operation this bit must be set to ´1´.

Receive Control 0

RC0	Offset	Reset Value
Receive Control 0	**$xx24_H$**	**00_H**

7	6	5	4	3	2	1	0
Res				**RDIS**	Res		
				rw			

Field	Bits	Type	Description
RDIS	3	rw	**Receive Data Input Sense** Configures the input polarity of the digital receive inputs. 0_B , In dual rail mode RDI, RDIN are active low, in DCIM mode ROID is active high. 1_B , In dual rail mode RDI, RDIN are active high, in DCIM mode ROID is active low.

Transmit Pulse Mask 0

See Chapter 3.9.6.1 and Chapter 3.9.6.2. The transmit pulse shape which is defined in ITU-T G.703 is output on pins XL1 and XL2. The level of the pulse shape can be programmed by registers XPM(2:0) if XPM2.XPDIS is set to ´0´ to create a custom waveform. If XPM2.XPDIS is set to ´1´, the custom waveform can be programed by the registers TXP(16:1) and the register bits of XPM(2:0) are unused with exception of the bits XPM2.XLT, XPM2.DAXLT and XPM2.XPDIS. In order to get an optimized pulse shape for the external transformers each pulse shape is internally divided into four sub pulse shapes if XPM2.XPDIS is set to ´0´. In each sub pulse shape a programmed 5-bit value defines the level of the analog voltage on pins XL1/2. Together four 5-bit values have to be programmed to form one complete transmit pulse shape. The four 5-bit values are sent in the following sequence:

XP04 to 00: First pulse shape level

XP14 to 10: Second pulse shape level

XP24 to 20: Third pulse shape level

XP34 to 30: Fourth pulse shape level

Changing the LSB of each subpulse in registers XPM(2:0) changes the amplitude of the differential voltage on XL1/2 by approximately 80 mV. Recommended values for standard applications are given in Table 22 and Table 23.

Note that in the special cases were the LBO pulse masks are performed in T1 mode, the programming of the pulse masks is done internally, independent on the settings in XPM(2:0).

XPM0	Offset	Reset Value
Transmit Pulse Mask0	$xx26_H$	$7B_H$

7	6	5	4	3	2	1	0
XP12	**XP11**	**XP10**	**XP04**	**XP03**	**XP02**	**XP01**	**XP00**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
XP12	7	rw	**Bit 2 of second pulse shape level**
XP11	6	rw	**Bit 1 of second pulse shape level**
XP10	5	rw	**Bit 0 (LSB) of second pulse shape level**
XP04	4	rw	**Bit 4 (MSB) of first pulse shape level**
XP03	3	rw	**Bit 3 of first pulse shape level**
XP02	2	rw	**Bit 2 of first pulse shape level**
XP01	1	rw	**Bit 1 of first pulse shape level**
XP00	0	rw	**Bit 0 (LSB) of first pulse shape level**

Transmit Pulse Mask 1

For description see **Transmit Pulse Mask 0**

XPM1	Offset	Reset Value
Transmit Pulse Mask1	$xx27_H$	03_H

7	6	5	4	3	2	1	0
XP30	XP24	XP23	XP22	XP21	XP20	XP14	XP13
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
XP30	7	rw	**Bit 0 (LSB) of fourth pulse shape level**
XP24	6	rw	**Bit 4 (MSB) of third pulse shape level**
XP23	5	rw	**Bit 3 of third pulse shape level**
XP22	4	rw	**Bit 2 of third pulse shape level**
XP21	3	rw	**Bit 1of third pulse shape level**
XP20	2	rw	**Bit 0 (LSB) of third pulse shape level**
XP14	1	rw	**Bit 4 (MSB) of second pulse shape level**
XP13	0	rw	**Bit 3 of second pulse shape level**

Transmit Pulse Mask 2

For description see **Transmit Pulse Mask 0**

XPM2	Offset	Reset Value
Transmit Pulse Mask2	$xx28_H$	40_H

7	6	5	4	3	2	1	0
0	XLT	DAXLT	XPDIS	XP34	XP33	XP32	XP31
r	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
0	7	r	**Always ´0´**
XLT	6	rw	**Transmit Line Tristate** See also **Chapter 3.9.1**. 0_B , Normal operation 1_B , Transmit line XL1 and XL2 are switched into high-impedance state. If this bit is set the transmit line monitor status information is frozen (default value after hardware reset).

Field	Bits	Type	Description
DAXLT	5	rw	**Disable Automatic Tristating of XL1/2** See **Chapter 3.9.7**. 0_B , Normal operation. If a short is detected on pins XL1/2 the transmit line monitor sets the XL1/2 outputs into a high-impedance state. 1_B , If a short is detected on XL1/2 pins automatic setting these pins into a high-impedance (by the XL-monitor) state is disabled.
XPDIS	4	rw	**Disable XPM Values** See **Chapter 3.9.6**. 0_B , XP values from registers XPM(2:0) are used for pulse shaping. 1_B , TXP values from registers TXP(16:1) are used for pulse shaping.
XP34	3	rw	**Bit 4 (MSB) of second pulse shape level** See **Chapter 3.9.6.1**.
XP33	2	rw	**Bit 3 of fourth pulse shape level**
XP32	1	rw	**Bit 2 of fourth pulse shape level**
XP31	0	rw	**Bit 1 of fourth pulse shape level**

Clear Channel Register 1

The registers CCB(1:3) are only valid in T1/J1 mode.

CCB1	Offset	Reset Value
Clear Channel Register 1	**xx2F$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
CH1	**CH2**	**CH3**	**CH4**	**CH5**	**CH6**	**CH7**	**CH8**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CH1	7	rw	**Channel Selection Bits** If AMI code is selected, all bits must be set to ´1´ for proper operation. 0_B , Normal operation. Bit robbing information and zero code suppression (ZCS, B7 stuffing) can change contents of the selected speech/data channel if assigned modes are enabled by bits MR5.EIBR and MR0.XC(1:0). 1_B , Clear channel mode. Contents of selected speech/data channel are not overwritten by internal or external bit robbing and ZCS information. Transmission of channel assigned signaling and control of pulse-density is applied by the user.
CH2	6		
CH3	5		
CH4	4		
CH5	3		
CH6	2		
CH7	1		
CH8	0		

Similar Registers

Registers CCB2 and CCB3 have the same description.

The Offset Addresses are listed in **CCBn Overview**, for layout and bit names refer to **Clear Channel Registers**

Table 35 CCBn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
CCB2	Clear Channel Register 2	30_H	
CCB3	Clear Channel Register 3	31_H	

Table 36 Clear Channel Registers

	7	6	5	4	3	2	1	0
CCB1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
CCB2	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
CCB3	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24

Mode Register 3

Only valid in E1 mode.

MR3	Offset	Reset Value
Mode Register 3	$xx31_H$	00_H

7	6	5	4	3	2	1	0
Res		**XLD**	**XLU**	**CMI**	Res		
		rw	rw	rw			

Field	Bits	Type	Description
XLD	5	rw	**Transmit LLB Down Code, E1 only** This bit is not valid in T1/J1 mode. In T1/J1 mode the bis MR5.XLD is used instead. 0_B , Normal operation. 1_B , A one in this bit position causes the transmitter to replace normal transmit data with the LLB down (deactivate) Code continuously until this bit is reset. The LLB down Code is optionally overwritten by the time slot 0 depending on bit LCR1.FLLB.
XLU	4	rw	**Transmit LLB UP Code, E1 only** This bit is not valid in T1/J1 mode. In T1/J1 mode the bit MR5.XLU is used instead. 0_B , Normal operation. 1_B , A one in this bit position causes the transmitter to replace normal transmit data with the LLB UP Code continuously until this bit is reset. The LLB UP Code is overwritten by the time slot 0 depending on bit LCR1.FLLB. For proper operation bit MR3.XLD must be cleared.

Field	Bits	Type	Description
CMI	3	rw	**Select CMI Precoding, E1 only** This bit is not valid in T1/J1 mode. In T1/J1 mode the similar bit for B8ZS precoding is DIC3.CMI. In E1 mode only valid if CMI code (MR0.XC(1:0) = ´01_b´) is selected. This bit defines the CMI precoding and influences transmit and receive data. *Note: Before local loop is selected, HDB3 precoding has to be disabled.* 0_B , CMI with HDB3 precoding 1_B , CMI without HDB3 precoding

Line Interface Mode 0

LIM0 **Offset** **Reset Value**

Line Interface Mode 0 **$xx36_H$** **00_H**

7	6	5	4	3	2	1	0
XFB	**XDOS**	**RTRS**	**DCIM**	Res	**RLM**	**LL**	**MAS**
rw	rw	rw	rw		rw	rw	rw

Field	Bits	Type	Description
XFB	7	rw	**Transmit Full Bauded Mode** Only applicable for dual-rail mode (bit LIM1.DRS = ´1´). *Note: If CMI coding is selected (MR0.XC(1:0) = ´01_b´) this bit has to be cleared.* 0_B , Output signals XDO/XDON are half bauded. 1_B , Output signals XDO/XDON are full bauded.
XDOS	6	rw	**Transmit Data Out Sense** *Note: If CMI coding is selected (MR0.XC(1:0) = ´01_b´) this bit has to be cleared. The transmit frame marker XFM is independent of this bit.* 0_B , Output signals XDO/XDON are active low. Output XOID is active high (normal operation). 1_B , Output signals XDO/XDON are active high. Output XOID is active low.
RTRS	5	rw	**Receive Termination Resistance Selection** This bit controls the analog switch of the receive line interface. *Note: If the RLT functionality is selected at one of the multi function ports, a logical equivalence is build out of RTRS and RLT for controlling the analog switch. If RLT functionality is not configured at one of the multi function ports, the analog switch is controlled only by RTRS.* 0_B , Analog is switched off. 1_B , Analog switch is switched on.

Field	Bits	Type	Description
DCIM	4	rw	**Digital Clock Interface Mode** *Note: DCO-X must be used in DCIM mode (CMR1.DXJA = ´0´).* 0_B , Normal operation. 1_B , Enables the digital Clock Interface Mode (synchronization interface mode) according to ITU-T G.703, Section 13. A 2048/1544 kHz clock is expected on RL1/2. On XL1/2 a 2048/1544 kHz output clock is driven. The transmit clock signal on XL1/2 is derived from the clock supplied on FCLKX (CMR1.DXSS = ´0´).
RLM	2	rw	**Receive Line Monitoring** See **Chapter 3.7.4**. 0_B , Normal receiver mode 1_B , Receiver mode for receive line monitoring; the receiver sensitivity is increased to detect resistively attenuated signals of -20 dB (short-haul mode only)
LL	1	rw	**Local Loop** See **Chapter 3.11.4**. 0_B , Normal operation 1_B , Local loop active. The local loop back mode disconnects the receive lines RL1/RL2 or ROID from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. The unipolar bit stream is transmitted undisturbed on the line. Receiver and transmitter coding must be identical. Operates in analog and digital line interface mode. In analog line interface mode data is transferred through the complete analog receiver.
MAS	0	rw	**Master Mode** See also **Table 19**. 0_B , Slave mode 1_B , Master mode on. Setting this bit the DCO-R circuitry is frequency synchronized to the clock (2.048 MHz or 8 kHz, see IPC.SSYF) supplied by SYNC. If this pin is connected to VSS or VDD (or left open and pulled up to VDD internally) the DCO-R circuitry is centered and no receive jitter attenuation is performed (only if 2.048 MHz clock is selected by resetting bit IPC.SSYF). The generated clocks are stable.

Line Interface Mode 1

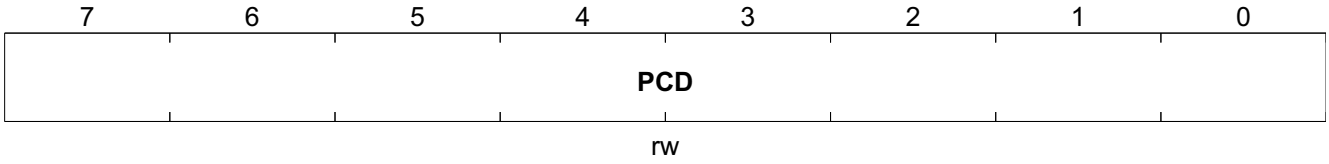
LIM1	Offset	Reset Value
Line Interface Mode 1	$xx37_H$	80_H

7	6	5	4	3	2	1	0
CLOS	**RIL2**	**RIL1**	**RIL0**	Res	**JATT**	**RL**	**DRS**
rw	rw	rw	rw		rw	rw	rw

Field	Bits	Type	Description
CLOS	7	rw	**Clear data in case of LOS** 0_B , Normal receiver mode, receive data stream is transferred normally in long-haul mode 1_B , Received data is cleared (driven to low level), as soon as LOS is detected
RIL2	6	rw	**Receive Input Threshold** Only valid if analog line interface is selected (LIM1.DRS = ´0´).“No signal” is declared if the voltage between pins RL1 and RL2 drops below the limits programmed by bits RIL(2:0) and the received data stream has no transition for a period defined in the PCD register. See DC characteristics for detail.
RIL1	5	rw	
RIL0	4	rw	
JATT	2	rw	**Transmit Jitter Attenuator** *Note: JATT is only used to define the jitter attenuation during remote loop operation. Remote loop operation can be set by LIM1.RL Jitter attenuation during normal operation is not affected by JATT.* 0_B , Transmit jitter attenuator is disabled for remote Loop. Transmit data bypasses the remote loop jitter attenuator buffer. 1_B , Jitter attenuator is active for remote loop. Received data from pins RL1/2 or ROID is sent "jitter-free" on ports XL1/2 or XOID. The de-jittered clock is generated by the DCO-X circuitry.
RL	1	rw	**Remote Loop** *Note: RL is logically OR´d with automatic loop switching by BOM messages.* 0_B , Normal operation. 1_B , Remote Loop active.
DRS	0	rw	**Dual-Rail Select** 0_B , The ternary interface is selected. Ports RL1/2 and XL1/2 become analog in/outputs. 1_B , The digital dual-rail interface is selected. Received data is latched on ports RDIP/RDIN while transmit data is output on pins XDOP/XDON.

Pulse Count Detection Register

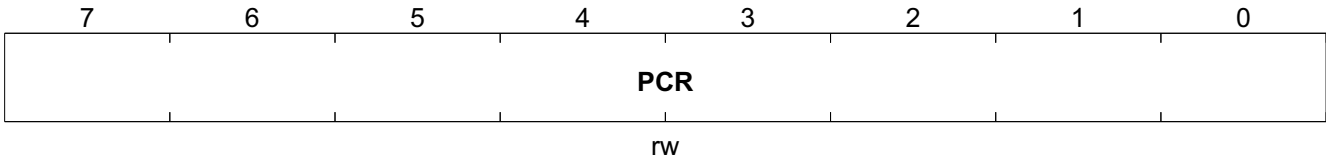
PCD	Offset	Reset Value
Pulse Count Detection Register	$xx38_H$	00_H



Field	Bits	Type	Description
PCD	7:0	rw	**Pulse Count Detection** A LOS alarm is detected if the incoming data stream has no transitions for a programmable number T consecutive pulse positions. The number T is programmable by the PCD register and can be calculated as follows: T = 16 x (N+1); with 0 ≤ N ≤ 255. The maximum time is: 256 x 16 x 488 ns = 2 ms. Every detected pulse resets the internal pulse counter. The counter is clocked with the receive clock RCLK.

Pulse Count Recovery

PCR	Offset	Reset Value
Pulse Count Recovery	$xx39_H$	00_H



Field	Bits	Type	Description
PCR	7:0	rw	**Pulse Count Recovery** A LOS alarm is cleared if a pulse-density is detected in the received bit stream. The number of pulses M which must occur in the predefined PCD time interval is programmable by the PCR register and can be calculated as follows: M = N+1; with 0 ≤ N ≤ 255. The time interval starts with the first detected pulse transition. With every received pulse a counter is incremented and the actual counter is compared to the contents of PCR register. If the pulse number is higher or equal to the PCR value the LOS alarm is reset otherwise the alarm stays active. In this case the next detected pulse transition starts a new time interval.

Line Interface Mode 2

LIM2	Offset	Reset Value
Line Interface Mode 2	$xx3A_H$	20_H

7	6	5	4	3	2	1	0
Res		**SLT1**	**SLT0**	**SCF**	**ELT**	Res	
		rw	rw	rw	rw		

Field	Bits	Type	Description
SLT1	5	rw	**Receive Slicer Threshold**
SLT0	4	rw	00_B , The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 55% of the peak amplitude. 01_B , The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 67% of the peak amplitude (recommended in some T1/J1 applications). 10_B , The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 50% of the peak amplitude (default, recommended in E1 mode). 11_B , The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 45% of the peak amplitude.
SCF	3	rw	**Select Corner Frequency of DCO-R** Setting this bit reduces the corner frequency of the DCO-R circuit by the factor of ten to 0.2 Hz. See **Chapter 3.7.9**. *Note: Reducing the corner frequency of the DCO-R circuitry increases the synchronization time before the frequencies are synchronized.*
ELT	2	rw	**Enable Loop-Timed** 0_B , Normal operation 1_B , Transmit clock is generated from the clock supplied by MCLK which is synchronized to the extracted receive route clock. In this configuration the transmit elastic buffer has to be enabled. For correct operation of loop timed the remote loop (bit LIM1.RL = ´0´) must be inactive and bit CMR1.DXSS must be cleared.

Loop Code Register 1

LCR1	Offset	Reset Value
Loop Code Register 1	$xx3B_H$	00_H

7	6	5	4	3	2	1	0
EPRM	XPRBS	LDC		LAC		FLLB	LLBP
rw	rw	rw		rw		rw	rw

Field	Bits	Type	Description
EPRM	7	rw	**Enable Pseudo-Random Binary Sequence Monitor** See **Chapter 3.11.1**. 0_B , Pseudo-Random Binary Sequence (PRBS) monitor is disabled. 1_B , PRBS is enabled. Setting this bit enables incrementing the CEC2 error counter with each detected PRBS bit error. With any change of state of the PRBS internal synchronization status an interrupt ISR1.LLBSC is generated. The current status of the PRBS synchronizer is indicated by bit LSR2.LLBAD.
XPRBS	6	rw	**Transmit Pseudo-Random Binary Sequence** A one in this bit position enables transmission of a pseudo-random binary sequence to the remote end. Depending on bit LLBP the PRBS is generated according to 2^{15} -1 or 2^{20} -1 with a maximum-14-zero restriction (ITU-T O. 151). See **Chapter 3.11.1**.
LDC	5:4	rw	**Length Deactivate (Down) Code** These bits defines the length of the LLB deactivate code which is programmable in register LCR2. 00_B , Length: 5 bit 01_B , Length: 6 bit, 2 bit, 3 bit 10_B , Length: 7 bit 11_B , Length: 8 bit, 2 bit, 4bit
LAC	3:2	rw	**Length Activate (Up) Code** These bits defines the length of the LLB activate code which is programmable in register LCR3. 00_B , Length: 5 bit 01_B , Length: 6 bit, 2 bit, 3 bit 10_B , Length: 7 bit 11_B , Length: 8 bit, 2 bit, 4 bit
FLLB	1	rw	**Framed Line Loop-Back/Invert PRBS** Depending on bit LCR1.XPRBS this bit enables different functions: LCR1.XPRBS = ´0´: **Table 37**. *Note: Invert PRBS LCR1.XPRBS = ´1´: see **Table 38***
LLBP	0	rw	**Line Loop-Back Pattern** See **Chapter 3.11.2** LCR1.XPRBS = ´0´: see **Table 39** LCR1.XPRBS = ´1´ or LCR1.EPRM = ´1´: see **Table 40**

Table 37 FLLB Constant Values (Case 1)

Name and Description	Value
Framed Line Loop-Back/Invert PRBS The line loop-back code is transmitted including framing bits. LLB code overwrites the FS/DL-bits.	0_B
Framed Line Loop-Back/Invert PRBS The line loop-back code is transmitted unframed. LLB code does not overwrite the FS/DL-bits.	1_B

Table 38 FLLB Constant Values (Case 2)

Name and Description	Value
Framed Line Loop-Back/Invert PRBS The generated PRBS is transmitted not inverted.	0_B
Framed Line Loop-Back/Invert PRBS The PRBS is transmitted inverted.	1_B

Table 39 LLBP Constant Values (Case 1)

Name and Description	Value
Line Loop-Back Pattern Fixed line loop-back code according to ANSI T1. 403.	0_B
Line Loop-Back Pattern Enable user-programmable line loop-back code by register LCR2/3.	1_B

Table 40 LLBP Constant Values (Case 2)

Name and Description	Value
Line Loop-Back Pattern 2^{15} -1	0_B
Line Loop-Back Pattern 2^{20} -1	1_B

Loop Code Register 2

LCR2	Offset	Reset Value
Loop Code Register 2	$xx3C_H$	00_H

7	6	5	4	3	2	1	0
LDC							
rw							

Field	Bits	Type	Description
LDC	7:0	rw	**Line Loop-Back Deactivate Code** If enabled by bit MR3.XLD = ´1´ in E1 or MR5.XLD = ´1´ in T1/J1 mode the LLB deactivate code automatically repeats until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LDC0 is transmitted last. For correct operations bit LCR1.XPRBS has to cleared. If LCR2 is changed while the previous deactivate code has been detected and is still received, bit LSR2.LLBDD in E1 or LSR1.LLBDD in T1/J1 mode will stay active until the incoming signal changes or a receiver reset is initiated (CMDR.RRES = ´1´).

Loop Code Register 3

LCR3	Offset	Reset Value
Loop Code Register 3	$3D_H$	00_H

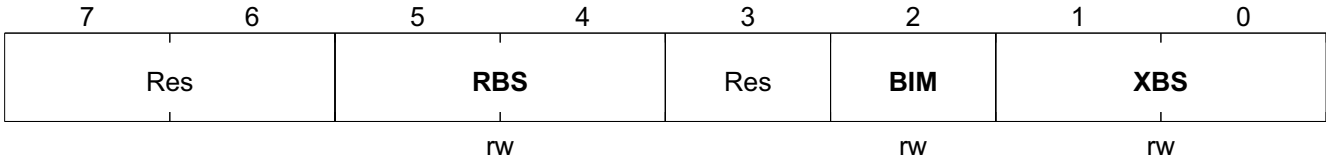
7	6	5	4	3	2	1	0
LAC							
rw							

Field	Bits	Type	Description
LAC	7:0	rw	**Line Loop-Back Activate Code** If enabled by bit MR3.XLD = ´1´ in E1 or MR5.XLD = ´1´ in T1/J1 mode the LLB activate code automatically repeats until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LAC0 is transmitted last. For correct operations bit LCR1.XPRBS has to cleared.If LCR3 is changed while the previous activate code has been detected and is still received, bit LSR2.LLBAD in E1 or LSR1.LLBAD in T1/J1 mode will stay active until the incoming signal changes or a receiver reset is initiated (CMDR.RRES = ´1´).

Digital Interface Control 1

See **Chapter 3.7.10**.

DIC1	Offset	Reset Value
Digital Interface Control 1	**xx3E$_H$**	**00$_H$**



Field	Bits	Type	Description
RBS	5:4	rw	**Receive Buffer Size** See **Table 21**. 00_B , Buffer size: 2 frames 01_B , Buffer size: 1 frame 10_B , Buffer size: 96 bits 11_B , bypass of receive elastic store
BIM	2	rw	**Bit Interleaved Mode** 0_B , Byte interleaved mode 1_B , Bit interleaved mode
XBS	1:0	rw	**Transmit Buffer Size** See **Table 21**. 00_B , Bypass of transmit elastic store 01_B , Buffer size: 1 frame 10_B , Buffer size: 2 frames 11_B , Buffer size: 96 bits

Digital Interface Control 2

DIC2	Offset	Reset Value
Digital Interface Control 2	xx3F$_H$	00$_H$

7	6	5	4	3	2	1	0
Res		**CRB**	Res				
		rw					

Field	Bits	Type	Description
CRB	5	rw	**Center Receive Elastic Buffer** Only applicable if the time slot assigner is disabled (PC(3:1).RPC(3:0) = ´0001$_b$´), no external or internal synchronous pulse receive is generated. A transition from low to high forces a receive slip and the read- pointer of the receive elastic buffer is centered. The delay through the buffer is set to one half of the current buffer size. It should be hold high for at least two 2.048 MHz periods before it is cleared.

Digital Interface Control 3

DIC3	Offset	Reset Value
Digital Interface Control 3	xx40$_H$	00$_H$

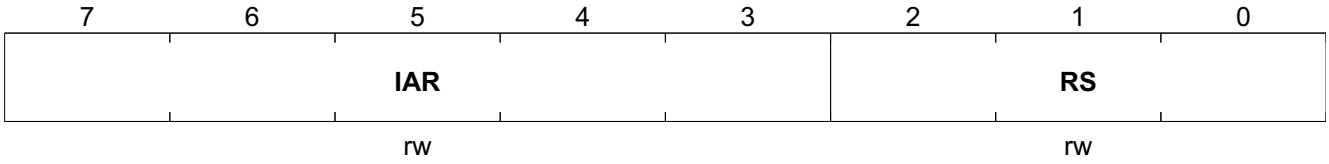
7	6	5	4	3	2	1	0
CMI	**RRTRI**	**RTRI**	**FSCT**	**RESX**	**RESR**	Res	
rw	rw	rw	rw	rw	rw		

Field	Bits	Type	Description
CMI	7	rw	**Select CMI Precoding (T1 only)** Only valid if CMI code (MR0.XC(1:0) = ´01$_b$´) is selected. This bit defines the CMI precoding and influences transmit and receive data. *Note: Before local loop is closed, B8ZS precoding has to be switched off.* 0_B , CMI with B8ZS precoding 1_B , CMI without B8ZS precoding

Field	Bits	Type	Description
RRTRI	6	rw	**RDO Tristate Mode** See **Chapter 3.7.4** *Note: RRTRI is logically exored with RTDMT multi function port, if this function is selected. RTDMT exor RRTRI sets additionally RCLK into tristate.* 00_B , normal operation (RDOP is switched to low level during inactive channel/bit phases). 01_B , RDO is switched into tristate mode during inactive channel/bit phases. 10_B , RDO is tristate constantly (and also RCLK). 11_B , RDO is tristate constantly (and also RCLK).
RTRI	5		
FSCT	4	rw	**FSC Tristate Mode** 0_B , normal operation of FSC pin. 1_B , FSC is switched into tristate mode.
RESX	3	rw	**Rising Edge Synchronous Transmit** Depending on this bit all transmit framer interface data are clocked (outputs) or sampled (inputs) with the selected active edge of the selected framer transmit clock. Only valid if CMR2.IXSC = ´0´: *Note: CMR2.IXSC = ´1´: value of RESX bit has no impact on the selected edge of the system interface clock but value of $\overline{RESR}$ bit is used as RESX. Example: If RESR = ´0´, the rising edge of system interface clock is the selected one for sampling data on XDI and vice versa.* 0_B , Clocked or sampled with the first falling edge of the selected framer interface transmit clock. 1_B , Clocked or sampled the first rising edge of the selected framer interface transmit clock.
RESR	2	rw	**Rising Edge Synchronous Receive** Depending on this bit all receive framer interface data are clocked (outputs) or sampled (inputs) with the selected active edge. 0_B , Clocked or sampled with the first falling edge of the selected framer interface receive clock. 1_B , Clocked or sampled with the first rising edge of the selected framer interface receive clock.

Clock Mode Register 4

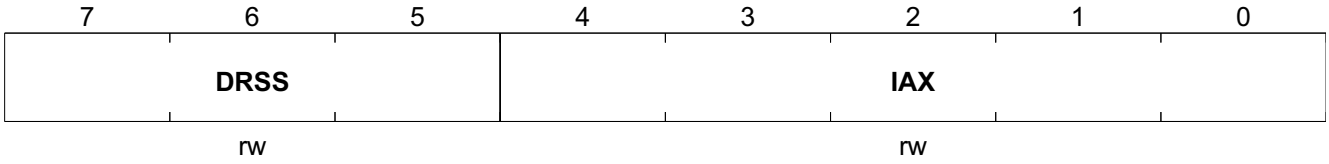
CMR4	Offset	Reset Value
Clock Mode Register 4	$xx41_H$	00_H



Field	Bits	Type	Description
IAR	7:3	rw	**Integral parameter selection** (Corner frequency and attenuation selection) for the DCO-R Only valid if CMR6.DCOCOMPN = ´1´and CMR2.ECFAR = ´1´, see **Chapter 3.7.9**.
RS	2:0	rw	**Receive Clock (RCLK) Frequency Selection** See also **Chapter 3.7**. 000_B , clock recovered from the line through the DPLL drives RCLK. 001_B , clock recovered from the line through the DPLL drives RCLK. logically OR´d with the incoming LOS signal. 010_B , 2.048 MHz, dejitered, sourced by DCO-R. 011_B , 4.096 MHz, dejitered, sourced by DCO-R. 100_B , 8.192 MHz, dejitered, sourced by DCO-R. 101_B , 16.384 MHz, dejitered, sourced by DCO-R. 110_B , 2.048 MHz logically OR´d with LOS. 111_B , 16.384 MHz logically OR´d with LOS.

Clock Mode Register 5

CMR5	Offset	Reset Value
Clock Mode Register 5	$xx42_H$	00_H



Field	Bits	Type	Description
DRSS	7:5	rw	**DCO-R Channel Selection** See **Chapter 3.7**. 000_B , Receive reference clock generated by the DPLL of channel 1. 001_B , Receive reference clock generated by the DPLL of channel 2. 010_B , Receive reference clock generated by the DPLL of channel 3. 011_B , Receive reference clock generated by the DPLL of channel 4. 100_B , Receive reference clock generated by the DPLL of channel 5. 101_B , Receive reference clock generated by the DPLL of channel 6. 110_B , Receive reference clock generated by the DPLL of channel 7. 111_B , Receive reference clock generated by the DPLL of channel 8.
IAX	4:0	rw	**Integral parameter selection** (Corner frequency and attenuation selection) for the DCO-X Only valid if CMR6.DCOCOMPN = ´1´ and CMR2.ECFAX = ´1´, see **Chapter 3.7.9**.

Clock Mode Register 6

CMR6	Offset	Reset Value
Clock Mode Register 6	$xx43_H$	00_H

7	6	5	4	3	2	1	0
DCOCOMPN	SRESR	SRESX	STF			SCFX	ATCS
rw	rw	rw	rw			rw	rw

Field	Bits	Type	Description
DCOCOMPN	7	rw	**Compatibility programming of DCO-R/DCO-X disable** Only applicable if CMR2.ECFAR/ECFAX is set. See Chapter 3.7.9, Table 18. 0_B , Programming of corner frequencies of DCO-R/DCO-X is done with registers CMR3.CFAR (3:0) /CFAX(3:0), compatible to the QuadLIU. Register bits CMR5.IAX(4:0)/CMR4.IAR(4:0) are not valid. 1_B , Programming of corner frequencies and attenuation factors of DCO-R/DCO-X is done with registers CMR3.CFAR (3:0)/CFAX(3:0) and CMR4.IAR(4:0)/CMR5.IAX(4:0) in the range 0.2 ... 20 Hz.
SRESR	6	rw	**Soft Reset of DCO-R** By setting this bit a soft reset of the DCO-R will be performed: The initial phase error is set to zero and the loop filter is cleared. To enable the DCO-R lock functionality, this bit must be cleared subsequently. See Chapter 3.7.9. 0_B , DCO-R enabled (normal lock functionality). 1_B , Soft reset of DCO-R, no lock functionality.
SRESX	5	rw	**Soft Reset of DCO-X** By setting this bit a soft reset of the DCO-X will be performed: The initial phase error is set to zero and the loop filter is cleared. To enable the DCO-X lock functionality, this bit must be cleared subsequently. See Chapter 3.7.9. 0_B , DCO-X enabled (normal lock functionality). 1_B , Soft reset of DCO-X, no lock functionality.
STF	4:2	rw	**Transmit Clock (TCLK) Frequency Selection** See Chapter 3.9.2.. Note that frequencies are not in ascend ordering. 000_B , 2.048 MHz. 001_B , 8.192 MHz. 010_B , 4.096 MHz. 011_B , 16.384 MHz. 100_B , 32.768 MHz. 101_B , Reserved. 110_B , Reserved. 111_B , Reserved.

Field	Bits	Type	Description
SCFX	1	rw	**Select Corner Frequency of DCO-X** Only applicable if CMR2.EXFAX = ´0´. See **Chapter 3.7.9** and **Chapter 3.9.4**. 0_B , Corner frequency of DCO-X is 2 Hz. 1_B , Corner frequency of DCO-X is 0.2 Hz.
ATCS	0	rw	**Automatic Transmit Clock Switching** See **Chapter 3.9.3**. If TCLK is lost, automatically switching to FCLKX can be performed. *Note: Kind of used transmit clock source is shown in status register XCLKS.* 0_B , Automatic clock switching is disabled. 1_B , Automatic clock switching is enabled.

Clock Mode Register 1

CMR1	Offset	Reset Value
Clock Mode Register 1	$xx44_H$	00_H

7	6	5	4	3	2	1	0
Res				**DCS**	Res	**DXJA**	**DXSS**
				rw		rw	rw

Field	Bits	Type	Description
DCS	3	rw	**Disable Clock-Switching** In Slave mode (LIM0.MAS = ´0´) the DCO-R is synchronized on the recovered route clock. In case of loss-of-signal LOS the DCO-R switches automatically to the clock sourced by port SYNC, see also Table 18. 0_B , Automatic switching from RCLK to SYNC is enabled 1_B , Automatic switching from RCLK to SYNC is disabled
DXJA	1	rw	**Disable Internal Transmit Jitter Attenuation** Setting this bit disables the transmit jitter attenuation. Reading the data out of the transmit elastic buffer and transmitting on XL1/2 (XDOP/N/XOID) is done with the clock provided on pin TCLK. In transmit elastic buffer bypass mode the transmit clock is taken from FCLKX, independent of this bit.

Field	Bits	Type	Description
DXSS	0	rw	**DCO-X Synchronization Clock Source** 0_B , The DCO-X circuitry synchronizes to the internal reference clock which is sourced by FCLKX/R or RCLK. Since there are many reference clock opportunities the following internal prioritizing in descending order from left to right is realized: LIM1.RL > CMR1.DXSS > LIM2.ELT > current working clock of transmit system interface. If one of these bits is set the corresponding reference clock is taken. 1_B , DCO-X synchronizes to an external reference clock provided on multi function port XPA or XPB pin function TCLK, if no remote loop is active. TCLK is selected by PC(2:1).XPC(3:0) = ´0011_B´.

Clock Mode Register 2

CMR2	Offset	Reset Value
Clock Mode Register 2	$xx45_H$	00_H

7	6	5	4	3	2	1	0
ECFAX	**ECFAR**	**DCOXC**	**DCF**	**IRSP**	**IRSC**	Res	**IXSC**
rw	rw	rw	rw	rw	rw		rw

Field	Bits	Type	Description
ECFAX	7	rw	**Enable Corner Frequency Adjustment for DCO-X** See **Chapter 3.7.9**. *Note: DCO-X must be activated.* 0_B , Adjustment is disabled (only 2 Hz and 0.2 Hz are possible). 1_B , Adjustment is enabled as programmed in CMR3.CFAX(3:0) and CMR4.IAX(4:0).
ECFAR	6	rw	**Enable Corner Frequency Adjustment for DCO-R** See **Chapter 3.7.9**. *Note: DCO-R must be activated.* 0_B , Adjustment is disabled (only 2 Hz and 0.2 Hz are possible). 1_B , Adjustment is enabled as programmed in CMR3.CFAR(3:0) and CMR5.IAR(4:0).
DCOXC	5	rw	**DCO-X Center-Frequency Enable** See **Chapter 3.7.9** 0_B , The center function of the DCO-X circuitry is disabled. 1_B , The center function of the DCO-X circuitry is enabled. DCO-X centers to 2.048 MHz related to the master clock reference (MCLK), if reference clock (e.g. FCLKX) is missing.

Field	Bits	Type	Description
DCF	4	rw	**DCO-R Center- Frequency Disabled** See also **Table 19**. 0_B , The DCO-R circuitry is frequency centered in master mode if no 2.048 MHz reference clock on pin SYNC is provided or in slave mode if a loss-of-signal occurs in combination with no 2.048 MHz clock on pin SYNC or a gapped clock is provided on pin RCLKI and this clock is inactive or stopped. 1_B , The center function of the DCO-R circuitry is disabled. The generated clock (DCO-R) is frequency frozen in that moment when no clock is available on pin SYNC or pin RCLKI. The DCO-R circuitry starts synchronization as soon as a clock appears on pins SYNC or RCLKI.
IRSP	3	rw	**Internal Receive System Frame Sync Pulse** *Note: Recommendation: This bit should be set to ´1´.* 0_B , The frame sync pulse is derived from RDOP output signal internally (free running). 1_B , The frame sync pulse for the receive system interface is internally sourced by the DCO-R circuitry. This internally generated frame sync signal can be output (active low) on multifunction ports RP(A to D) (RPC(3:0) = ´0001_H´).
IRSC	2	rw	**Internal Receive Digital (Framer) Clock** See also **Figure 35**. 0_B , The working clock for the receive framer interface is sourced by FCLKR or in receive elastic buffer bypass mode from the corresponding extracted receive clock RCLK. 1_B , The working clock for the receive framer interface is sourced internally by DCO-R or in bypass mode by the extracted receive clock. FCLKR is ignored.
IXSC	0	rw	**Internal Transmit Digital (Framer) Clock** See also **Figure 35**. 0_B , The working clock for the transmit framer interface is sourced by FCLKX. 1_B , The working clock for the transmit framer interface is sourced internally by the working clock of the receive framer interface. FCLKX is ignored.

Global Configuration Register

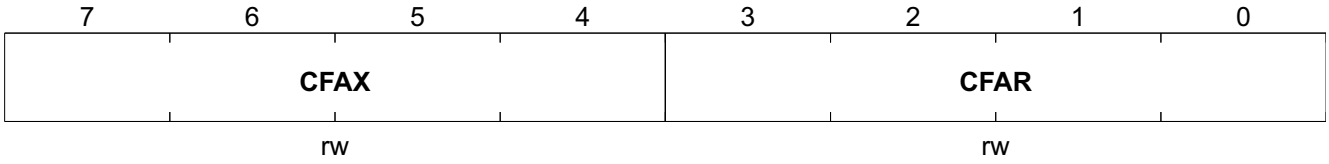
GCR	Offset	Reset Value
Global Configuration Register	0046_H	00_H

7	6	5	4	3	2	1	0
VIS	**SCI**	Res					**PD**
rw	rw						rw

Field	Bits	Type	Description
VIS	7	rw	**Masked Interrupts Visible** See also **Chapter 3.5.3** 0_B , Masked interrupt status bits are not visible in registers ISR(7:0). 1_B , Masked interrupt status bits are visible in ISR(7:0), but they are not visible in register GIS.
SCI	6	rw	**Status Change Interrupt** 0_B , Interrupts are generated either on activation or deactivation of the internal interrupt source. 1_B , The following interrupts are activated both on activation and deactivation of the internal interrupt source: ISR2.LOS, ISR2.AIS, ISR3.LMFA16.
PD	0	rw	**Power Down** Switches between power-up and power-down mode. After switching from power down to power up a receiver reset should be made by setting of CMDR.RRES. 0_B , Power up 1_B , Power down: All outputs are driven inactive; multifunction ports are driven high by the weak internal pull-up device.

Clock Mode Register 3

CMR3	Offset	Reset Value
Clock Mode Register 3	$xx48_H$	00_H

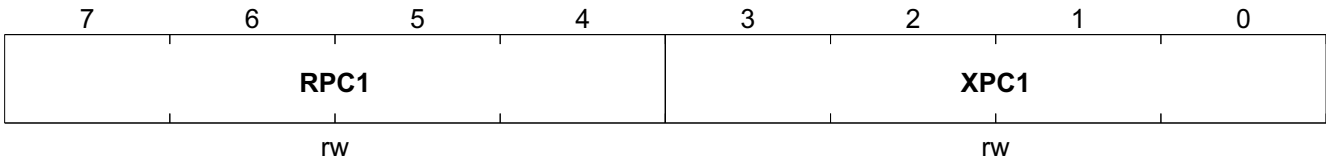


Field	Bits	Type	Description
CFAX	7:4	rw	**Corner Frequency Adjustment for DCO-X** See **Chapter 3.7.9**. *Note: DCO-X must be activated and CMR2.ECFAX must be set (adjustment must be enabled).*
CFAR	3:0	rw	**Corner Frequency Adjustment for DCO-R** See **Chapter 3.7.9**. *Note: DCO-R must be activated and CMR2.ECFAR must be set (adjustment must be enabled).*

Port Configuration 1

See **Chapter 3.12**.

PC1	Offset	Reset Value
Port Configuration 1	$xx80_H$	00_H



Field	Bits	Type	Description
RPC1	7:4	rw	**Receive Multifunction Port Configuration** See **Chapter 3.12**. The multifunction ports RP(A to C) are bidirectional. After Reset the ports RPA and RPB are reserved, the port RPC is configured as RCLK output. With the selection of the pin function the In/Output configuration is also achieved. Register PC1 configures port RPA, while PC2 configures port RPB and PC3 configures port RPC. See **RPC1 Constant Values**

Field	Bits	Type	Description
XPC1	3:0	rw	**Transmit Multifunction Port Configuration** See **Chapter 3.12**. The multifunction ports XP(A to B) are bidirectional. After Reset these ports are configured as inputs. With the selection of the pin function the In/Output configuration is also achieved. Each of the three different input functions (TCLK, XLT and $\overline{\text{XLT}}$) may only be selected once. No input function must be selected twice or more. Register PC1 configures port XPA and PC2 the port XPB. See **XPC1 Constant Values**

Table 41 RPC1 Constant Values

Name and Description	Value
reserved	0000_B
reserved	0001_B
reserved	0010_B
reserved	0011_B
reserved	0100_B
reserved	0101_B
reserved	0110_B
reserved	0111_B
RLT: Receive line termination (input) “Hardware” switching of receive line termination, see **Chapter 3.7.3**	1000_B
GPI: general purpose input Value of this input is stored in register MFPI.	1001_B
GPOH: General purpose output, high level Pin is set fixed to high level	1010_B
GPOL: General purpose output, low level Pin is set fixed to low level	1011_B
LOS: Loss of signal Loss of signal indication output	1100_B
RTDMT: Receive TDM tristate (input) receive TDM i/f tristate (RDOP, RCLK).	1101_B
RDON: Receive data out negative negative receive data out in dual rail mode or bipolar violation out in LIU single rail mode	1110_B
RCLK: RCLK output	1111_B

Table 42 XPC1 Constant Values

Name and Description	Value
reserved	0000_B
reserved	0001_B
reserved	0010_B

Table 42 XPC1 Constant Values (cont'd)

Name and Description	Value
TCLK: Transmit Clock (Input) A 2.048/8.192 MHz clock has to be sourced by the system if the internal generated transmit clock (DCO-X) is not used. Optionally this input is used as a synchronization clock for the DCO-X circuitry with a frequency of 2.048 MHz.	0011_B
reserved	0100_B
reserved	0101_B
reserved	0110_B
XCLK: Transmit Line Clock (Output) Frequency: 2.048 MHz	0111_B
XLT: Transmit Line Tristate control input, high active With a high level on this port the transmit lines XL1/2 or XDOP/N are set directly into tristate. This pin function is logically OR´d with register XPM2.XLT. See **Chapter 3.9.1**.	1000_B
GPI: General Purpose Input, low level Value of this input is stored in register MFPI.	1001_B
GPOH: General Purpose Output, high level Pin is set fixed to high level	1010_B
GPOL: General Purpose Output, low level Pin is set fixed to low level	1011_B
reserved	1100_B
XDIN: Transmit Data In Negative Negative transmit data in for dual rail mode	1101_B
XLT: Transmit Line Tristate control input, low active see XLT	1110_B
reserved	1111_B

Registers PC2 to PC3 have the same layout and description, but the 4 LSBs of PC3 are not used because only 2 MFPs in transmit direction exists.

The bits (3:0) of the register PC3 can be written and read, but are not valid.

Only one of the ports RPA, RPB or RPC must be configured as RTDMT.

Only one of the ports XPA or XPB must be configured as XLT or $\overline{\text{XLT}}$.

The registers PC1, PC2 and PC4 have the reset values ´00_H´, PC3 has the reset value ´$F0_H$´.

The Offset Addresses are listed in **PCn Overview**, for bit names refer to **Port Configuration Registers**.

Table 43 PCn Overview

Register Short Name	Register Long Name	Offset Address	Page Number
PC2	Port Configuration Register 2	$xx81_H$	
PC3	Port Configuration Register 3	$xx82_H$	

Table 44 Port Configuration Registers

	7	6	5	4	3	2	1	0
PC1	RPC13	RPC12	RPC11	RPC10	XPC13	XPC12	XPC11	XPC10
PC2	RPC23	RPC22	RPC21	RPC20	XPC23	XPC22	XPC21	XPC20
PC3	RPC33	RPC32	RPC31	RPC30	XPC33	XPC32	XPC31	XPC30

Port Configuration 5

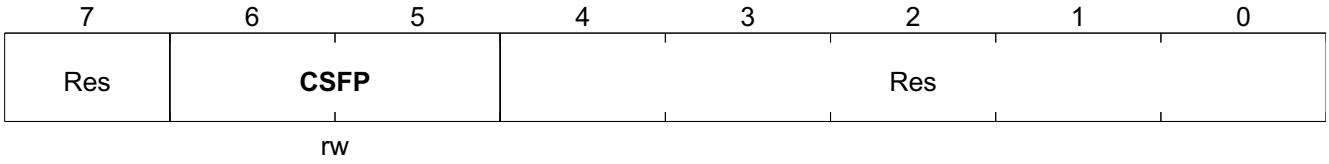
PC5	Offset	Reset Value
Port Configuration 5	$xx84_H$	00_H

7	6	5	4	3	2	1	0
PHDSX	**PHDSR**	Res			**0**	**CSRP**	**CRP**
rw	rw				rw	rw	rw

Field	Bits	Type	Description
PHDSX	7	rw	**Phase Decoder Switch for DCO-X** See formulas in **GCM6**. 0_B , switch phase decoder by 1/3 1_B , switch phase decoder by 1/6
PHDSR	6	rw	**Phase Decoder Switch for DCO-R** See formulas in **GCM6**. 0_B , switch phase decoder by 1/3 1_B , switch phase decoder by 1/6
0	2	rw	**Fixed 0**
CSRP	1	rw	**Configure FCLKR Port** 0_B , FCLKR: Input 1_B , FCLKR: Output
CRP	0	rw	**Configure RCLK Port** 0_B , RCLK: Input 1_B , RCLK: Output

Global Port Configuration 1

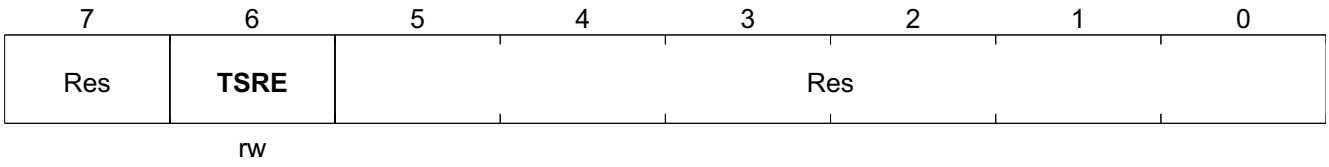
GPC1	Offset	Reset Value
Global Port Configuration 1	0085_H	00_H



Field	Bits	Type	Description
CSFP	6:5	rw	**Configure SEC/FSC Port** The FSC pulse is generated if the DCO-R circuitry of the selected channel is active (CMR2.IRSC = ´1´ or CMR1.RS(1:0) = ´10_b´ or ´11_b´), see **Chapter 3.8.4** 00_B , SEC: Input, active high 01_B , SEC: Output, active high 10_B , FSC: Output, active high 11_B , FSC: Output, active low

Port Configuration 6

PC6	Offset	Reset Value
Port Configuration 6	$xx86_H$	00_H



Field	Bits	Type	Description
TSRE	6	rw	**Transmit Serial Resistor Enable** *Note: See **Table 23** for more details* 0_B , Internal serial resistors are disabled. 1_B , Internal serial resistors are enabled.

Global Port Configuration Register 2

GPC2	Offset	Reset Value
Global Port Configuration Register 2	$008A_H$	00_H

7	6	5	4	3	2	1	0
Res	FSS			Res	R1S		
	rw				rw		

Field	Bits	Type	Description
FSS	6:4	rw	**FSC Source Selection** See **Chapter 3.8.4**. 000_B , FSC sourced by channel 1. 001_B , FSC sourced by channel 2. 010_B , FSC sourced by channel 3. 011_B , FSC sourced by channel 4. 100_B , FSC sourced by channel 5. 101_B , FSC sourced by channel 6. 110_B , FSC sourced by channel 7. 111_B , FSC sourced by channel 8.
R1S	2:0	rw	**RCLK1 Source Selection** See **Chapter 3.7**. 000_B , RCLK1 sourced by channel 1. 001_B , RCLK1 sourced by channel 2. 010_B , RCLK1 sourced by channel 3. 011_B , RCLK1 sourced by channel 4. 100_B , RCLK1 sourced by channel 5. 101_B , RCLK1 sourced by channel 6. 110_B , RCLK1 sourced by channel 7. 111_B , RCLK1 sourced by channel 8.

Global Clock Mode Register 1

GCM1	Offset	Reset Value
Global Clock Mode Register 1	0092_H	00_H

7	6	5	4	3	2	1	0
PHD_E1							
rw							

Field	Bits	Type	Description
PHD_E1	7:0	rw	**Frequency Adjust for E1 lower 8 bits, for highest 4 bits see GCM2)** For details see calculation formulas in register **GCM6** and **Table 45**.

Global Clock Mode Register 2

GCM2	Offset	Reset Value
Global Clock Mode Register 2	0093_H	10_H

7	6	5	4	3	2	1	0
PHSDEM	PHSDIR	PHSDS	VFREQ_EN	PHD_E1			
rw	rw	rw	rw	rw			

Field	Bits	Type	Description
PHSDEM	7	rw	**RX Phase Decoder Demand** 0_B , Default operation 1_B , See formulas in **GCM6**.
PHSDIR	6	rw	**RX Phase Decoder Direction** 0_B , Default operation 1_B , See formulas in **GCM6**.
PHSDS	5	rw	**RX Phase Decoder Switch** 0_B , Default operation 1_B , See formulas in **GCM6**.

Field	Bits	Type	Description
VFREQ_EN	4	rw	**Variable Frequency Enable** If “fixed mode” mode is selected the clock frequency at the pin MCLK must be 2.048 for E1 or 1.544 MHz for T1/J1 respectively. The setting of the whole clock mode is done automatically: Register bits of GCM1, GCM2.PHSDEM, PHDIR, PHSDS, PHD_E1 and GCM3 to GCM8 are unused. If “fixed mode” mode is selected and the SPI- or SCI-interface is used as controller interface, the pinstrapping values at D(15:5) are also not used. See also **Chapter 3.5.5**. *Note: If “fixed mode “ is enabled all of the eight ports must work in the same mode, either in T1 or in E1 mode. A switching between E1 and T1 modes causes a reset of the whole clock system. If “fixed mode“ is disabled a switching between E1 and T1 mode (which can be done in this case individually for every port) causes not a reset of the whole clock system.* 0_B , Fixed clock frequency of 2.048 (E1) or 1.544 MHz (T1/J1) 1_B , Variable master clock frequency (normal operation, operation after reset)
PHD_E1	3:0	rw	**Frequency Adjust for E1** (highest 4 bits, for lower 8 bits see GCM1) The 12 bit frequency adjust value is in the decimal range of -2048 to +2047. Negative values are represented in 2s-complement format. For details see calculation formulas in register **GCM6** and **Table 45**. 100000000000_B, -2048 .....$_B$, 000000000000_B, 0 .....$_B$, 011111111111_B, +2047

Global Clock Mode Register 3

GCM3	Offset	Reset Value
Global Clock Mode Register 3	0094_H	00_H

7	6	5	4	3	2	1	0
PHD_T1							
rw							

Field	Bits	Type	Description
PHD_T1	7:0	rw	**Frequency Adjust for T1** (lower 8 bits, for highest 4 bits see GCM4) The 12 bit frequency adjust value is in the decimal range of -2048 to +2047. Negative values are represented in 2s-complement format. For details see calculation formulas in register **GCM6** and **Table 45**. 100000000000_B, -2048 .....$_B$, 000000000000_B, 0 .....$_B$, 011111111111_B, +2047

Global Clock Mode Register 4

GCM4	Offset	Reset Value
Global Clock Mode Register 4	0095_H	00_H

7	6	5	4	3	2	1	0
DVM_T1			Res	PHD_T1			
rw				rw			

Field	Bits	Type	Description
DVM_T1	7:5	rw	**Divider Mode for T1** This bits can be write and read to be software compatible to QuadLIU, but has no influence on the clock system

Field	Bits	Type	Description
PHD_T1	3:0	rw	**Frequency Adjust for T1** (highest 4 bits, for lower 8 bits see GCM3) The 12 bit frequency adjust value is in the decimal range of -2048 to +2047. Negative values are represented in 2s-complement format. For details see calculation formulas in register **GCM6** and **Table 45**. 100000000000_B, -2048 .....B, 000000000000_B, 0 .....B, 011111111111_B, +2047

Global Clock Mode Register 5

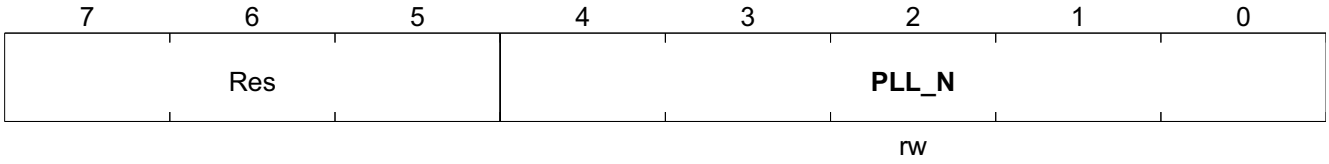
GCM5	Offset	Reset Value
Global Clock Mode Register 5	**0096_H**	**00_H**

7	6	5	4	3	2	1	0
MCLK_LOW	Res		**PLL_M**				
rw			rw				

Field	Bits	Type	Description
MCLK_LOW	7	rw	**Master Clock Range Low** This bit can be write and read to be software compatible to QuadLIU, but has no influence on the clock system.
PLL_M	4:0	rw	**PLL Dividing Factor M** For details see calculation formulas in register **GCM6** and **Table 45**. 00001_B, 1 .....B, 11111_B, 31

Global Clock Mode Register 6

GCM6	Offset	Reset Value
Global Clock Mode Register 6	0097_H	00_H



Field	Bits	Type	Description
PLL_N	4:0	rw	**PLL Dividing Factor N** For details see calculation formulas below and **Table 45**. 000001_B, 1 .....$_B$, 111111_B, 63

Flexible Clock Mode Settings

If “flexible master clock mode” is used (VFREQ_EN = ´1´), the according register settings can be calculated as follows (a windows-based program for automatic calculation is available, see **Chapter 8.3**. For some of the standard frequencies see the table below.

1. The master clock MCLK must be in the following frequency range:

1.02 MHz ≤ f_{MCLK} ≤ 20 MHz

2. Generally the PLL of the master clocking unit includes an input divider with a dividing factor PLL_M +1 and a feedback divider with a dividing factor 4 x (PLL_N +1). So it generates a clock f_{PLL} of about

f_{PLL} = f_{MCLK} x 4 x (PLL_N +1) / (PLL_M +1) .

3. The selection of PLL_N and PLL_M must be done in the following way:

The PLL frequency f_{PLL} must be in the following range:

200 MHz ≤ f_{PLL} ≤ 300 MHz .

The combinations of the values PLL_M and PLL_M must fulfill the equations:

2 MHz ≤ f_{MCLK} / (PLL_M +1) ≤ 6 MHz , if PLL_N is in the range 25 to 63.

5 MHz ≤ f_{MCLK} / (PLL_M +1) ≤ 15 MHz , if PLL_N is in the range 1 to 24.

4. In E1 mode, the selection of PHSN_E1 and PHSX_E1 must be done in such a manner that the frequency for the receiver f_{RX_E1} has nearly the value 16 x f_{DATA_E1} x (1 + 100ppm) = 32.7713 MHz:

f_{RX_E1} = f_{PLL} / {PHSN_E1 + (PHSX_E1 / 6)} .

In T1/J1 mode, the selection of PHSN_T1 and PHSX_T1 must be done in such a manner that the frequency for the receiver f_{RX_T1} has nearly the value 16 x f_{DATA_T1} x (1 + 100ppm) = 24.706 MHz:

f_{RX_T1} = f_{PLL} / {PHSN_T1 + (PHSX_T1 / 6)} .

GCM2.PHSDEM, GCM2.PHSDIR, GCM2.PHSDS, PC5.PHDSX and PC5.PHDSR must be left to ´0´

5. To bring the “characteristic E1 frequency” f_{outE1} exact to 16 x f_{DATA_E1} = 32.7680 MHz a correction value PHD_E1 is necessary:

PHD_E1 = round **(**12288 x { [PHSN_E1 + (PHSX_E1 / 6)] - [f_{pll} / (16 x f_{DATA_E1})] }**)** .

To bring the “characteristic T1 frequency” f_{outT1} exact to 16 x f_{DATA_T1} = 24.704 MHz a correction value PHD_T1 is necessary:

PHD_T1 = round (12288 x { [PHSN_T1 + (PHSX_T1 / 6)] - [f_{pll} / (16 x f_{DATA_T1})] }) .

Example: f_{MCLK} = 2.048 MHz

PLL_N = 33; PLL_M = 0 : f_{PLL} = 278.528 MHz

PHSN_E1 = 8; PHSN_E1 = 2: f_{RX_E1} = 33.42 MHz

PHD_E1 = -2048: f_{outE1} = 32.768 MHz

Table 45 Clock Mode Register Settings for E1 or T1/J1

fMCLK [MHz]	GCM1	GCM2	GCM3	GCM4	GCM5	GCM6	GCM7	GCM8
1.5440	$F0_H$	19_H	00_H	08_H	00_H	$2B_H$	98_H	DA_H
2.0480	00_H	18_H	$D2_H$	$0A_H$	00_H	21_H	$A8_H$	$9B_H$
8.1920	00_H	18_H	$D2_H$	$0A_H$	03_H	21_H	$A8_H$	$9B_H$
12.3520	$F0_H$	19_H	00_H	08_H	07_H	$2B_H$	98_H	DA_H
16.3840	00_H	18_H	$D2_H$	$0A_H$	07_H	21_H	$A8_H$	$9B_H$

Global Clock Mode Register 7

GCM7	Offset	Reset Value
Global Clock Mode Register 7	**0098_H**	**80_H**

7	6	5	4	3	2	1	0
1	**PHSX_E1**			**PHSN_E1**			
r	rw			rw			

Field	Bits	Type	Description
1	7	r	**Fixed ´1´**
PHSX_E1	6:4	rw	**Frequency Adjustment Value E1** For details see calculation formulas in register **GCM6** and **Table 45**. 000_B , 0 ……B , 101_B , 5
PHSN_E1	3:0	rw	**Frequency Adjustment Value E1** For details see calculation formulas in register **GCM6** and **Table 45**. 0001_B, 1 ……B , 1111_B, 15

Global Clock Mode Register 7

GCM8	Offset	Reset Value
Global Clock Mode Register 7	**0099_H**	**80_H**

7	6	5	4	3	2	1	0
1	**PHSX_T1**			**PHSN_T1**			
r	rw			rw			

Field	Bits	Type	Description
1	7	r	**Fixed ´1´**
PHSX_T1	6:4	rw	**Frequency Adjustment value T1** For details see calculation formulas in register **GCM6** and **Table 45**. 000_B , 0 .....B , 101_B , 5
PHSN_T1	3:0	rw	**Frequency Adjustment value T1** For details see calculation formulas in register **GCM6** and **Table 45**. 0001_B, 1 .....B , 1111_B, 15

Global Interrupt Mask Register

GIMR	Offset	Reset Value
Global Interrupt Mask Register	**$00A7_H$**	**FF_H**

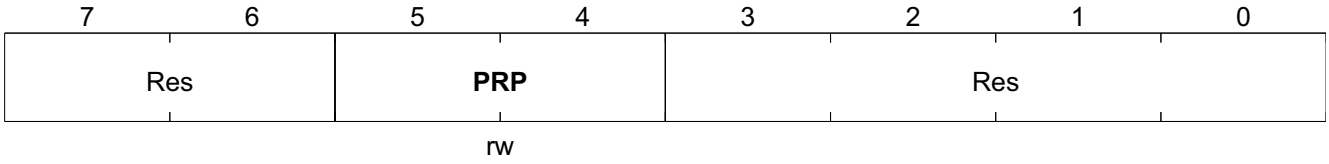
7	6	5	4	3	2	1	0
Res							**PLLL**
							rw

Field	Bits	Type	Description
PLLL	0	rw	**PLL Locked Interrupt Mask** 0_B , GIS2.PLLLC is enabled. 1_B , GIS2.PLLLC is disabled.

Test Pattern Control Register 0

See **Chapter 3.11.1**.

TPC0	Offset	Reset Value
Test Pattern Control Register 0	**xxA8$_H$**	**00$_H$**

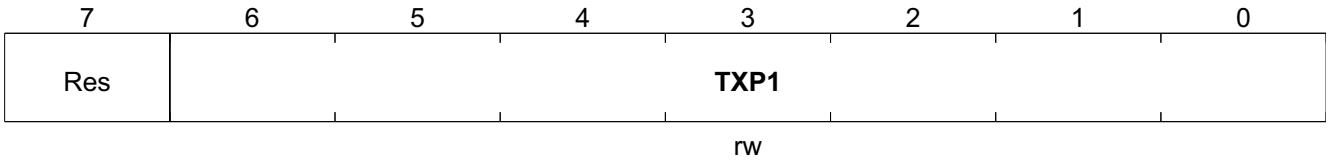


Field	Bits	Type	Description
PRP	5:4	rw	**PRBS Pattern Selection** 00_B , PRBS11 pattern. 01_B , PRBS15 pattern. 10_B , PRBS20 pattern. 11_B , PRBS23 pattern.

TX Pulse Template Register 1

See **Chapter 3.9.6.1** and **Chapter 3.9.6.2**. This register contains the transmit amplitude of the 1st 1/16 of the transmit pulse. The contents of this register is ignored unless bit XPM2.XPDIS is set. By default, the values programmed in XPM0 to XPM2 are used to control the transmit pulse template.

TXP1	Offset	Reset Value
TX Pulse Template Register 1	**xxC1$_H$**	**00$_H$**



Field	Bits	Type	Description
TXP1	6:0	rw	**Transmit Pulse Amplitude** Two´s Complement number of pulse amplitude, see Table 25 and Table 26

Similar Registers

Registers TXP1to TXP16 have the same description and layout. Every register TXPn defines the amplitude of the part n of 16 of the transmit pulse. An overview is given is the next table.

Note that the reset values of the registers TXP1 to TXP8 are ´38$_H$´, that of the registers TXP9 to TXP16 are ´00$_H$´.

Table 46 TXP Overview

Register Short Name	Register Long Name	Offset Address	Page Number
TXP2	TX Pulse Template Register 2	$xxC2_H$	
TXP3	TX Pulse Template Register 3	$xxC3_H$	
TXP4	TX Pulse Template Register 4	$xxC4_H$	
TXP5	TX Pulse Template Register 5	$xxC5_H$	
TXP6	TX Pulse Template Register 6	$xxC6_H$	
TXP7	TX Pulse Template Register 7	$xxC7_H$	
TXP8	TX Pulse Template Register 8	$xxC8_H$	
TXP9	TX Pulse Template Register 9	$xxC9_H$	
TXP10	TX Pulse Template Register 10	$xxCA_H$	
TXP11	TX Pulse Template Register 11	$xxCB_H$	
TXP12	TX Pulse Template Register 12	$xxCC_H$	
TXP13	TX Pulse Template Register 13	$xxCD_H$	
TXP14	TX Pulse Template Register 14	$xxCE_H$	
TXP15	TX Pulse Template Register 15	$xxCF_H$	
TXP16	TX Pulse Template Register 16	$xxD0_H$	

Global Port Configuration Register 3

See **Chapter 3.7**.

GPC3	Offset	Reset Value
Global Port Configuration Register 3	**$00D3_H$**	**21_H**

7	6	5	4	3	2	1	0
Res	**R3S**			Res	**R2S**		
	rw				rw		

Field	Bits	Type	Description
R3S	6:4	rw	**RCLK3 Source Selection** 000_B , RCLK3 sourced by channel 1. 001_B , RCLK3 sourced by channel 2. 010_B , RCLK3 sourced by channel 3. 011_B , RCLK3 sourced by channel 4. 100_B , RCLK3 sourced by channel 5. 101_B , RCLK3 sourced by channel 6. 110_B , RCLK3 sourced by channel 7. 111_B , RCLK3 sourced by channel 8.

Field	Bits	Type	Description
R2S	2:0	rw	**RCLK2 Source Selection** 000_B , RCLK2 sourced by channel 1. 001_B , RCLK2 sourced by channel 2. 010_B , RCLK2 sourced by channel 3. 011_B , RCLK2 sourced by channel 4. 100_B , RCLK2 sourced by channel 5. 101_B , RCLK2 sourced by channel 6. 110_B , RCLK2 sourced by channel 7. 111_B , RCLK2 sourced by channel 8.

Global Port Configuration Register 4

See **Chapter 3.7**.

GPC4	Offset	Reset Value
Global Port Configuration Register 4	**$00D4_H$**	**43_H**

7	6	5	4	3	2	1	0
Res	**R5S**			Res	**R4S**		
	rw				rw		

Field	Bits	Type	Description
R5S	6:4	rw	**RCLK5 Source Selection** 000_B , RCLK5 sourced by channel 1. 001_B , RCLK5 sourced by channel 2. 010_B , RCLK5 sourced by channel 3. 011_B , RCLK5 sourced by channel 4. 100_B , RCLK5 sourced by channel 5. 101_B , RCLK5 sourced by channel 6. 110_B , RCLK5 sourced by channel 7. 111_B , RCLK5 sourced by channel 8.
R4S	2:0	rw	**RCLK4 Source Selection** 000_B , RCLK4 sourced by channel 1. 001_B , RCLK4 sourced by channel 2. 010_B , RCLK4 sourced by channel 3. 011_B , RCLK4 sourced by channel 4. 100_B , RCLK4 sourced by channel 5. 101_B , RCLK4 sourced by channel 6. 110_B , RCLK4 sourced by channel 7. 111_B , RCLK4 sourced by channel 8.

Global Port Configuration Register 5

See **Chapter 3.7**.

GPC5	Offset	Reset Value
Global Port Configuration Register 5	$00D5_H$	65_H

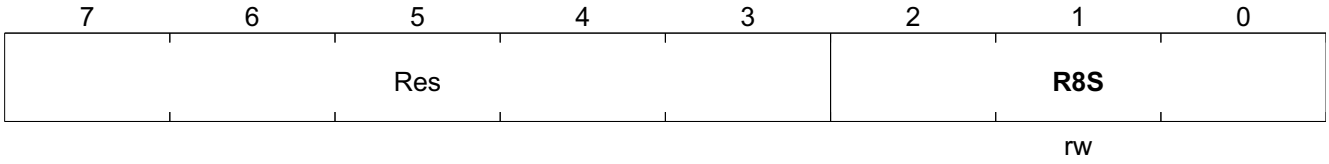
7	6	5	4	3	2	1	0
Res	R7S			Res	R6S		
	rw				rw		

Field	Bits	Type	Description
R7S	6:4	rw	**RCLK7 Source Selection** 000_B , RCLK7 sourced by channel 1. 001_B , RCLK7 sourced by channel 2. 010_B , RCLK7 sourced by channel 3. 011_B , RCLK7 sourced by channel 4. 100_B , RCLK7 sourced by channel 5. 101_B , RCLK7 sourced by channel 6. 110_B , RCLK7 sourced by channel 7. 111_B , RCLK7 sourced by channel 8.
R6S	2:0	rw	**RCLK6 Source Selection** 000_B , RCLK6 sourced by channel 1. 001_B , RCLK6 sourced by channel 2. 010_B , RCLK6 sourced by channel 3. 011_B , RCLK6 sourced by channel 4. 100_B , RCLK6 sourced by channel 5. 101_B , RCLK6 sourced by channel 6. 110_B , RCLK6 sourced by channel 7. 111_B , RCLK6 sourced by channel 8.

Global Port Configuration Register 6

See **Chapter 3.7**.

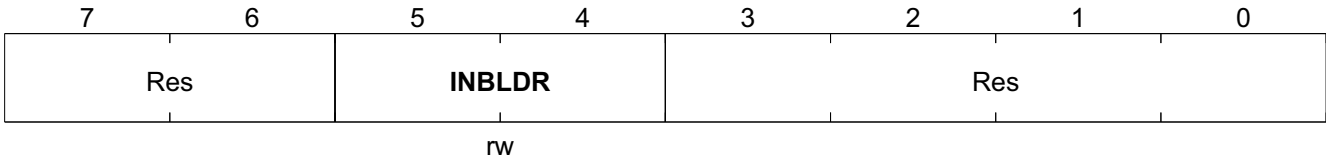
GPC6	Offset	Reset Value
Global Port Configuration Register 6	**$00D6_H$**	**07_H**



Field	Bits	Type	Description
R8S	2:0	rw	**RCLK8 Source Selection** 000_B , RCLK8 sourced by channel 1. 001_B , RCLK8 sourced by channel 2. 010_B , RCLK8 sourced by channel 3. 011_B , RCLK8 sourced by channel 4. 100_B , RCLK8 sourced by channel 5. 101_B , RCLK8 sourced by channel 6. 110_B , RCLK8 sourced by channel 7. 111_B , RCLK8 sourced by channel 8.

In-Band Loop Detection Time Register

INBLDTR	Offset	Reset Value
In-Band Loop Detection Time Register	**$00D7_H$**	**00_H**



Field	Bits	Type	Description
INBLDR	5:4	rw	**In-Band Loop Detection Time for Line Side** See **Chapter 3.11.2**. 00_B , at least 16 consecutive in-band loop pattern must be valid for detection and to perform automatic loop switching. 01_B , at least 32 consecutive in-band loop pattern must be valid for detection and to perform automatic loop switching. 10_B , in-band loop pattern must be valid for at least 4 seconds for detection and to perform automatic loop switching. 11_B , in-band loop pattern must be valid for at least 5 seconds for detection and to perform automatic loop switching.

Automatic Loop Switching Register

Enabling of automatic loop switching by In-band loop codes, see **Chapter 3.11.2**, is performed by this register.

ALS	Offset	Reset Value
Automatic Loop Switching Register	**xxD9$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
Res							**LILS**
							rw

Field	Bits	Type	Description
LILS	0	rw	**Line In-Band Loop Switching (Remote Loop)** This bit controls if automatic switching of the remote loop will be done by In-Band loop codes from the line side, see **Chapter 3.11.2**. *Note: Generation of an interrupt when loop up or down code is detected can be selected by demasking (register IMR6). Setting both, SILS and LILS to ´1´ is forbidden.* 0_B , automatic switching of remote loop (“on line side”) is disabled (default). 1_B , automatic switching of remote loop (“on line side”) by In-band loop codes detected from the line side is enabled if local loop is not activated by LIM0.LL = ´1´.

Interrupt Mask Register 7

Masks interrupt bits of register ISR7.

IMR7	Offset	Reset Value
Interrupt Mask Register 7	**xxDF$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
Res			**XCLKSS1**	**XCLKSS0**	Res		
			rw	rw			

Field	Bits	Type	Description
XCLKSS1	4	rw	**XCLKSS1 Interrupt Masking** 0_B , ISR7.XCLKSS1 is enabled. 1_B , ISR7.XCLKSS1 is disabled
XCLKSS0	3	rw	**XCLKSS0 Interrupt Masking** 0_B , ISR7.XCLKSS0 is enabled. 1_B , ISR7.XCLKSS0 is disabled

LIU Mode Register 3

LIM3	Offset	Reset Value
LIU Mode Register 3	$xxE2_H$	00_H

7	6	5	4	3	2	1	0
Res						DRR	DRX
						rw	rw

Field	Bits	Type	Description
DRR	1	rw	**Dual-Rail mode on digital side, receive direction** 0_B , single rail mode on framer receive side. 1_B , dual rail mode on framer receive side.
DRX	0	rw	**Dual-Rail mode on digital side, transmit direction** 0_B , single rail mode on framer transmit side. 1_B , dual rail mode on framer transmit side.

4.1.2 Status Registers

Receive Buffer Delay

RBD	Offset	Reset Value
Receive Buffer Delay	$xx49_H$	00_H

7	6	5	4	3	2	1	0
Res		RBD					
		r					

Field	Bits	Type	Description
RBD	5:0	r	**Receive Elastic Buffer Delay** These bits informs the user about the current delay (in time slots) through the receive elastic buffer. The delay is updated every 512 or 256 bits (DIC1.RBS(1:0)). Before reading this register the user has to set bit DEC.DRBD in order to halt the current value of this register. After reading RBD updating of this register is enabled. Not valid if the receive buffer is bypassed. 000000_B , Delay < 1 time slot $\cdots_B$, 111111_B , Delay > 63 time slot

Version Status Register

VSTR	Offset	Reset Value
Version Status Register	$004A_H$	$_H$

7	6	5	4	3	2	1	0
VSTR							
r							

Field	Bits	Type	Description
VSTR	7:0	r	**Version Number of Chip** The value is ´20_H´.

Receive Equalizer Status

RES	Offset	Reset Value
Receive Equalizer Status	$xx4B_H$	00_H

7	6	5	4	3	2	1	0
EV		Res	RES				
r			r				

Field	Bits	Type	Description
EV	7:6	r	**Equalizer Status Valid** These bits informs the user about the current state of the receive equalization network. 00_B , Equalizer status not valid, still adapting 01_B , Equalizer status valid 10_B , Equalizer status not valid 11_B , Equalizer status valid but high noise floor
RES	4:0	r	**Receive Equalizer Status** The current line attenuation status in steps of about 1.7 dB for E1 and 1.4 dB for T1/J1 mode are displayed in these bits. Only valid if bits EV(1:0) = ´01_b´. Accuracy: ± 2 digits, based on temperature influence and noise amplitude variations. 00000_B , Minimum attenuation: 0 dB …B , 11001_B , Maximum attenuation: -43 dB (E1), -36 dB (T1/J1)

Line Status Register 0

LSR0	Offset	Reset Value
Line Status Register 0	xx4C$_H$	00$_H$

7	6	5	4	3	2	1	0
LOS	AIS	Res					
r	r						

Field	Bits	Type	Description
LOS	7	r	**Loss-of-Signal** • Detection: This bit is set when the incoming signal has “no transitions” (analog interface) or logical zeros (digital interface) in a time interval of T consecutive pulses, where T is programmable by register PCD. Total account of consecutive pulses: 16 ≤ T ≤ 4096. Analog interface: The receive signal level where “no transition” is declared is defined by the programmed value of LIM1.RIL(2:0). • Recovery: Analog interface: The bit is reset in short-haul mode when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM1.RIL(2:0)) for at least M pulse periods defined by register PCR in the PCD time interval. In long-haul mode additionally bit RES.6 must be set for at least 250 µs. Digital interface: The bit is reset when the incoming data stream contains at least M ones defined by register PCR in the PCD time interval. With the rising edge of this bit an interrupt status bit (ISR2.LOS) is set. The bit is also set during alarm simulation and reset, if MR0.SIM is cleared and no alarm condition exists.
AIS	6	r	**Alarm Indication Signal** The function of this bit is determined by MR0.ALM. • MR0.ALM = ´0´: This bit is set when two or less zeros in the received bit stream are detected in a time interval of 250 ms and the OctalLIU™ is in asynchronous state (LSR0.LFA = ´1´). The bit is reset when no alarm condition is detected (according to ETSI standard). • MR0.ALM = ´1´: This bit is set when the incoming signal has two or less Zeros in each of two consecutive double frame period (512 bits). This bit is cleared when each of two consecutive doubleframe periods contain three or more zeros or when the frame alignment signal FAS has been found. (ITU-T G.775) The bit is also set during alarm simulation and reset if MR0.SIM is cleared and no alarm condition exists.With the rising edge of this bit an interrupt status bit (ISR2.AIS) is set.

Line Status Register 1

LSR1	Offset	Reset Value
Line Status Register 1	$xx4D_H$	xx_H

7	6	5	4	3	2	1	0
EXZD	**PDEN**	Res	**LLBDD**	**LLBAD**	Res	**XLS**	**XLO**
r	r		r	r		r	r

Field	Bits	Type	Description
EXZD	7	r	**Excessive Zeros Detected** Significant only, if excessive zero detection has been enabled (MR0.EXZE = ´1´). Set after detection of more than 3 (HDB3 code) or 15 (AMI code) contiguous zeros in the received data stream.This bit is cleared on read.
PDEN	6	r	**Pulse-Density Violation Detected** The pulse-density of the received data stream is below the requirement defined by ANSI T1. 403 or more than 14 consecutive zeros are detected. With the violation of the pulse-density this bit is set and remains active until the pulse-density requirement is fulfilled for 23 consecutive "1"-pulses. Additionally an interrupt status ISR0.PDEN is generated with the rising edge of PDEN.
LLBDD	4	r	**Line Loop-Back Deactivation Signal Detected, only valid in T1 mode** In E1 mode the equivalent bit is LSR2.LLBDD. This bit is set in case of the LLB deactivate signal is detected and then received over a period of more than 33,16 ms with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}. If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation.Any change of this bit causes an LLBSC interrupt.
LLBAD	3	r	**Line Loop-Back Activation Signal Detected, only valid in T1 mode** In E1 mode the equivalent bit is LSR2.LLBAD. Depending on bit LCR1.EPRM the source of this status bit changed. • LCR1.EPRM = ´0´: This bit is set in case of the LLB activate signal is detected and then received over a period of more than 33,16 ms with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}. If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation. Any change of this bit causes an LLBSC interrupt. • LCR1.EPRM = ´1´: The current status of the PRBS synchronizer is indicated in this bit. It is set high if the synchronous state is reached even in the presence of a bit error rate of up to 10^{-3}. A data stream containing all zeros or all ones with/without framing bits is also a valid pseudo-random binary sequence.

Field	Bits	Type	Description
XLS	1	r	**Transmit Line Short** See **Chapter 3.9.7**. Significant only if the ternary line interface is selected by LIM1.DRS = ´0´. 0_B , Normal operation. No short is detected. 1_B , The XL1 and XL2 are shortened for at least 3 pulses. As a reaction of the short the pins XL1 and XL2 are automatically forced into a high-impedance state if bit XPM2.DAXLT is reset. After 128 consecutive pulse periods the outputs XL1/2 are activated again and the internal transmit current limiter is checked. If a short between XL1/2 is still further active the outputs XL1/2 are in high-impedance state again. When the short disappears pins XL1/2 are activated automatically and this bit is reset. With any change of this bit an interrupt ISR1.XLSC is generated. In case of XPM2.XLT is set this bit is frozen.
XLO	0	r	**Transmit Line Open** See also **Chapter 3.9.7**. 0_B , Normal operation 1_B , This bit is set if at least 32 consecutive zeros were sent on pins XL1/XL2 or XDOP/XDON. This bit is reset with the first transmitted pulse. With the rising edge of this bit an interrupt ISR1.XLSC is set. In case of XPM2.XLT is set this bit is frozen.

Line Status Register 3

LSR3	Offset	Reset Value
Line Status Register 3	**xx4E$_H$**	**xx$_H$**

7	6	5	4	3	2	1	0
ESC			Res				
r							

Field	Bits	Type	Description
ESC	7:5	r	**Error Simulation Counter, T1 only** This three-bit counter is incremented by setting bit MR0.SIM. The state of the counter determines the function to be tested. For complete checking of the alarm indications, eight simulation steps are necessary (LSR3.ESC = ´000_b´ after a complete simulation).

Table 47 Alarm Simulation States

Tested Alarms ESC(2:0) =	0	1	2	3	4	5	6	7
LFA			x				x	
LMFA			x				x	
RRA (bit2 = 0)		x						
RRA (S-bit frame 12)			x					
RRA (DL-pattern)							x	
LOS[1)]		x	x			x		
EBC[2)] (F12,F72)			x				(x)	
EBC[2)] (only ESF)		x	x			x	(x)	
AIS[1)]		x	x			x	x	
FEC[2)]			x				(x)	
CVC		x	x			x		
CEC (only ESF)		x	x			x	x	
RSP		x						
RSN						x		
XSP		x						
XSN						x		
BEC[1)]		x	x			x		
COEC			x				x	

1) Only active during FMR0.SIM = 1

2) FEC is counting +2 while EBC is counting +1 if the framer is in synchronous state; if asynchronous in state 2 but synchronous in state 6, counters are incremented during state 6

Some of these alarm indications are simulated only if the OctalLIU™ is configured in the appropriate mode. At simulation steps 0, 3, 4, and 7 pending status flags are reset automatically and clearing of the error counters and interrupt status registers ISR(7:0) should be done. Incrementing the simulation counter should not be done at time intervals shorter than 1.5 ms (F4, F12, F72) or 3 ms (ESF). Otherwise, reactions of initiated simulations might occur at later steps. Control bit FMR0.SIM has to be held stable at high or low level for at least one receive clock period before changing it again.

Line Status Register 2

LSR2	Offset	Reset Value
Line Status Register 2	$xx4F_H$	xx_H

7	6	5	4	3	2	1	0
Res			LLBDD	LLBAD	Res		
			r	r			

Field	Bits	Type	Description
LLBDD	4	r	**Line Loop-Back Deactivation Signal Detected, only valid in E1 mode** In T1/J1 mode the equivalent bit is LSR1.LLBDD. This bit is set in case of the LLB deactivate signal is detected and then received over a period of more than 25 ms with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}. If framing is aligned, the time slot 0 is not taken into account for the error rate calculation.Any change of this bit causes an LLBSC interrupt.
LLBAD	3	r	**Line Loop-Back Activation Signal Detected, only valid in E1 mode** In T1/J1 mode the equivalent bit is LSR1.LLBAD. Depending on bit LCR1.EPRM the source of this status bit changed. • LCR1.EPRM = ´0´: This bit is set in case of the LLB activate signal is detected and then received over a period of more than 25 ms with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}. If framing is aligned, the time slot 0 is not taken into account for the error rate calculation. Any change of this bit causes an LLBSC interrupt. • LCR1.EPRM = ´1´: The current status of the PRBS synchronizer is indicated in this bit. It is set high if the synchronous state is reached even in the presence of a bit error rate of 10^{-1}. A data stream containing all zeros or all ones with/without framing bits is also a valid pseudo-random binary sequence.

Code Violation Counter Lower Byte

CVCL	Offset	Reset Value
Code Violation Counter Lower Byte	$xx52_H$	00_H

7	6	5	4	3	2	1	0
CV7	CV6	CV5	CV4	CV3	CV2	CV1	CV0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CV7	7	r	**Code Violations** If the HDB3 or the CMI code with HDB3-precoding is selected, the 16-bit counter is incremented when violations of the HDB3 code are detected. The error detection mode is determined by programming the bit MR0.EXTD. If simple AMI coding is enabled (MR0.RC(1:0) = ´01_b´) all bipolar violations are counted. The error counter does not roll over.During alarm simulation, the counter is incremented every four bits received up to its saturation. Clearing and updating the counter is done according to bit MR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCVC is reset automatically with reading the error counter high byte. If MR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
CV6	6	r	
CV5	5	r	
CV4	4	r	
CV3	3	r	
CV2	2	r	
CV1	1	r	
CV0	0	r	

Code Violation Counter Higher Byte

CVCH	Offset	Reset Value
Code Violation Counter Higher Byte	$xx53_H$	00_H

7	6	5	4	3	2	1	0
CV15	CV14	CV13	CV12	CV11	CV10	CV9	CV8
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CV15	7	r	**Code Violations** If the HDB3 or the CMI code with HDB3-precoding is selected, the 16-bit counter is incremented when violations of the HDB3 code are detected. The error detection mode is determined by programming the bit MR0.EXTD. If simple AMI coding is enabled (MR0.RC(1:0) = ´01_b´) all bipolar violations are counted. The error counter does not roll over.During alarm simulation, the counter is incremented every four bits received up to its saturation. Clearing and updating the counter is done according to bit MR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCVC is reset automatically with reading the error counter high byte. If MR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
CV14	6	r	
CV13	5	r	
CV12	4	r	
CV11	3	r	
CV10	2	r	
CV9	1	r	
CV8	0	r	

PRBS Bit Error Counter Lower Bytes

BECL	Offset	Reset Value
PRBS Bit Error Counter Lower Bytes	$xx58_H$	00_H

7	6	5	4	3	2	1	0
BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
BEC7	7	r	**PRBS Bit Error Counter** If the PRBS monitor is enabled by LCR1.EPRM = ´1´ this 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state LSR1.LLBAD = ´1´. The error counter does not roll over.During alarm simulation, the counter is incremented continuously with every second received bit. Clearing and updating the counter is done according to bit MR1.ECM.If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the PRBS bit error counter bit DEC.DBEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DBEC is automatically reset with reading the error counter high byte. If MR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
BEC6	6	r	
BEC5	5	r	
BEC4	4	r	
BEC3	3	r	
BEC2	2	r	
BEC1	1	r	
BEC0	0	r	

PRBS Bit Error Counter Higher Bytes

BECH	Offset	Reset Value
PRBS Bit Error Counter Higher Bytes	$xx59_H$	00_H

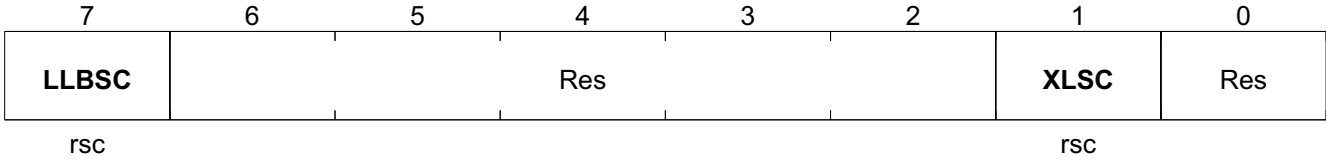
7	6	5	4	3	2	1	0
BEC15	**BEC14**	**BEC13**	**BEC12**	**BEC11**	**BEC10**	**BEC9**	**BEC8**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
BEC15	7	r	**PRBS Bit Error Counter** If the PRBS monitor is enabled by LCR1.EPRM = ´1´ this 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state LSR1.LLBAD = ´1´. The error counter does not roll over.During alarm simulation, the counter is incremented continuously with every second received bit. Clearing and updating the counter is done according to bit MR1.ECM.If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the PRBS bit error counter bit DEC.DBEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DBEC is automatically reset with reading the error counter high byte. If MR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.
BEC14	6	r	
BEC13	5	r	
BEC12	4	r	
BEC11	3	r	
BEC10	2	r	
BEC9	1	r	
BEC8	0	r	

Interrupt Status Register 1

All bits are reset when ISR1 is read. If bit GCR.VIS is set, interrupt statuses in ISR1 are flagged although they are masked by register IMR1. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS, see **Chapter 3.5.3**.

ISR1	Offset	Reset Value
Interrupt Status Register 1	**xx69$_H$**	**00$_H$**



Field	Bits	Type	Description
LLBSC	7	rsc	**Line Loop-Back Status Change, E1 only** In T1/J1 mode this bit is not valid and ISR3.LLBSC is used instead. Depending on bit LCR1.EPRM the source of this interrupt status changed: • LCR1.EPRM = 0: This bit is set, if the LLB activate signal or the LLB deactivate signal, respectively, is detected over a period of 25 ms with a bit error rate less than 10^{-2}. The LLBSC bit is also set, if the current detection status is left, i.e., if the bit error rate exceeds 10^{-2}. The actual detection status can be read from the LSR2.LLBAD / LSR2.LLBDD in E1 or LSR1.LLBAD / LSR1.LLBDD in T1/J1 mode, respectively. • PRBS Status Change LCR1.EPRM = ´1´: With any change of state of the PRBS synchronizer this bit is set. The current status of the PRBS synchronizer is indicated in LSR2.LLBAD (E1) or LSR1.LLBAD (T1/J1).
XLSC	1	rsc	**Transmit Line Status Change** XLSC is set with the rising edge of the bit LSR1.XLO or with any change of bit LSR1.XLS. The actual status of the transmit line monitor can be read from the LSR1.XLS and LSR1.XLO.

Interrupt Status Register 2

All bits are reset when ISR2 is read. If bit GCR.VIS is set, interrupt statuses in ISR2 are flagged although they are masked by register IMR2. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS. See **Chapter 3.5.3**

ISR2	Offset	Reset Value
Interrupt Status Register 2	**xx6A$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
Res				**AIS**	**LOS**	Res	
				r	r		

Field	Bits	Type	Description
AIS	3	r	**Alarm Indication Signal (Blue Alarm)** This bit is set when an alarm indication signal is detected and bit LSR0.AIS is set. If GCR.SCI is set high this interrupt status bit is activated with every change of state of LSR0.AIS.It is set during alarm simulation.
LOS	2	r	**Loss-of-Signal (Red Alarm)** This bit is set when a loss-of-signal alarm is detected in the received data stream and LSR0.LOS is set. If GCR.SCI is set high this interrupt status bit is activated with every change of state of LSR0.LOS. It is set during alarm simulation.

Interrupt Status Register 3

All bits are reset when ISR3 is read. If bit GCR.VIS is set, interrupt statuses in ISR3 are flagged although they are masked by register IMR3. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS, see **Chapter 3.5.3**.

ISR3	Offset	Reset Value
Interrupt Status Register 3	**xx6B$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
Res	**SEC**	Res		**LLBSC**	Res	**RSN**	**RSP**
	rsc			rsc		rsc	rcs

Field	Bits	Type	Description
SEC	6	rsc	**Second Timer** The internal one-second timer has expired. The timer is derived from clock RCLK or external pin SEC/FSC.

Field	Bits	Type	Description
LLBSC	3	rsc	**Line Loop-Back Status Change, T1/J1 only** In E1 mode this bit is not valid and ISR1.LLBSC is used instead. Depending on bit LCR1.EPRM the source of this interrupt status changed: • LCR1.EPRM = 0: This bit is set, if the LLB activate signal or the LLB deactivate signal, respectively, is detected over a period of 25 ms with a bit error rate less than 10^{-2}. The LLBSC bit is also set, if the current detection status is left, i.e., if the bit error rate exceeds 10^{-2}. The actual detection status can be read from the LSR2.LLBAD / LSR2.LLBDD in E1 or LSR1.LLBAD / LSR1.LLBDD in T1/J1 mode, respectively. • PRBS Status Change LCR1.EPRM = ´1´: With any change of state of the PRBS synchronizer this bit is set. The current status of the PRBS synchronizer is indicated in LSR2.LLBAD (E1) or LSR1.LLBAD (T1/J1).
RSN	1	rsc	**Receive Slip Negative** The frequency of the receive route clock is greater than the frequency of the receive system interface working clock based on 2.048 MHz. A frame is skipped. It is set during alarm simulation. See **Chapter 3.7.10**.
RSP	0	rcs	**Receive Slip Positive** The frequency of the receive route clock is less than the frequency of the receive system interface working clock based on 2.048 MHz. A frame is repeated. It is set during alarm simulation. See **Chapter 3.7.10**.

Interrupt Status Register 4

All bits are reset when ISR4 is read. If bit GCR.VIS is set, interrupt statuses in ISR4 are flagged although they are masked by register IMR4. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS, see **Chapter 3.5.3**.

ISR4	Offset	Reset Value
Interrupt Status Register 4	**xx6C$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
XSP	**XSN**	Res					
rsc	rsc						

Field	Bits	Type	Description
XSP	7	rsc	**Transmit Slip Positive** The frequency of the transmit clock is less than the frequency of the transmit system interface working clock based on 2.048 MHz. A frame is repeated. After a slip has performed writing of register XC1 is not necessary.

Field	Bits	Type	Description
XSN	6	rsc	**Transmit Slip Negative** The frequency of the transmit clock is greater than the frequency of the transmit system interface working clock based on 2.048 MHz. A frame is skipped. After a slip has performed writing of register XC1 is not necessary.

Global Interrupt Status Register

This status register points to pending interrupts sourced by ISR(1:4) and ISR(6:7), see **Chapter 3.5.3**.

GIS	Offset	Reset Value
Global Interrupt Status Register	**xx6E$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
ISR7	**ISR6**	**ISR5**	**ISR4**	**ISR3**	**ISR2**	**ISR1**	**ISR0**
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
ISR7	7	rsc	**Interrupt Status Register 7 Pointer** 0_B , No interrupt is pending in ISR6. 1_B , At least one interrupt is pending in ISR6.
ISR6	6	rsc	**Interrupt Status Register 6 Pointer** 0_B , No interrupt is pending in ISR6. 1_B , At least one interrupt is pending in ISR6.
ISR5	5	rsc	**Interrupt Status Register 5 Pointer** Always ´0´, because no ISR5 exists
ISR4	4	rsc	**Interrupt Status Register 4 Pointer** 0_B , No interrupt is pending in ISR4. 1_B , At least one interrupt is pending in ISR4.
ISR3	3	rsc	**Interrupt Status Register 3 Pointer** 0_B , No interrupt is pending in ISR3. 1_B , At least one interrupt is pending in ISR3.
ISR2	2	rsc	**Interrupt Status Register 2 Pointer** 0_B , No interrupt is pending in ISR2. 1_B , At least one interrupt is pending in ISR2.
ISR1	1	rsc	**Interrupt Status Register 1 Pointer** 0_B , No interrupt is pending in ISR1. 1_B , At least one interrupt is pending in ISR1.
ISR0	0	rsc	**Interrupt Status Register 0 Pointer** Always ´0´, because no ISR0 exists.

Channel Interrupt Status Register

This status register points to pending interrupts of channels 1to 8, see Chapter 3.5.3.

CIS	Offset	Reset Value
Channel Interrupt Status Register	$006F_H$	00_H

7	6	5	4	3	2	1	0
GIS8	GIS7	GIS6	GIS5	GIS4	GIS3	GIS2	GIS1
rsc	rsc	rsc	rsc	rsc	rsc	rsc	rsc

Field	Bits	Type	Description
GIS8	7	rsc	**GIS 8: Global Interrupt Status of Channel 8** 0_B , no interrupt is pending on channel 8. 1_B , at least one interrupt is pending on channel 8, read GIS of channel 8 for more information.
GIS7	6	rsc	**Global Interrupt Status of Channel 7** 0_B , no interrupt is pending on channel 7. 1_B , at least one interrupt is pending on channel 7, read GIS of channel 7 for more information.
GIS6	5	rsc	**Global Interrupt Status of Channel 6** 0_B , no interrupt is pending on channel 6. 1_B , at least one interrupt is pending on channel 6, read GIS of channel 6 for more information.
GIS5	4	rsc	**Global Interrupt Status of Channel 5** 0_B , no interrupt is pending on channel 5. 1_B , at least one interrupt is pending on channel 5, read GIS of channel 5 for more information.
GIS4	3	rsc	**Global Interrupt Status of Channel 4** 0_B , no interrupt is pending on channel 4. 1_B , at least one interrupt is pending on channel 4, read GIS of channel 4 for more information.
GIS3	2	rsc	**Global Interrupt Status of Channel 3** 0_B , no interrupt is pending on channel 3. 1_B , at least one interrupt is pending on channel 3, read GIS of channel 3 for more information.
GIS2	1	rsc	**Global Interrupt Status of Channel 2** 0_B , no interrupt is pending on channel 2. 1_B , at least one interrupt is pending on channel 2, read GIS of channel 2 for more information.
GIS1	0	rsc	**Global Interrupt Status of Channel 1** 0_B , no interrupt is pending on channel 1. 1_B , at least one interrupt is pending on channel 1, read GIS of channel 1 for more information.

Multi Function Port Input Register

This register always reflects the state of the multi function ports, see **Chapter 3.12**. If used as an input, the according port should be switched to general purpose input mode. If not, the programmed output signal can be monitored through this register (see registers PC1 to PC3).

MFPI	Offset	Reset Value
Multi Function Port Input Register	**$xxAB_H$**	**xx_H**

7	6	5	4	3	2	1	0
Res	**RPC**	**RPB**	**RPA**	Res		**XPB**	**XPA**
	r	r	r			r	r

Field	Bits	Type	Description
RPC	6	r	**RPC Input Level** 0_B , Low level on pin RPC. 1_B , High level on pin RPC.
RPB	5	r	**RPB Input Level** 0_B , Low level on pin RPB. 1_B , High level on pin RPB.
RPA	4	r	**RPA Input Level** 0_B , Low level on pin RPA. 1_B , High level on pin RPA.
XPB	1	r	**XPB Input Level** 0_B , Low level on pin XPB. 1_B , High level on pin XPB.
XPA	0	r	**XPA Input Level** 0_B , Low level on pin XPA. 1_B , High level on pin XPA.

Interrupt Status Register 6

ISR6	Offset	Reset Value
Interrupt Status Register 6	$xxAC_H$	00_H

7	6	5	4	3	2	1	0
Res						LILSU	LILSD
						rsc	rsc

Field	Bits	Type	Description
LILSU	1	rsc	**Line In-Band Loop Switching Up Interrupt** See **Chapter 3.11.2**. 0_B , no line loop up code detected. 1_B , line loop up code detected and line loop is switched on if ALS.LILS is set.
LILSD	0	rsc	**Line In-Band Loop Switching Down Interrupt** See **Chapter 3.11.2**. 0_B , no line loop down code detected. 1_B , line loop down code detected and line loop is switched off if ALS.LILS is set.

Global Interrupt Status 2

Interrupt status register for the PLL of the master clocking unit.

GIS2	Offset	Reset Value
Global Interrupt Status 2	$00AD_H$	00_H

7	6	5	4	3	2	1	0
Res						PLLLS	PLLLC
						r	rsc

Field	Bits	Type	Description
PLLLS	1	r	**PLL Locked Status Information** *Note: PLLLS is only a status bit, not an interrupt status bit, so type is r and not rsc. This bit is valid independent on value of COMP. For COMP = ´0´ this bit must be used instead of bit 7 of register CIS which has then the function GIS8.* 0_B , PLL is unlocked. 1_B , PLL is locked

Field	Bits	Type	Description
PLLLC	0	rsc	**PLL Locked Status Change** 0_B , No change of PLL lock status since last read of this register. 1_B , PLL lock status has changed since last read. Status information is available in bit PLLLS.

Interrupt Status Register 7

All bits are reset when ISR7 is read. If bit GCR.VIS is set, interrupt statuses in ISR7 are flagged although they are masked by register IMR7. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS, see **Chapter 3.5.3**.

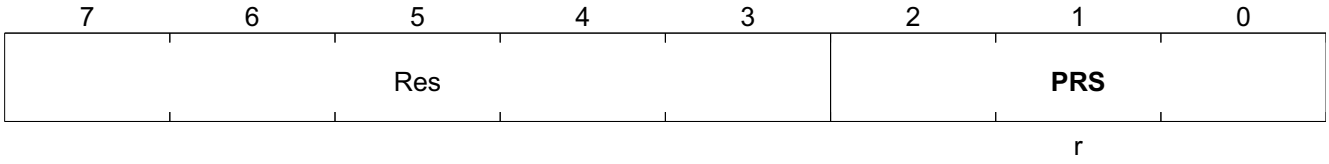
ISR7	Offset	Reset Value
Interrupt Status Register 7	**xxD8$_H$**	**00$_H$**

7	6	5	4	3	2	1	0
Res			**XCLKSS1**	**XCLKSS0**	Res		
			rsc	rsc			

Field	Bits	Type	Description
XCLKSS1	4	rsc	**XCLK Source Switched 1** See **Chapter 3.9.3**. Shows if an automatically switching of the DCO-X reference between TCLK and FCLKX was performed. If automatically switching is not enabled (CMR6.ATCS = ´0´), this bit is always ´0´. Note that the status of TCLK is shown independent on CMR6.ATC in **CLKSTAT**.TCLKLOS. 0_B , DCO-X reference not switched. 1_B , DCO-X reference has switched between TCLK and FCLKX. The XCLK is always sourced by the DCO-X output.
XCLKSS0	3	rsc	**XCLK Source Switched 0** See **Chapter 3.9.3**. Shows if an automatically switching of the XCLK source between TCLK and DCO-X output was performed. If automatically switching is not enabled (CMR6.ATCS = ´0´), this bit is always ´0´. Note that the status of TCLK is shown independent on CMR6.ATC in **CLKSTAT**.TCLKLOS. 0_B , XCLK source not switched. 1_B , XCLK source has switched automatically from TCLK to DCO-X output in case of TCLK loss or automatically switched back from DCO-X output to TCLK in case that TCLK is active again. The DCO-X is always sourced by FCLKX.

PRBS Status Register

PRBSSTA	Offset	Reset Value
PRBS Status Register	$xxDA_H$	$0x_H$



Field	Bits	Type	Description
PRS	2:0	r	**PRBS Status Information** *Note: Every change of the bits PRS sets the interrupt bit ISR1.LLBSC if register bit LCR1.EPRM is set. No pattern is also detected if signal "alarm simulation" is active. Detection of all_zero or all_ones is done over 12, 16, 21 or 24 consecutive bits, dependent on the choosed PRBS polynomial (11, 15, 20 or 23). Because every bit error in the PRBS increments the bit error counter BEC, no special status information like "PRBS detected with errors" is given here* 000_B , No pattern detected. 001_B , Reserved. 010_B , PRBS pattern detected. 011_B , Inverted PRBS pattern detected. 100_B , Reserved. 101_B , Reserved. 110_B , All-zero pattern detected. 111_B , All-ones pattern detected.

Clock Status Register

The bits show the current status of the input clocks TCLK and FCLKX.

CLKSTAT	Offset	Reset Value
Clock Status Register	$xxFE_H$	xx_H

7	6	5	4	3	2	1	0
Res			TCLKLOS	FCLKXLOS	Res		
			r	r			

Field	Bits	Type	Description
TCLKLOS	4	r	**Loss of TCLK** Status of TCLK. *Note: See **Chapter 3.9.3** for more detail.* 0_B , TCLK is active. 1_B , TCLK is lossed.
FCLKXLOS	3	r	**Loss of FCLKX** Status of FCLKX. *Note: See **Chapter 3.9.3** for more detail.* 0_B , FCLKX is active. 1_B , FCLKX is lossed.

5 Package Outlines

Figure 39 shows the package outline.

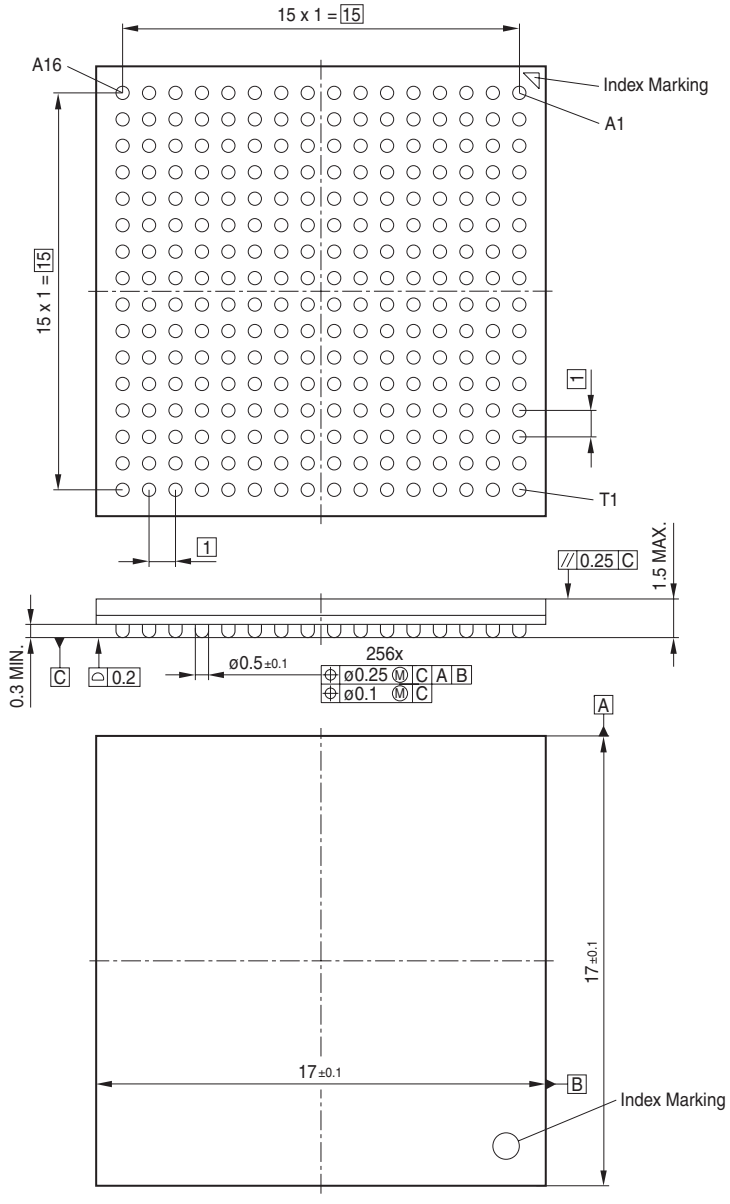


Figure 39 PG-LBGA-256-1 (Plastic Low Profile Ball Grid Array Package), SMD

Dimensions in mm

Note: The upper drawing shows the “Bottom View” of the package.

6 Electrical Characteristics

In Table 48 the absolute maximum ratings of the OctalLIUTM are listed.

Table 48 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient temperature under bias	T_A	-40	–	85	°C	–
Storage temperature	T_{stg}	-65	–	125	°C	–
Moisture Level 3 temperature	T_{ML3}	–	–	225	°C	According to IPS J-STD 020
		–	–	245	°C	According to Infineon internal standard
IC supply voltage (pads, digital)	V_{DD}	-0.5	3.3	4.5	V	–
IC supply voltage (core, digital)	V_{DDC}	-0.5	1.8	2.4	V	–
IC supply voltage receive (analog)	V_{DDR}	-0.4	–	4.5	V	–
IC supply voltage transmit (analog)	V_{DDX}	-0.4	–	4.5	V	–
Receiver input signal with respect to ground	V_{RLmax}	-0.8	–	4.5	V	RL1, RL2
Voltage on any pin with respect to ground	V_{max}	-0.4	–	4.5	V	Except RL1, RL2
ESD robustness[1] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	–	–	2000	V	[2]
ESD robustness[3] CDM	$V_{ESD,CDM}$	–	–	500	V	–

1) According to JEDEC standard JESD22-A114.
2) For RL1 and RL2 1500 V
3) According to ESD Association Standard DS5.3.1 - 1999

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 49 defines the maximum values of voltages and temperature which may be applied to guarantee proper operation of the OctalLIUTM.

Table 49 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient temperature	T_A	-40	–	85	°C	–
Supply voltage digital pads	V_{DD}	3.13	3.30	3.46	V	3.3 V ± 5%[1]
Supply voltage digital core	V_{DDC}	1.62	1.80	1.98	V	1.8 V ± 10% [1]
Supply voltage analog receiver	V_{DDR}	3.13	3.30	3.46	V	3.3 V ± 5% [1]
Supply voltage analog transmitter	V_{DDX}	3.13	3.30	3.46	V	3.3 V ± 5% [1]
Analog input voltages	V_{RL}	0	–	V_{DDR}+0.3	V	RL1, RL2
Digital input voltages	V_{ID}	-0.4	–	3.46	V	V_{DD} = 3.3 V ±5 %
Ground	V_{SS} V_{SSR} V_{SSX}	0	–	0	V	–

1) Voltage ripple on analog supply less than 50 mV

Note: In the operating range, the functions given in the circuit description are fulfilled.
V_{DD}, V_{DDR} and V_{DDX} have to be connected to the same voltage level,
V_{SS}, V_{SSR} and V_{SSX} have to be connected to ground level.

Table 50 DC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage	V_{IL}	-0.4	–	0.8	V	[1]
Input high voltage	V_{IH}	2.0	–	3.46	V	[1]
Output low voltage	V_{OL}	V_{SS}	–	0.45	V	I_{OL} = +2 mA[2]
Output high voltage	V_{OH}	2.4	–	V_{DD}	V	I_{OH} = -2 mA [2]
Average power supply current at 1.8 V supply (analog line interface mode)	I_{DD18E1}	–	–	300	mA	E1 application [3]LIM1.DRS = ´0´, PRBS pattern; 2 MHz at framer interface
	I_{DD18T1}	–	–	250	mA	T1 application [3] LIM1.DRS = ´0´, PRBS pattern; 1.5 MHz at framer interface
Average power supply current at 3.3 V supply (analog line interface mode)	I_{DD33E1}	–	–	370	mA	E1 application [3] LIM1.DRS = ´0´, PRBS pattern; 2 MHz at system interface
	I_{DD33T1}	–	–	370	mA	T1 application [3] LIM1.DRS = ´0´, PRBS pattern; 1.5 MHz at system interface
Average power supply current at 1.8 V supply (digital line interface mode)	I_{DD18E1}	–	–	350	mA	E1 application [3] LIM1.DRS = ´1´, PRBS pattern; 16 MHz at system interface
Average power supply current at 3.3 V supply (digital line interface mode)	I_{DD33T1}	–	–	25	mA	E1 application [3] LIM1.DRS = ´1´, PRBS pattern; 16 MHz at system interface
Input leakage current	I_{IL11}	–	–	1	µA	V_{IN} =V_{DD} [4]; all except RDO

Table 50 DC Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{IL12}	–	–	1	µA	$V_{IN} = V_{SS}$ 3); all except RDO
Input pullup current	I_{IP}	2	–	15	µA	$V_{IN} = V_{SS}$
Output leakage current	I_{OZ1}	–	–	1	µA	V_{OUT} = tristate 1) $V_{SS} < V_{meas} < V_{DD}$measured against V_{DD} and V_{SS}; all except XL1/2
Transmitter leakage current	I_{TL}	–	–	30	µA	XL1/2 = V_{DDX}; XPM2.XLT = ´1´
		–	–	30	µA	XL1/2 = V_{SSX}; XPM2.XLT = ´1´
Transmitter output impedance	R_X	–	–	3	Ω	Applies to XL1and XL2 5)
Transmitter output current	I_X	–	–	105	mA	XL1, XL2
Differential peak voltage of a mark (between XL1 and XL2)	V_X	–	–	2.15	V	–
Receiver peak voltage of a mark (at RL1 or RL2)	V_{RL12}	-0.45	–	3.8	V	RL1, RL2
		-0.75	–	4.1	V	RZ signals; must only be applied during T1 pulse over/undershoot according to ANSI T1.403-1999
Receiver differential peak voltage of a mark (between RL1 and RL2)	V_{RL12}	–	–	4.0	V	RL1, RL2
		–	–	4.63	V	RZ signals; must only be applied during T1 pulse over/undershoot according to ANSI T1.403-1999
Receiver input impedance	Z_R	–	50	–	kΩ	5)
Receiver sensitivity	S_{RSH}	0	–	10	dB	RL1, RL2 LIM0.EQON = ´0´ (short-haul)
Receiver sensitivity -	S_{RLH}	-43	–	0	dB	RL1, RL2 LIM0.EQON = ´1´ (E1, long-haul)
		-36	–	0	dB	RL1, RL2 LIM0.EQON = ´1´ (T1/J1, long-haul)
Receiver input threshold	V_{RTH}	–	45	–	%	LIM2.SLT(1:0) = $´11_b´$ 5)
		–	50	–	%	LIM2.SLT(1:0) = $´10_b´$ 5) default setting
		–	55	–	%	LIM2.SLT(1:0) = $´00_b´$ 5)
		–	67	–	%	LIM2.SLT(1:0) = $´01_b´$ 5)
Multi Purpose Analog Switch	R_{DSON}	2.7	–	7.1	Ω	–
	R_{DSOFF}	100	–	–	kΩ	–
	R_{DSONDC}	–	–	2	mA	@ 125 °C
	R_{DSON}	–	–	25	mA	@ 50% duty cycle

Table 50 DC Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Loss-Of-signal (LOS) detection limit	V_{LOS}	1560	–	1710	mV	RIL(2:0) = ´000_b´ 5)
		790	–	960	mV	RIL(2:0) = ´001_b´ 5)
		430	–	500	mV	RIL(2:0) = ´010_b´ 6)
		220	–	260	mV	RIL(2:0) = ´011_b´ 5)
		125	–	130	mV	RIL(2:0) = ´100_b´ 5)
		65	–	70	mV	RIL(2:0) = ´101_b´ 5)
		35	–	40	mV	RIL(2:0) = ´110_b´ 5)
		10	–	15	mV	RIL(2:0) = ´111_b´ 5)

1) Applies to all input pins except analog pins RLx
2) Applies to all output pins except pins XLx
3) Wiring conditions and external circuit configuration according to **Figure 58** and **Table 66**.
4) Pin leakage is measured in a test mode with all internal pullups disabled. RDO pins are not tristatable, no leakage is measured.
5) Parameter not tested in production
6) Value measured in production to fulfil ITU-T G.775

Note: Typical characteristics specify mean values expected over the production spread. If not specified otherwise, typical characteristics apply at T_A = 25 °C and 3.3 V supply voltage.

6.1 AC Characteristics

6.1.1 Master Clock Timing

Figure 40 shows the timing and Table 51 the appropriate timing parameter values of the master clock at the pin MCLK. The accuracy is required to fulfill the jitter requirements, see Chapter 3.7.9.1 and Chapter 3.9.4.

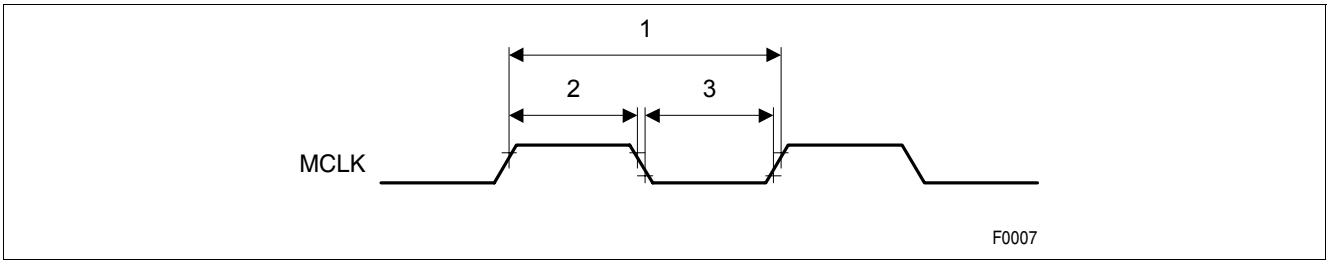


Figure 40 MCLK Timing

Table 51 MCLK Timing Parameter Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period of MCLK	1	–	488	–	ns	E1, fixed mode
		–	648	–	ns	T1/J1, fixed mode
		50	–	980.4	ns	E1/T1/J1, flexible mode
High phase of MCLK	2	40	–	–	%	–
Low phase of MCLK	3	40	–	–	%	–
Clock accuracy	–	32[1)]	–	28[2)]	ppm	–

1) If clock divider programming fits without rounding
2) If clock divider programming requires rounding

6.1.2 JTAG Boundary Scan Interface

Figure 41 shows the timing and Table 52 the appropriate timing parameter values at the JTAG pins to perform a boundary scan test of the OctalLIUTM, see Chapter 3.5.4.

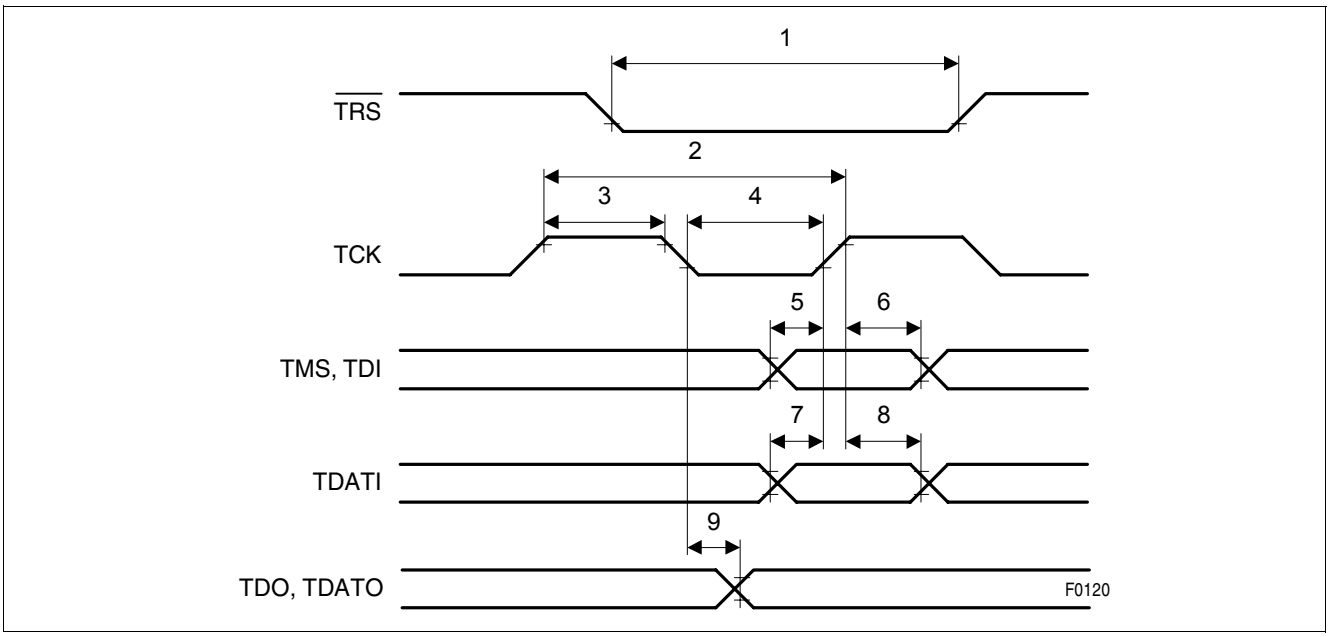


Figure 41 JTAG Boundary Scan Timing

Table 52 JTAG Boundary Scan Timing Parameter Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\overline{\text{TRS}}$ reset active low time	1	200	–	–	ns	–
TCK period	2	250	–	–	ns	–
TCK high time	3	80	–	–	ns	–
TCK low time	4	80	–	–	ns	–
TMS, TDI setup time	5	40	–	–	ns	–
TMS, TDI hold time	6	40	–	–	ns	–
TDATI setup time	7	40	–	–	ns	–
TDATI hold time	8	40	–	–	ns	–
TDO, TDATO output delay	9	–	–	100	ns	–

6.1.3 Reset

Figure 42 shows the timing and Table 53 the appropriate timing parameter value at the pin $\overline{RES}$ to perform a reset of the OctalLIUTM.

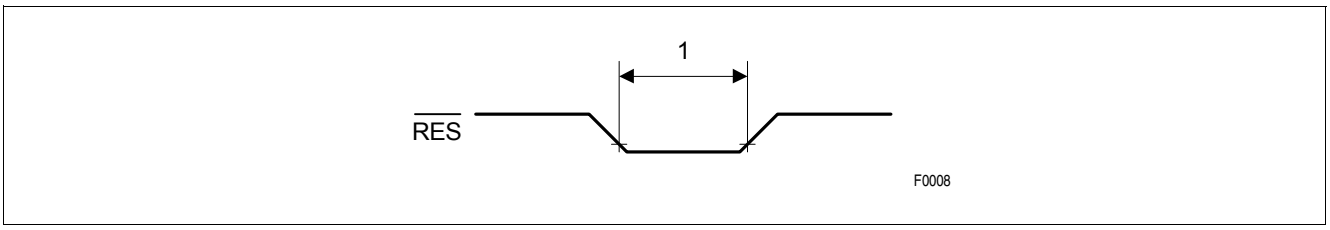


Figure 42 Reset Timing

Table 53 Reset Timing Parameter Value

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\overline{RES}$ pulse width low	1	10[1)]	–	–	µs	–

1) While MCLK is running

6.1.4 Asynchronous Microprocessor Interface

6.1.4.1 Intel Bus Interface Mode

Figure 43 to Figure 46 show the timing of the SCI Interface and Table 54 the appropriate timing parameter values.

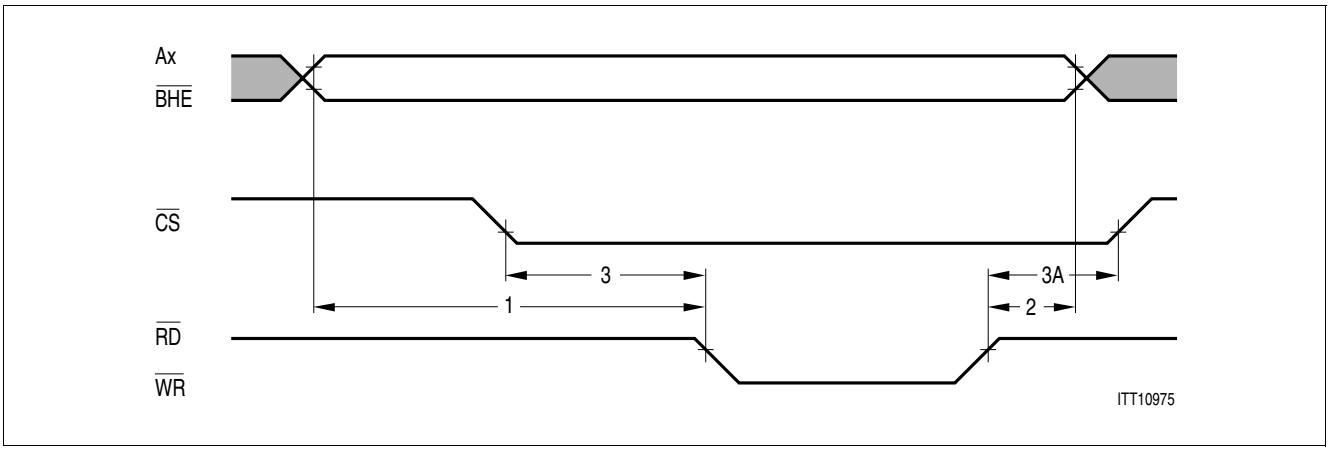


Figure 43 Intel Non-Multiplexed Address Timing

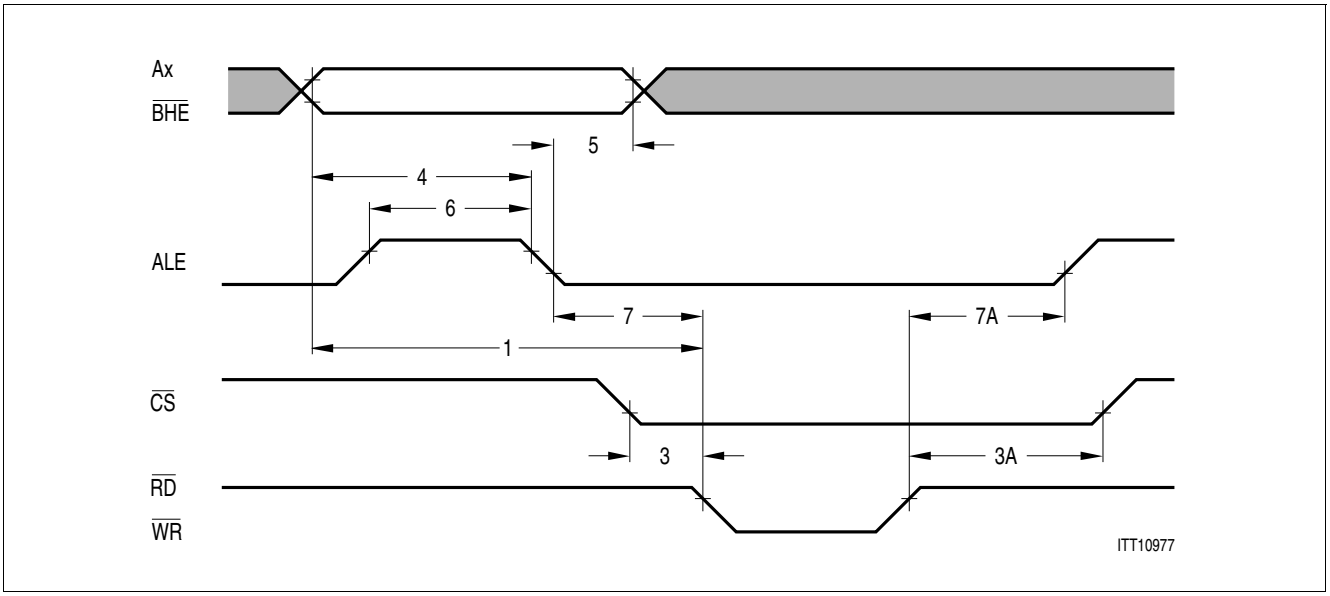


Figure 44 Intel Multiplexed Address Timing

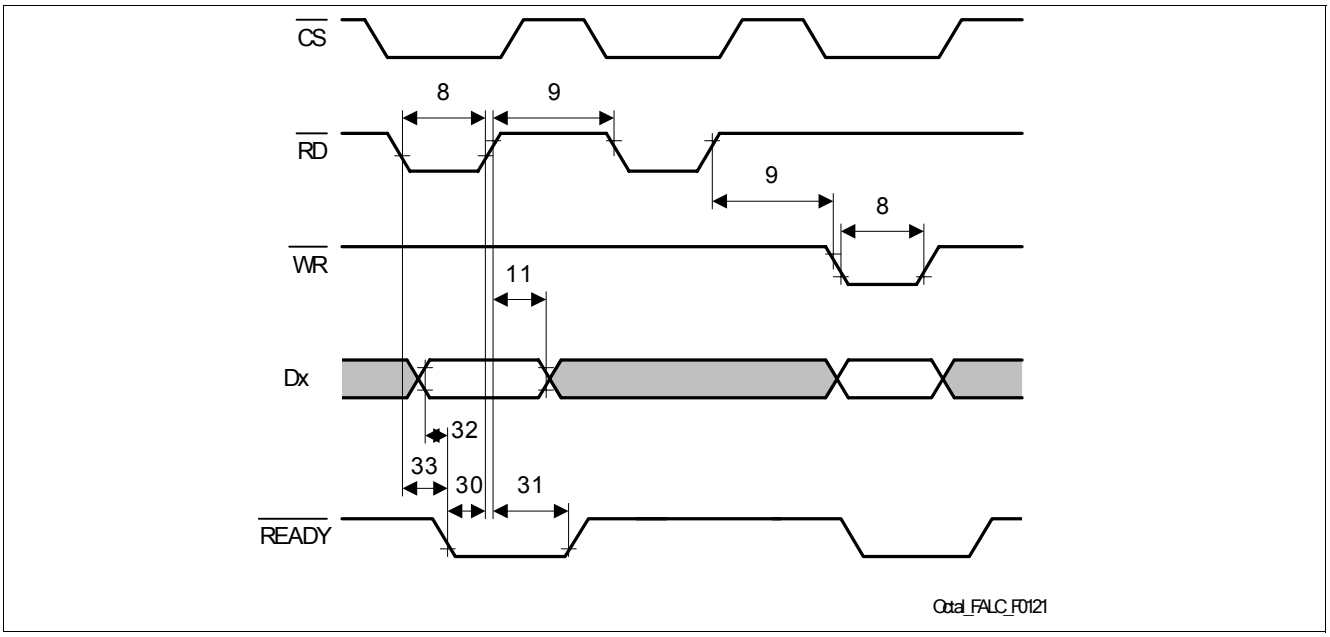


Figure 45 Intel Read Cycle Timing

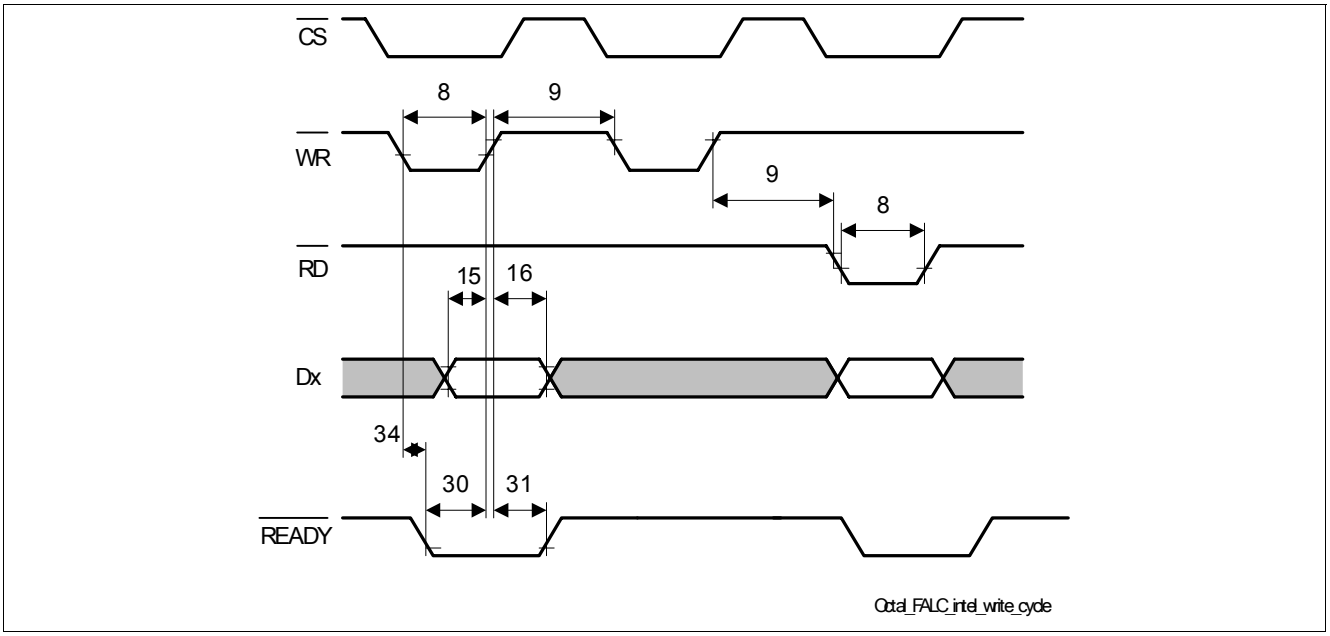


Figure 46 Intel Write Cycle Timing

Table 54 Intel Bus Interface Timing Parameter Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Address, $\overline{BHE}$ setup time	1	5	–	–	ns	–
Address, $\overline{BHE}$ hold time	2	0	–	–	ns	–
$\overline{CS}$ setup time	3	0	–	–	ns	–
$\overline{CS}$ hold time	3A	0	–	–	ns	–
Address, $\overline{BHE}$ stable before ALE inactive	4	10	–	–	ns	–
Address, $\overline{BHE}$ hold after ALE inactive	5	10	–	–	ns	–
ALE pulse width	6	30	–	–	ns	–
ALE setup time before $\overline{RD}$ or $\overline{WR}$	7	0	–	–	ns	–
ALE hold time after $\overline{RD}$ or $\overline{WR}$	7A	30	–	–	ns	–
$\overline{RD}$, $\overline{WR}$ pulse width	8	80	–	–	ns	–
RD, WR control interval	9	70	–	–	ns	–
Data hold after $\overline{RD}$ inactive	11	10	–	30	ns	–
Data stable before $\overline{WR}$ inactive	15	30	–	–	ns	–
Data hold after $\overline{WR}$ inactive	16	10	–	–	ns	–
$\overline{RD}$ or $\overline{WR}$ delay after $\overline{READY}$	30	–	–	40	ns	–
$\overline{READY}$ hold time after $\overline{RD}$ or $\overline{WR}$	31	5	–	–	ns	–
Data stable before $\overline{READY}$	32	–	–	90	ns	–
$\overline{RD}$ to $\overline{READY}$ delay	33	–	–	90	ns	–
$\overline{WR}$ to $\overline{READY}$ delay	34	–	–	90	ns	–

6.1.4.2 Motorola Bus Interface Mode

Figure 47 and **Figure 48** show the timing of the SCI Interface and **Table 55** the appropriate timing parameter values.

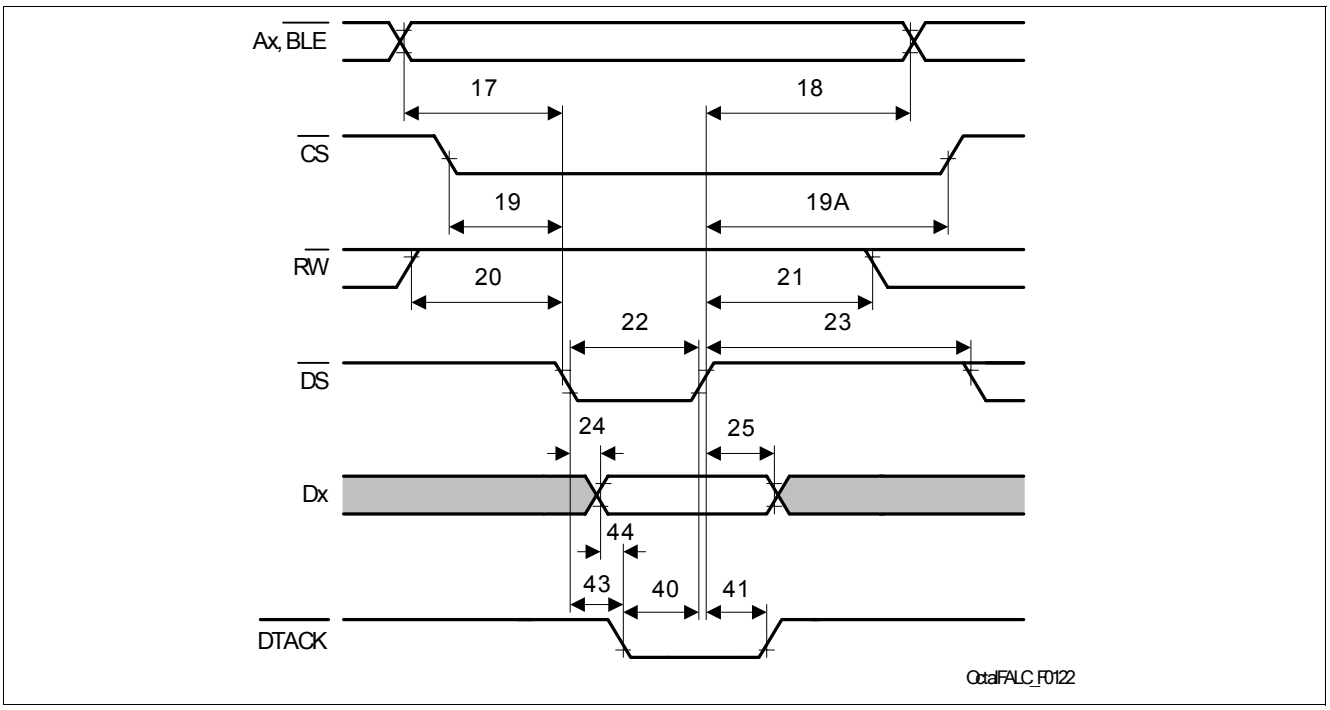


Figure 47 Motorola Read Cycle Timing

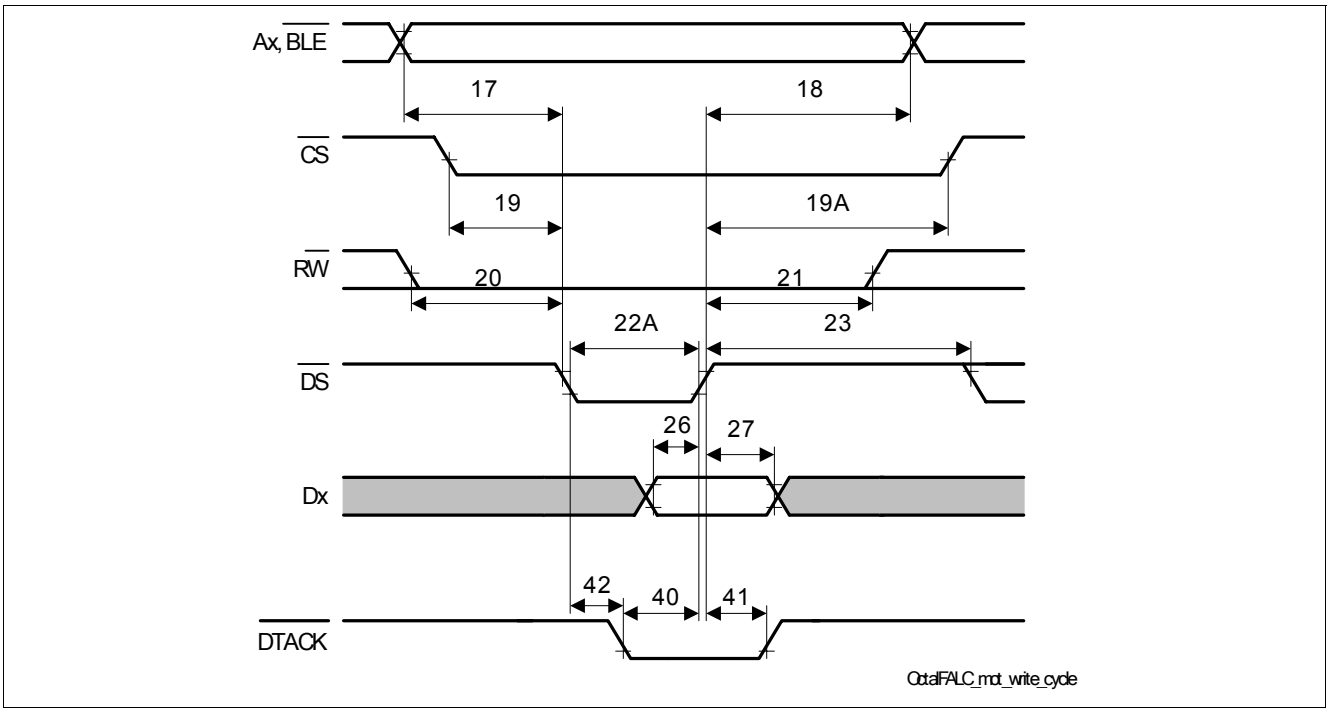


Figure 48 Motorola Write Cycle Timing

Table 55 Motorola Bus Interface Timing Parameter Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Address, $\overline{BLE}$ setup time before $\overline{DS}$ active	17	15	–	–	ns	–
Address, $\overline{BLE}$ hold after $\overline{DS}$ inactive	18	0	–	–	ns	–
$\overline{CS}$ active before $\overline{DS}$ active	19	0	–	–	ns	–
$\overline{CS}$ hold after $\overline{DS}$ inactive	19A	0	–	–	ns	–
$\overline{RW}$ stable before $\overline{DS}$ active	20	10	–	–	ns	–
$\overline{RW}$ hold after $\overline{DS}$ inactive	21	0	–	–	ns	–
$\overline{DS}$ pulse width (read access)	22	80	–	–	ns	–
$\overline{DS}$ pulse width (write access)	22A	80	–	–	ns	–
$\overline{DS}$ control interval	23	70	–	–	ns	–
Data valid after $\overline{DS}$ active (read access)	24	–	–	75	ns	–
Data hold after $\overline{DS}$ inactive (read access)	25	–	–	30	ns	–
Data stable before $\overline{DS}$ active (write access)	26	30	–	–	ns	–
Data hold after $\overline{DS}$ inactive (write access)	27	10	–	–	ns	–
$\overline{DS}$ delay after $\overline{DTACK}$	40	–	–	25	ns	–
$\overline{DTACK}$ hold time after DS inactive	41	10	–	–	ns	–
$\overline{DS}$ to $\overline{DTACK}$ delay for write	42	–	–	100	ns	–
$\overline{DS}$ to $\overline{DTACK}$ delay for read	43	–	–	100	ns	–
Data strobe before $\overline{DTACK}$	44	0	–	–	ns	–

6.1.4.3 SCI Interface

Figure 49 shows the timing of the SCI Interface and **Table 56** the appropriate timing parameter values.

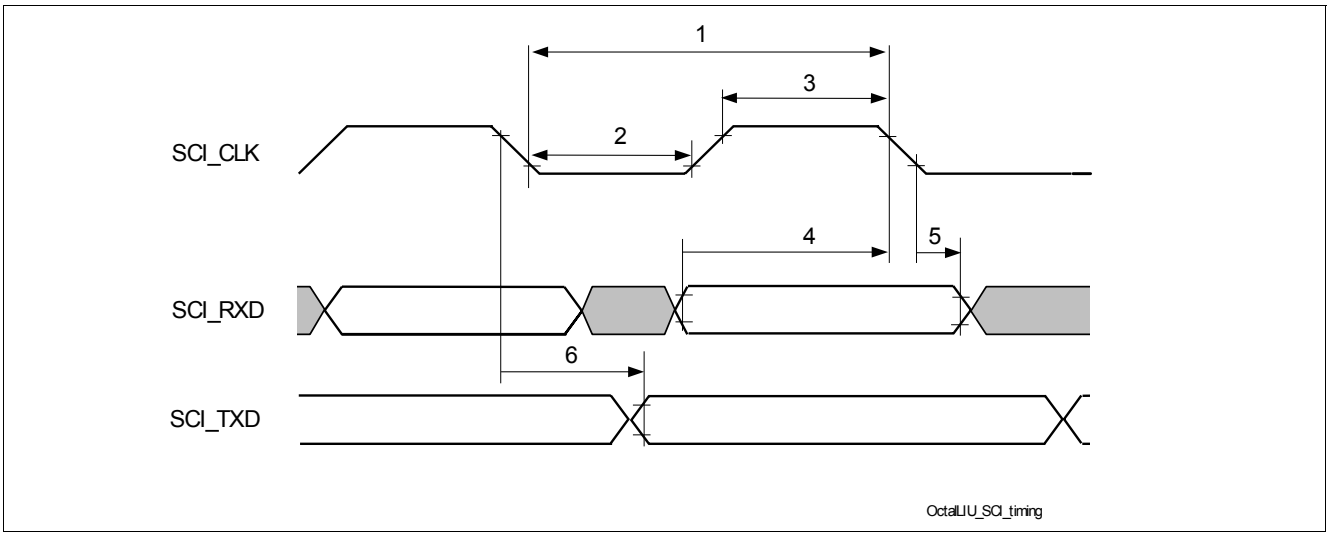


Figure 49 SCI Interface Timing

Table 56 SCI Timing Parameter Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCI_CLK cycle time in full duplex mode	1	170	–	–	ns	–
SCI_CLK cycle time in half duplex mode	1	500	–	–	ns	–
SCI_CLK clock low time	2	76.5	–	–	ns	–
SCI_CLK clock high time	3	76.5	–	–	ns	–
SCI_RXD setup time before SCI_CLK	4	0	–	–	ns	–
SCI_RXD hold time after SCI_CLK	5	0	–	–	ns	–
SCI_TXD delay time after SCI_CLK	6	–	–	30	ns	–

6.1.4.4 SPI Interface

Figure 50 shows the timing of the SCI Interface and **Table 57** the appropriate timing parameter values.

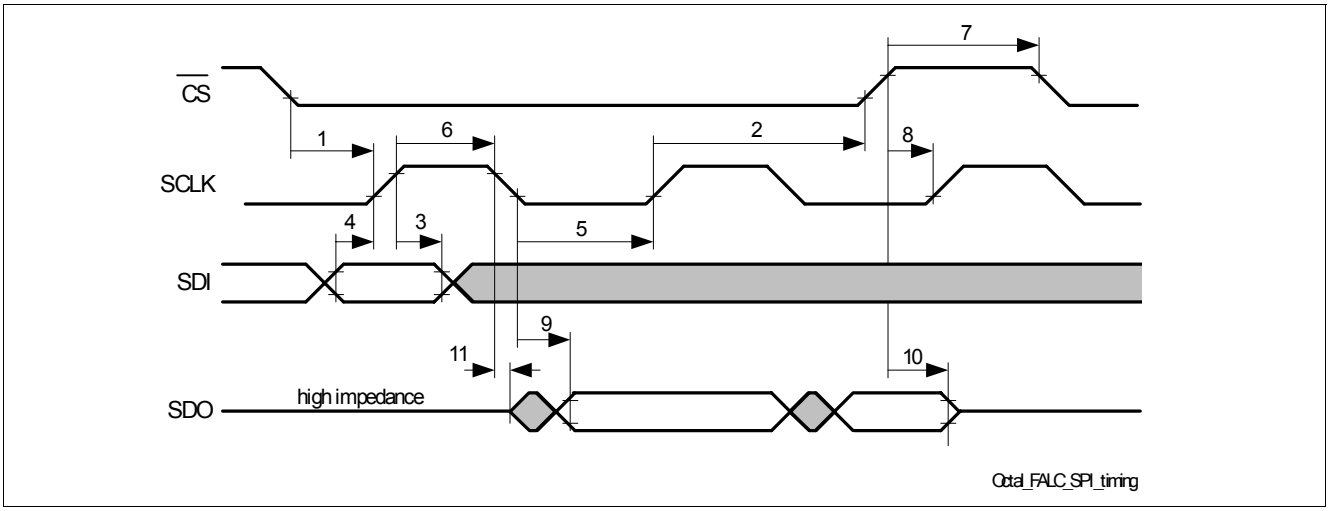


Figure 50 SPI Interface Timing

Table 57 SPI Timing Parameter Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK frequency	–	–	–	100	MHz	–
$\overline{CS}$ setup time before SCLK	1	40	–	–	ns	–
$\overline{CS}$ hold time after SCLK	2	40	–	–	ns	–
SDI hold time after SCLK	3	40	–	–	ns	–
SDI setup time before SCLK	4	40	–	–	ns	–
SCLK low time	5	45	–	–	ns	–
SCLK high time	6	45	–	–	ns	–
$\overline{CS}$ high time	7	100	–	–	ns	–
Clock disable time before SCLK	8	50	–	–	ns	–
SDO output stable after SCLK	9	–	–	40	ns	–
SDO output hold after $\overline{CS}$ disable	10	–	–	40	ns	–
SDO output high impedance after SCLK	11	0	–	–	ns	–

6.1.5 Digital Interface (Framer Interface)

Figure 51, Figure 52, Figure 53 and Figure 54 show the timing and Table 59, Table 60, Table 61 the appropriate timing parameter values at the digital interface of the OctalLIUTM.

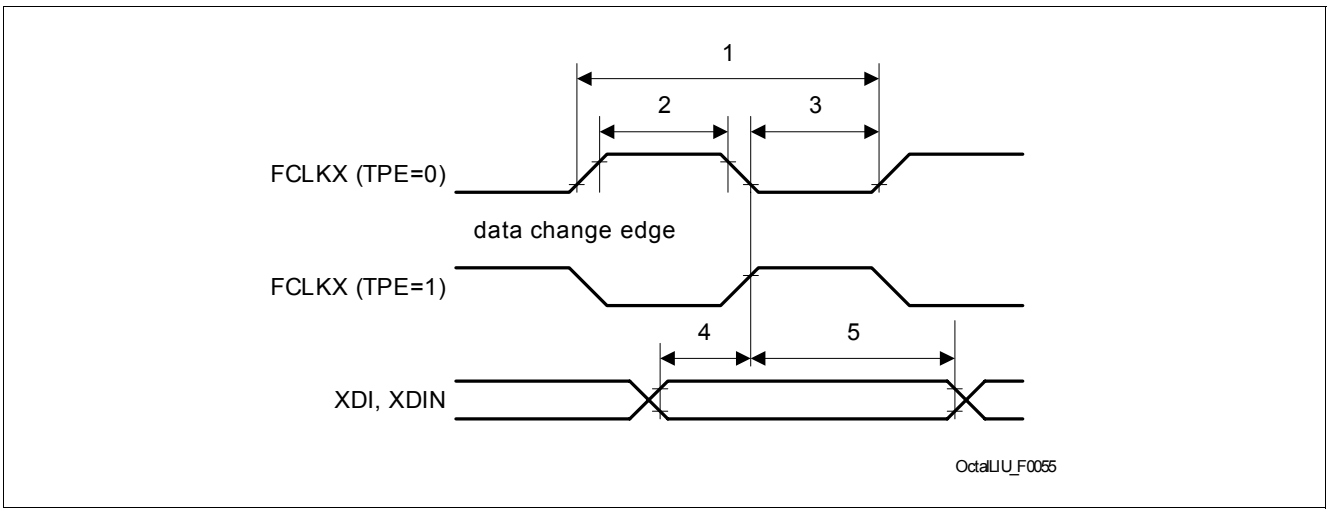


Figure 51 FCLKX Output Timing

Table 58 FCLKX Timing Parameter Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLKX clock period E1	1	–	488	–	ns	–
FCLKX clock period T1/J1	1	–	648	–	ns	–
FCLKX high	2	40	–	–	%	–
FCLKX low	3	40	–	–	%	–
XDI, XDIN setup time	4	5	–	–	ns	–
XDI, XDIN hold time	5	15	–	–	ns	–

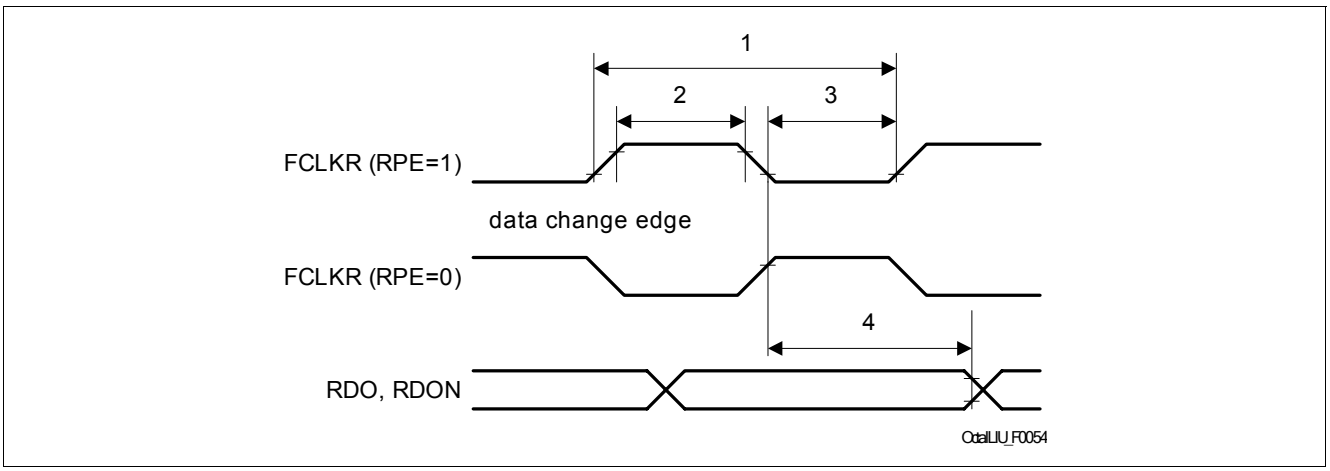


Figure 52 FCLKR Output Timing

Table 59 FCLKR Timing Parameter Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLKR clock period E1	1	–	488	–	ns	–
FCLKR clock period T1/J1	1	–	648	–	ns	–
FCLKR high	2	40	–	–	%	–
FCLKR low	3	40	–	–	%	–
RDO, RDON delay	4	0	–	35	ns	–

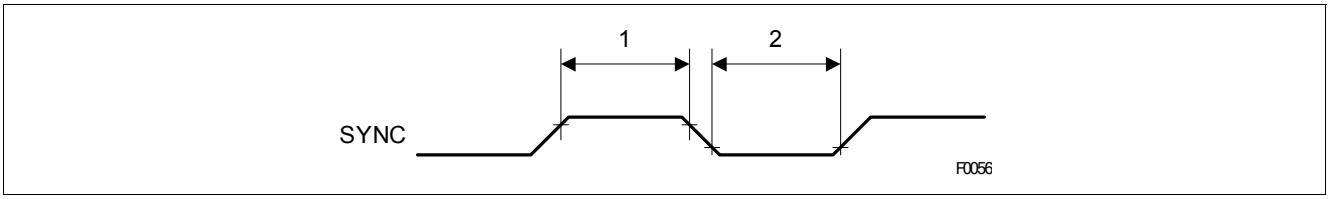


Figure 53 SYNC Timing

Table 60 SYNC Timing Parameter Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SYNC high time	1	125	–	–	ns	–
SYNC low time	2	122	–	–	ns	–

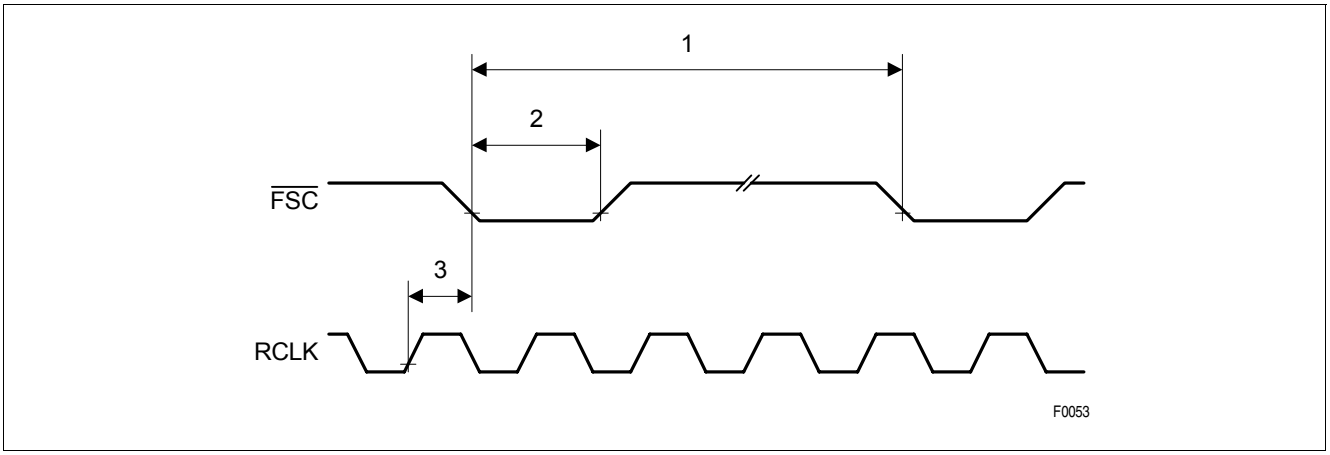


Figure 54 FSC Timing

Table 61 FSC Timing Parameter Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FSC period	1	–	125	–	µs	–
FSC low time E1	2	–	244	–	ns	–
FSC low time T1/J1	2	–	324	–	ns	–
RCLK to FSC delay	3	–	50	80	ns	–

6.1.6 Pulse Templates - Transmitter

The transmitter includes a programmable pulse shaper to generate transmit pulse masks according to:

- For T1: FCC68; ANSI T1. 403 1999, figure 4; ITU-T G703 11/2001, figure 10 (for different cable lengths), see **Figure 56**. For measurement configuration were R_{load} = 100 Ω see **Figure 33**.
- For E1: ITU-T G703 11/2001, figure 15 (for 0 m cable length), see **Figure 55**; ITU-T G703 11/2001, figure 20 (for DCIM mode). For measurement configuration were R_{load} = 120 Ω or R_{load} = 75 Ω see **Figure 32**.

The transmit pulse form is programmed either

- By the registers XMP(2:0) compatible to the QuadLIU®, see **Table 24** and **Table 25**, if the register bit XPM2.XPDIS is cleared
- Or by the registers TXP(16:1), if the register bit XPM2.XPDIS is set, see **Table 26** and **Table 27**.

6.1.6.1 Pulse Template E1

With the given values in **Table 25** or **Table 27**, for transformer ratio: 1 : 2.4, cable type AWG24 and with R_{load} = 120 Ω the pulse mask according to ITU-T G703 11/2001, see **Figure 55**, is fulfilled.

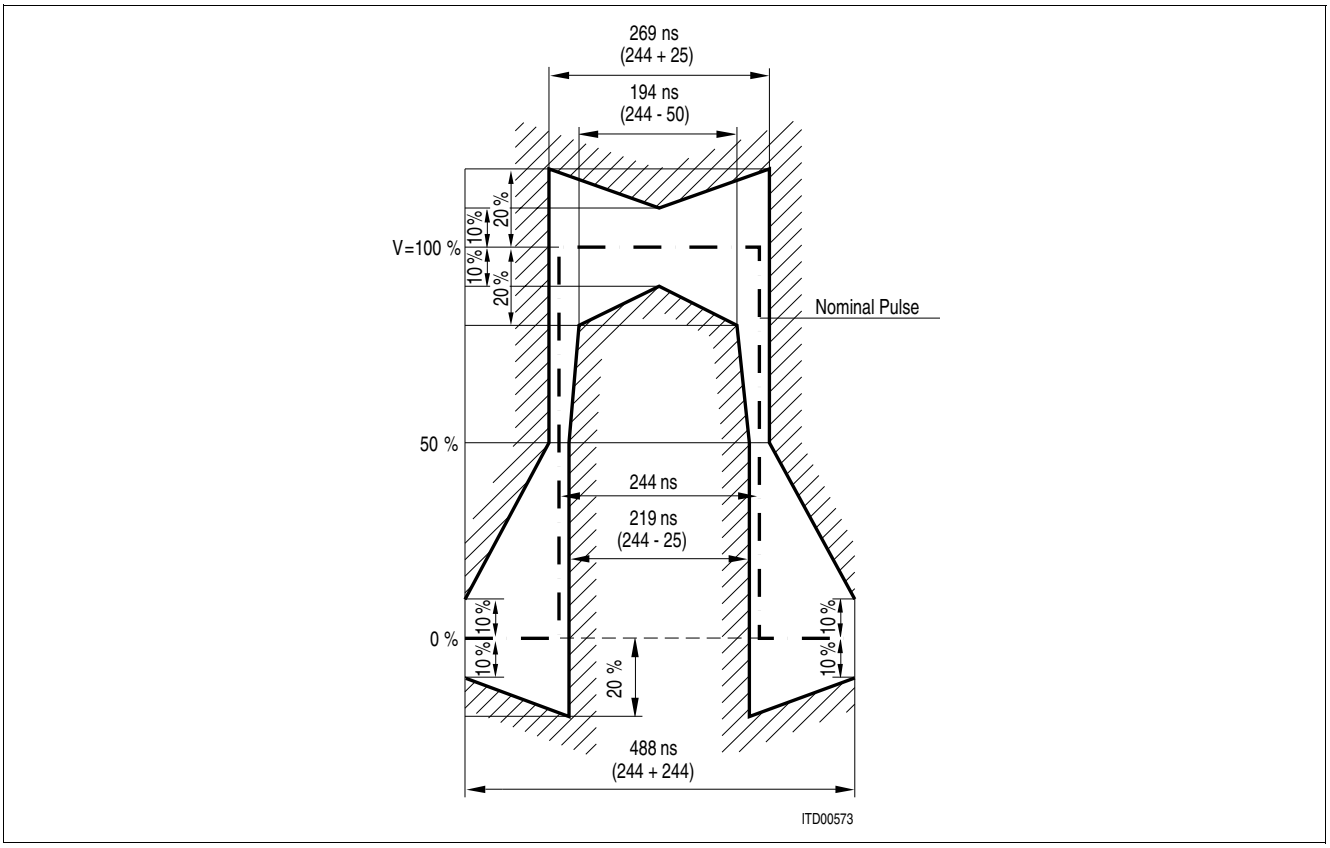


Figure 55 E1 Pulse Shape at Transmitter Output

6.1.6.2 Pulse Template T1

With the given values in **Table 24** or **Table 26**, for transformer ratio: 1 : 2.4, cable type AWG24 and with R_{load} = 100 Ω the pulse mask according to ITU-T G703 11/2001, figure 10, see **Figure 56**, is fulfilled.

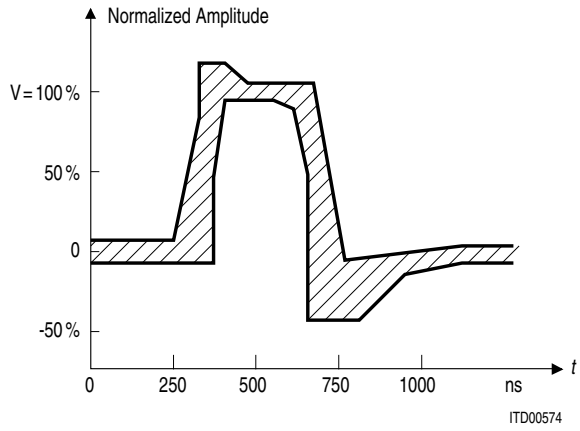


Figure 56 T1 Pulse Shape at the Cross Connect Point

Table 62 T1 Pulse Template at Cross Connect Point (T1.102 [1])

Maximum Curve		Minimum Curve	
Time [ns]	**Level [%][2]**	**Time [ns]**	**Level [%]**
0	5	0	-5
250	5	350	-5
325	80	350	50
325	115	400	95
425	115	500	95
500	105	600	90
675	105	650	50
725	-7	650	-45
1100	5	800	-45
1250	5	925	-20
		1100	-5
		1250	-5

1) Requirements of ITU-T G.703 are also fulfilled

2) 100 % value must be in the range of 2.4 V and 3.6 V; tested at 0 and 200 m using PIC 22AWG cable characteristics.

6.2 Capacitances

Values of capacitances of the input and of the output pins of the OctalLIUTM are listed in **Table 63**.

Table 63 Capacitances

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{IN}	5	–	10	pF	–
Output capacitance [1]	C_{OUT}	8	–	15	pF	All except XLx
Output capacitance [1]	C_{OUT}	8	–	20	pF	XLx

1) Not tested in production

6.3 Package Characteristics

The following table shows the thermal characteristics of the BGA package together with different PCBs.

Table 64 Package Characteristic Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal Resistance between junction and PCB for BGA 256 package [1]	R_{thjab}	–	29	–	K/W	Single layer PCB, natural convection
		–	23.7	–	K/W	4 layer PCB, natural convection
		–	22.4	–	K/W	6 layer PCB, natural convection
		–	22.3	–	K/W	10 layer PCB, natural convection
Junction Temperature	R_j	–		125	°C	–

6.4 Test Configuration

6.4.1 AC Tests

The values for AC characteristics of the chapters above are based on the following definitions of levels and load capacitances:

Table 65 AC Test Conditions

Parameter	Symbol	Values	Unit	Note / Test Condition
Load Capacitance	C_L	50	pF	–
Input Voltage high	V_{IH}	2.4	V	All except RLx
Input Voltage low	V_{IL}	0.4	V	All except RLx
Test Voltage high	V_{TH}	2.0	V	All except XLx
Test Voltage low	V_{TL}	0.8	V	All except XLx

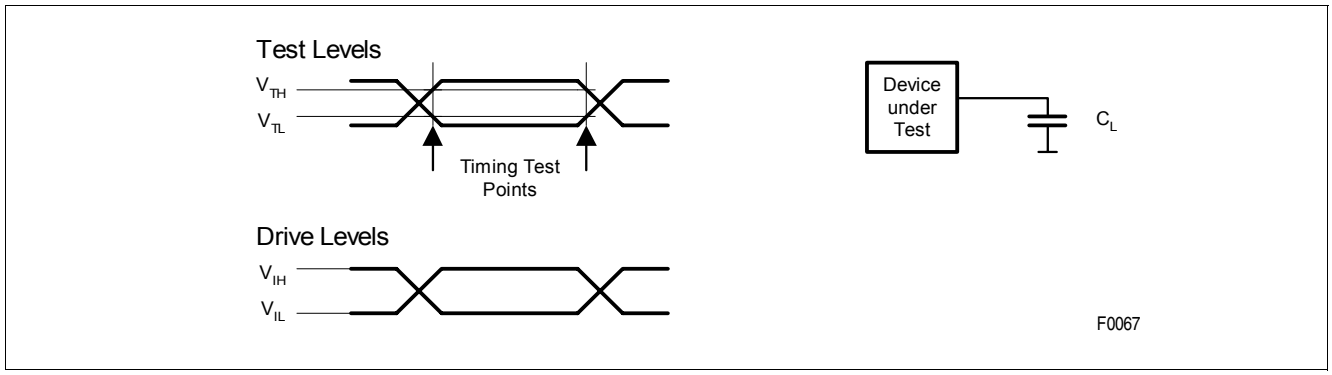


Figure 57 Input/Output Waveforms for AC Testing

6.4.2 Power Supply Test

For power supply test all eight channels of the OctalLIUTM are active. Transmitter and receiver are configured as for typical applications. The transmitted data are looped back to the receiver by a short line as shown in **Figure 58**. On the system side the interfaces of all channels work independent from another (no multiplex mode is configured).

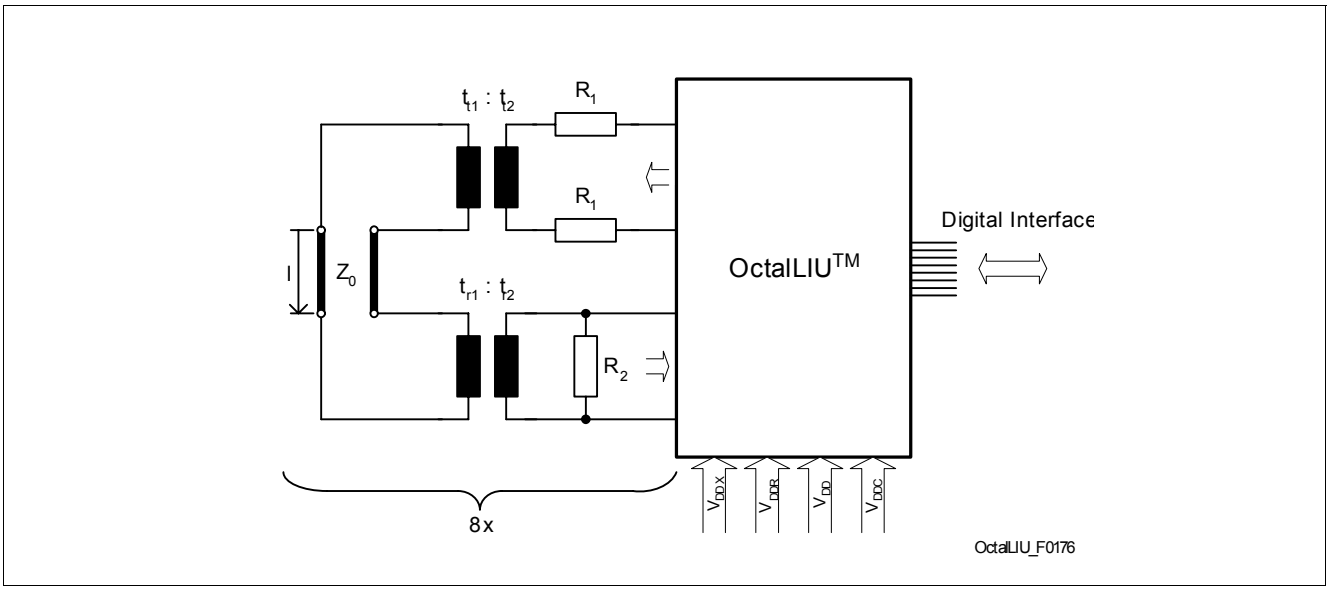


Figure 58 Device Configuration for Power Supply Testing

Table 66 Power Supply Test Conditions E1

Parameter	Symbol	Values	Unit	Note / Test Condition
Load Resistance at transmitter	R_1	7.5	Ω	1%; XL3 and XL4 are left open; PC6.TSRE = ´1´
Termination Resistance at receiver	R_2	120	Ω	1%; integrated receive line resistor R_{TERM} is switched off (LIM0.RTRS =´0´)
Line Impedance	R_L	120	Ω	–
Line Length	l	< 0.2	m	–
Transformer Ratio Transmit	tt1 : tt2	2.4 : 1		–
Transformer Ratio Receive	tr1 : tr2	1 : 1		–
Framer interface Frequency	XCLK RCLK	2.048	MHz	–
Test SignalActive Channels (DCOs active, 2-frame buffer)4	–	2^{15}-1	–	PRBS pattern
Pulse Mask Programming (compatible to QuadLIU®)	XPM2	40_H	–	Pulse mask according to ITU-T G703 11/2001, see **Figure 55**
	XPM1	03_H	–	
	XPM0	$7B_H$	–	
Ambient Temperature	–	85	°C	–

Table 67 Power Supply Test Conditions T1/J1

Parameter	Symbol	Values	Unit	Note / Test Condition
Load Resistance	R_1	2	Ω	1%; XL3 and XL4 are left open; PC6.TSRE = ´1´
Termination Resistance	R_2	100	Ω	1%; integrated receive line resistor R_{TERM} is switched off (LIM0.RTRS =´0´)
Line Impedance	R_L	100	Ω	–
Line Length	l	< 0.2	m	–
Transformer Ratio Transmit	tt1 : tt2	2.4 : 1	–	–
Transformer Ratio Receive	tr1 : tr2	1 : 1	–	–
Framer interface Frequency	XCLK RCLK	1.544	MHz	–
Test SignalActive Channels (DCOs active, 2-frame buffer)4	–	2^{15}-1	–	PRBS pattern
Pulse Mask Programming (compatible to QuadLIU®)	XPM2	02_H	–	Pulse mask according to ITU-T G703 11/2001, figure 10, see **Figure 56**
	XPM1	27_H	–	
	XPM0	$9F_H$	–	
Ambient Temperature	–	85	°C	–

7 Operational Description

7.1 Operational Overview

Every of the eight channels of the OctalLIU™ can be operated in two clock modes, which are either E1 mode or T1/J1 mode, selected by the register bit GCM2.VFREQ_EN, see **Chapter 3.5.5**:

- In the so called “flexible master clocking mode” (GCM2.VFREQ_EN = ´1´) all eight ports can work in E1 or in T1 mode individually, independent from another.
- In the so called “clocking fixed mode” (GCM2.VFREQ_EN = ´0´) all eight ports must work together either in E1 or in T1 mode.

The device is programmable via one of the three integrated micro controller interfaces which are selected by strapping of the pins IM(1:0):

- The asynchronous interface has two modes: Intel (IM(1:0) = ´00_b´) and Motorola (IM(1:0) = ´01_b´). This interface enables byte or word access to all control and status registers, see **Chapter 3.5.1**.
- SPI interface (IM(1:0) = ´10_b´), see **Chapter 3.5.2.2**.
- SCI interface (IM(1:0) = ´11_b´), see **Chapter 3.5.2.1**.

The OctalLIU™ has three different kinds of registers:

- The control registers configure the whole device and have write and read access.
- The status registers are read-only and are updated continuously. Normally, the processor reads the status registers periodically to analyze the alarm status and signaling data.
- The interrupt status registers are read-only and are cleared by reading (“rsc”). They are updated (set) continuously. Normally, the processor reads the interrupt status registers after an interrupt occurs at pin INT. Masking can be done with the appropriate interrupt mask registers. Mask registers are control registers.

All this registers can be separate into two groups:

- Global registers are not belonging especially to one of the eight channels. The higher address byte is ´00_H´.
- The other registers are belonging to one of the eight channels. The higher address bytes - marked as ´xx_H´ in the register description - are identical to the numbers 0 up to 7 of the appropriate channels. So every of this registers exist eight time in the whole device.

7.2 Device Reset

After the device is powered up, the OctalLIU™ must be forced to the reset state first.

The OctalLIU™ is forced to the reset state if a low signal is input on pin $\overline{\text{RES}}$ for a minimum period of 10 µs, see **Figure 42**. During reset the OctalLIU™

- Needs an active clock on pin MCLK
- The pin COMP must be ´0´.
- The pins IM(1:0) must have defined values to select the micro controller interface.
- Only if IM(1:0) = ´11_b´ (SCI interface is selected) the pins A(5:0) must have defined values to select the SCI source address of the device.
- Only if IM1 = ´1´ (SCI or SPI interface is selected) the pins D(15:5) must have defined values to configure the central PLL in the master clocking unit of the device.

During and after reset all internal flip-flops are reset and most of the control registers are initialized with default values.

SIgnals (for example RL1/2 receive line) should not be applied before the device is powered up.

After reset the complete device is initialized, especially to E1 operation and “flexible master clocking mode”. The complete initialization is listed in **Table 68**. Additionally all interrupt mask registers IMR1, IMR3, IMR4, IMR6 and IMR7 are initialized to ´FF_H´, so that not masking is performed.

After reset the OctalLIU™ must be configured first. General guidelines for configuration are described in **Chapter 7.4** for E1 mode and **Chapter 7.5** for T1/J1 mode.

For reset see also **Chapter 3.5.5.1**.

7.3 Device Initialization

After reset, the OctalLIU™ is initialized for E1 with register values listed in the following table.

Table 68 Initial Values after Reset

Register	Reset Value	Meaning
LIM0, LIM1, PCD, PCR	´00_H´, ´00_H´, ´00_H´, ´00_H´	Slave Mode, local loop off Analog interface selected; remote loop off; Pulse count for LOS detection cleared; Pulse count for LOS recovery cleared
XPM(2:0)	´40_H´, ´03_H´, ´$7B_H$´	E1 Transmit pulse template for 0 m but with unreduced amplitude (note that transmitter is in tristate mode)
IMR(7:0)	´FF_H´	All interrupts are disabled
GCR	´00_H´	Internal second timer, power on
CMR1	´00_H´	RCLK output: DPLL clock, DCO-X enabled, DCO-X internal reference clock
CMR2	´00_H´	RCLK selected, XCLK selected
PC(3:1)	´00_H´, ´$F0_H$´ ´00_H´, ´00_H´	Functions of ports RP(A to B) are reserved, function of port RPC is RCLK output (but is only pulled up, because PC5.CRP = ´0´ after reset), functions of ports XP(A to B) are reserved.
PC5	´00_H´	FCLKR, FCLKX, RCLK configured to inputs,
GCM(6:1)	GCM2 = ´10_H´, others ´00_H´	“Flexible master clocking mode” selected
GPC(5:3)	´65_H´, ´43_H´, ´21_H´	Source for RCLK1 up to RCLK7 are the appropriate channels (only valid for COMP = ´0´)
GPC6	´07_H´	QuadLIU compatible system interface multiplexed modes are selected, source for RCLK8 is channel 8 (both only valid for COMP = ´0´)
CMR(6:4)	´00_H´	Recovered line clock drives RCLK
GPC2	´00_H´	Source for SEC and RCLK1 is channel 1
TXP(16:1)	TXP(1:8) = ´38_H´ TXP(9:16) = ´00_H´	This registers are not used after reset because XPM2.XPDIS = ´0´
INBLDTR	´00_H´	Minimum In-band loop detection time
ALS	´00_H´	No automatic loop switching is performed
PRBSTS(4:1)	all ´00_H´	No time slots are selected for PRBS pattern

7.4 Device Configuration in E1 Mode

E1 Configuration

For a correct start up of the primary access interface a set of parameters specific to the system and hardware environment must be programmed after reset goes inactive. Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T and ETSI recommendations (e.g. fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 69** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, can be programmed simultaneously. The bit MR1.PMOD should always be kept low (otherwise T1/J1 mode is selected).

Table 69 Configuration Parameters (E1)

Basic Set Up	
Master clocking mode	GCM(6:1) according to external MCLK clock frequency
E1 mode select	MR1.PMOD = ´0´
Clock system configuration	CMR(3:1), GPC1; if COMP = ´0´ CMR(6:4) and GPC(6:2)
Specification of line interface	LIM0, LIM1, XPM(2:0)
Specification of transmit pulse mask	XPM(2:0) or TXP(16:1)
Line interface coding	MR0.XC(1:0), MR0.RC(1:0)
Loss-of-signal detection/recovery conditions	PCD, PCR, LIM1, LIM2
Multi Function Port selection	PC(3:1)

Features like alarm simulation etc. are activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

Note: Read access to unused register addresses: value should be ignored. Write access to unused register addresses: should be avoided, or set to "00" hex. All control registers (except XS(16:1), CMDR, DEC) are of type Read/Write.

Specific E1 Register Settings

The following is a suggestion for a basic configuration to meet most of the E1 requirements. Depending on different applications and requirement any other configuration can be used.

Table 70 Line Interface Configuration (E1)

MR2.DAIS = ´1´	Disables AIS insertion into the data stream (necessary for proper operation)
MR2.RTM = ´1´	Sets the receive dual elastic store in a "free running" mode (necessary for proper operation)
MR5.TT0 = ´1´	Enables transmit transparent mode (necessary for proper operation)
MR5.XTM = ´1´	Sets the transmitter in a "free running" mode (necessary for proper operation)
MR0.XC0/ MR0.RC0/ LIM1.DRS MR3.CMI	The OctalLIU™ supports requirements for the analog line interface as well as the digital line interface. For the analog line interface the codes AMI and HDB3 are supported. For the digital line interface modes (dual- or single-rail) the OctalLIU™ supports AMI, HDB3, CMI (with and without HDB3 precoding).
PCD = ´$0A_H$´	LOS detection after 176 consecutive "zeros" (fulfills G.775).
PCR = ´15_H´	LOS recovery after 22 "ones" in the PCD interval. (fulfills G.775).
LIM1.RIL(2:0) = ´02_H´	LOS threshold of 0.6 V (fulfills G.775).

Attention: After the device configuration a software reset should be executed by setting of bits CMDR.XRES/RRES.

7.5 Device Configuration in T1/J1 Mode

After reset, the OctalLIU™ is initialized for E1 doubleframe format. To configure T1/J1 mode, bit MR1.PMOD has to be set high. After the internal clocking is settled to T1/J1mode (takes up to 20 µs), the following register values are initialized:

T1/J1 Initialization

For a correct start up of the primary access interface a set of parameters specific to the system and hardware environment must be programmed after $\overline{\text{RES}}$ goes inactive (high). Both the basic and the operational parameters

must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T recommendations (e.g. fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. Table 71 gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, can be programmed simultaneously. The bit MR1.PMOD must always be kept high (otherwise E1 mode is selected). J1 mode is selected by additionally setting RC0.SJR = ´1´.

Features like channel loop-back, idle channel activation, clear channel activation, extensions for signaling support, alarm simulation, etc. are activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

Table 71 Configuration Parameters (T1/J1)

Basic Set Up	T1	J1
Master clocking mode	GCM(6:1) according to external MCLK clock frequency	
T1/J1 mode select	MR1.PMOD = ´1´,	MR1.PMOD = ´1´,
Clock system configuration	CMR(3:1), GPC1; if COMP = ´0´ CMR(6:4) and GPC(6:2)	
Specification of line interface	LIM0, LIM1,	
Specification of transmit pulse mask	XPM(2:0) or TXP(16:1)	
Line interface coding	MR0.XC(1:0), MR0.RC(1:0)	
Loss-of-signal detection/recovery conditions	PCD, PCR, LIM1, LIM2	
AIS to framer interface	MR2.XAIS	
Multi Function Port selection	PC(3:1)	

Note: Read access to unused register addresses: value should be ignored. Write access to unused register addresses: should be avoided, or set to ´00_H´. All control registers (except XS(12:1), CMDR, DEC) are of type read/write

Specific T1/J1 Configuration

The following is a suggestion for a basic configuration to meet most of the T1/J1 requirements. Depending on different applications and requirements any other configuration can be used.

Table 72 Line Interface Configuration (T1/J1)

Register	Function
MR2.DAIS = ´1´	Disables AIS insertion into the data stream (necessary for proper operation)
LOOP.RTM = ´1´	Sets the receive dual elastic store in a “free running” mode (necessary for proper operation)
MR4.TM = ´1´	Enables transparent mode (necessary for proper operation)
MR5.XTM = ´1´	Sets the transmitter in a “free running” mode (necessary for proper operation)
CCB(3:1) = ´FF_H‘	“Clear Channel” mode is selected (necessary for proper operation only if AMI code is selected)
MR0.XC0/1 MR0.RC0/1 LIM1.DRS CCB(3:1) DIC3.CMI	The OctalLIU™ supports requirements for the analog line interface as well as the digital line interface. For the analog line interface the codes AMI (with and without bit 7stuffing) and B8ZS are supported. For the digital line interface modes (dual- or single-rail) the OctalLIU™ supports AMI (with and without bit 7 stuffing), B8ZS (with and without B8ZS precoding).
PCD = ´$0A_H$´	LOS detection after 176 consecutive “zeros” (fulfills G.775/Telcordia (Bellcore)/AT&T)

Table 72 Line Interface Configuration (T1/J1)

Register	Function
PCR = ´15$_H$´	LOS recovery after 22 “ones” in the PCD interval (fulfills G.775, Bellcore/AT&T).
LIM1.RIL(2:0) = ´02$_H$´	LOS threshold of 0.6 V (fulfills G.775).
GCR.SCI = ´1´	Additional Recovery Interrupts. Help to meet alarm activation and deactivation conditions in time.
LIM2.LOS1 = ´1´	Automatic pulse-density check on 15 consecutive zeros for LOS recovery condition (Bellcore requirement)

Note: After the device configuration a software reset should be executed by setting of bits CMDR.XRES/RRES.

7.6 Device Configuration for Digital Clock Interface Mode (DCIM)

The following table shows the necessary configuration for the Digital Clock Interface Mode (DCIM), see ITU-T G.703 11/2001, chapter 13. The receive clock at RL1/RL2 (2.048 MHz) is supported at multi function port RPC. The transmit clock at FCLKX (2.048 MHz) is transmitted at XL1/XL2.

DCIM mode is standardized only for 2.048 MHz (E1 mode, MR1.PMOD = ´0´). The OctalLIU™ can handle also 1.544 MHz if MR1.PMOD = ´1´.

Table 73 Device Configuration for DCIM Mode

MR1.PMOD	Selects 2.048 MHz or 1.544 MHz, see text above
LIM0.DCIM = ´1´	Selects DCIM mode.
LIM1.RL = ´0´	TX clock mode.
CMR1.DXSS = ´0´	
CMR1.DXJA = ´0´	
LIM1.DRS = ´0´ MR0.RC(1:0) = ´10_b´	Line interface mode RX
MR0.XC(1:0) = ´10_b´	Line interface mode TX
PC1.RPC1(3:0) = ´1111_b´	Select RCLK as output
PC5.CRP = ´1´	
CMR1.DRSS(1:0) or CMR5.DRSS(2:0) : select the appropriate channel	RX clock mode
CMR1.DCS = ´1´	
LIM0.MAS = ´0´	
CMR1.RS(1:0) = ´10_b´ or CMR4.RS(2:0) = ´010_b´	
GCM(1:8) see **Chapter 3.5.5** and **GCM6**	Configure clock system
LIM2.SCF, CMR6.SCFX, CMR2.ECFAX, CMR2.ECFAR, CMR3:CFAX(3:0), CMR3.CFAR(3:0), CMR4.IAR(4:0), CMR5.IAX(4:0): see **Chapter 3.7.9** and **Table 18**	Configure DCO-X and DCO-R
DIC1.RBS(1:0) = ´10_b´	Configure elastic buffers
DIC1.XBS(1:0) = ´11_b´	

8 Appendix

8.1 Protection Circuitry

The design in **Figure 59** shows an example of how to build up a generic E1/T1/J1 platform. The circuit shown has been successfully checked against ITU-T K.20 and K.21 lightning surge tests (basic level).

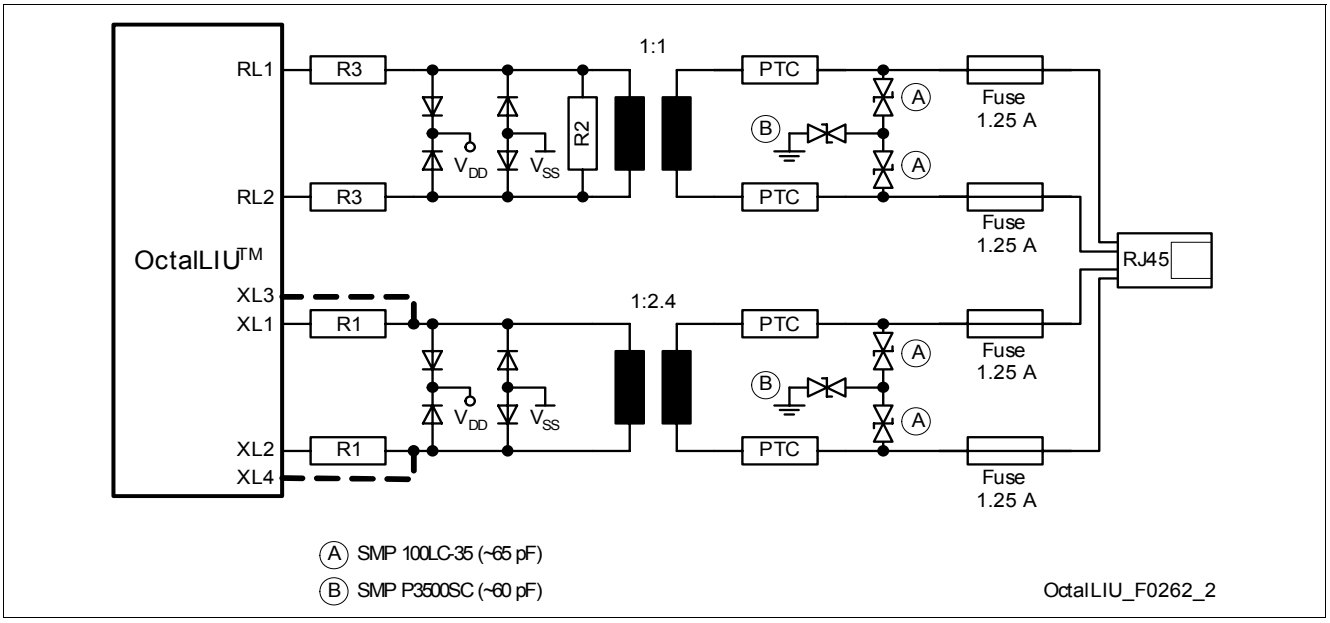


Figure 59 Protection Circuitry Examples (shown for one channel)

8.2 Application Notes

Several application notes and technical documentation provide additional information. Online access to supporting information is available on the internet page:

http://www.infineon.com/octalliu

On the same page you find as well the

- Boundary Scan File for OctalLIU™ Version 1.1 (BSDL File)

8.3 Software Support

The following software package is provided together with the OctalLIU™ Reference System EASY 2256:

- E1 and T1 driver functions supporting different ETSI, AT&T and Telcordia (former: Bellcore) requirements
- IBIS model for OctalLIU™ Version 1.1 (according to ANSI/EIA-656)
- “Flexible Master Clock Calculator”, which calculates the required settings for the registers GCM(1:8) depending on the external master clock frequency (MCLK)
- “External Line Front End Calculator”, which provides an easy method to optimize the external components depending on the selected application type.r

The both calculators run under a Win9x/NT environment. Calculation results are traced an can be stored in a file or printed out for documentation.

Screen shots of both programs are shown in **Figure 60** and **Figure 61** below.

Figure 60 Screen Shot of the “Master Clock Frequency Calculator”

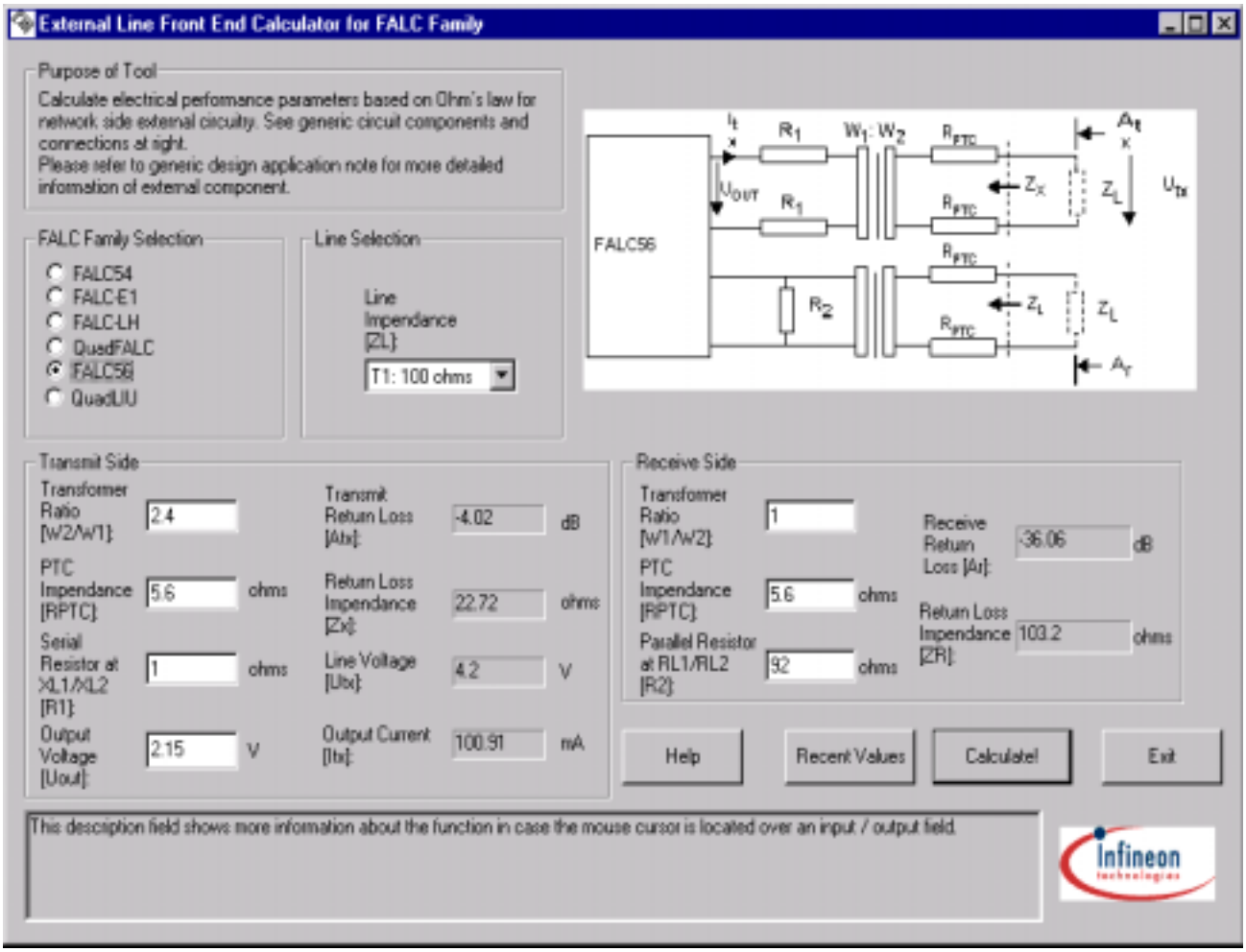


Figure 61 Screen Shot of the "External Line Frontend Calculator"

Terminology

A	
A/D	Analog to digital
ADC	Analog to Digital Converter
AIS	Alarm Indication Signal (blue alarm)
AGC	Automatic Gain Control
ALOS	Analog Loss Of Signal
AMI	Alternate Mark Inversion
ANSI	American National Standards Institute
ATM	Asynchronous Transfer Mode
AUXP	AUXiliary Pattern
B	
B8ZS	Binary 8 Zero Supression (Line coding to avoid too long strings of consecutive "0")
Bellcore	Bell Communications Research
BPV	BiPolar Violation
BSN	Backward Sequence Number
C	
CDR	Clock and Data Recovery
CIS	Channel Interrupt Status
CMI	Coded Mark Inversion code (also known as 1T2B code)
D	
D/A	Digital to Analog
DAC	Digital to Analog Converter
DCIM	Digital Clock Interface Mode
DCO	Digitally Controlled Oscillator
DCO-R	DCO of receiver
DCO-X	DCO of transmitter
DL	Digital Loop
DPLL	Digitally controlled Phase Locked Loop
DS1	Digital Signal level 1
E	
ESD	ElectroStatic Discharge
EASY	Evaluation system for FALC and LIU products
EQ	EQualizer
ETSI	European Telecommunication Standards Institute
F	
FALC®	Framing And Line interface Component
FCC	US Federal Communication Commission
FCS	Frame Check Sequence (used in PPR)
G	

GIS	Global Interrupt Status
H	
HBM	Human body model for ESD classification
HDB3	High density bipolar of order 3
I	
IBIS	I/O buffer information specification (ANSI/EIA-656)
IBL	In Band Loop
ISDN	Integrated Services Digital Network
ITU	International Telecommunications Group
J	
JATT	Jitter ATTenuator
JTAG	Joined Test Action Group
L	
LBO	Line Build Out
LCV	Line Code Violation
LIU	Line Interface Unit
LL	Local Loop
LLB	Line Loop Back
LOS	Loss of Signal (red alarm)
LSB	Least Significant Bit
M	
MFP	Multi Function Port
MSB	Most Significant Bit
MUX	MUltipleXer
N	
NRZ	Non Return to Zero signal
P	
PCM	Pulse Code Modulation
PD	Pull Down resistor
PDV	Pulse Density Violation
PLB	Payload Loop Back
PLL	Phase Locked Loop
PMQFP	Plastic Metric Quad Flat Pack (device package)
PRBS	Pseudo Random Binary Sequence
PTQFP	Plastic Thin Metric Quad Flat Pack (device package)
PU	Pull Up resistor
R	
RAI	Remote Alarm Indication (yellow alarm)
RAM	Random Access Memory
RDI	Remote Defect Indication
RL	Remote Loop
RLM	Receive Line Monitoring
ROM	Read-Only Memory

RX	Receiver
S	
SAPI	Service Access Point Identifier (special octet in PPR)
SCI	Serial ControlInterface
SPI	Serial Peripheral Interface
Sidactor	Overvoltage protection device for transmission lines
T	
TAP	Test Access Port
TEI	Terminal Endpoint Identifier (special octet in PPR)
TX	Transmitter
U	
UI	Unit Interval
Z	
ZCS	Zero Code Suppression

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