

3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

MAX793/MAX794/MAX795

General Description

The MAX793/MAX794/MAX795 microprocessor (μ P) supervisory circuits monitor and control the activities of +3.0V/+3.3V μ Ps by providing backup-battery switchover, among other features such as low-line indication, μ P reset, write protection for CMOS RAM, and a watchdog (see the *Selector Guide* below). The backup-battery voltage can exceed V_{CC}, permitting the use of 3.6V lithium batteries in systems using 3.0V to 3.3V for V_{CC}.

The MAX793/MAX795 offer a choice of reset threshold voltage range (denoted by suffix letter): 3.00V to 3.15V (T), 2.85V to 3.00V (S), and 2.55V to 2.70V (R). The MAX794's reset threshold is set externally with a resistor divider. The MAX793/MAX794 are available in 16-pin DIP and narrow SO packages, and the MAX795 comes in 8-pin DIP and SO packages.

Selector Guide

FEATURE	MAX793	MAX794	MAX795
Active-Low Reset	✓	✓	✓
Active-High Reset	✓	✓	
Programmable Reset Threshold		✓	
Low-Line Early Warning Output	✓	✓	
Backup-Battery Switchover	✓	✓	✓
External Switch Driver	✓	✓	✓
Power-Fail Comparator	✓	✓	
Battery OK Output	✓		
Watchdog Input	✓	✓	
Battery Freshness Seal	✓	✓	
Manual Reset Input	✓	✓	
Chip-Enable Gating	✓	✓	✓
Pin-Package	16-DIP/SO	16-DIP/SO	8-DIP/SO

Applications

Battery-Powered Computers and Controllers
Embedded Controllers
Intelligent Controllers
Critical μ P Power Monitoring
Portable Equipment

Pin Configurations appear at end of data sheet.

Features

MAX793/MAX794/MAX795

- ◆ **Precision Supply-Voltage Monitor:**
 - Fixed Reset Trip Voltage (MAX793/MAX795)
 - Adjustable Reset Trip Voltage (MAX794)
- ◆ **Guaranteed Reset Assertion to V_{CC} = 1V**
- ◆ **Backup-Battery Power Switching—Battery Voltage Can Exceed V_{CC}**
- ◆ **On-Board Gating of Chip-Enable Signals—7ns Max Propagation Delay**

MAX793/MAX794 Only

- ◆ **Battery Freshness Seal**
- ◆ **Battery OK Output (MAX793)**
- ◆ **Uncommitted Voltage Monitor for Power-Fail or Low-Battery Warning**
- ◆ **Independent Watchdog Timer (1.6s timeout)**
- ◆ **Manual Reset Input**

Ordering Information

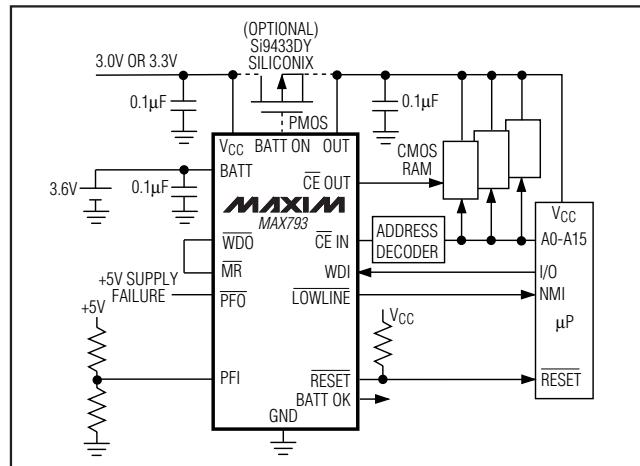
PART*	TEMP RANGE	PIN-PACKAGE
MAX793_CPE	0°C to +70°C	16 Plastic DIP
MAX793_CSE	0°C to +70°C	16 Narrow SO

Ordering Information continued at end of data sheet.

*The MAX793/MAX795 offer a choice of reset threshold voltage. Select the letter corresponding to the desired reset threshold voltage range (T = 3.00V to 3.15V, S = 2.85V to 3.00V, R = 2.55V to 2.70V) and insert it into the blank to complete the part number. The MAX794's reset threshold is adjustable.

Devices are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)

V _{CC}	-0.3V to +6.0V
V _{BATT}	-0.3V to +6.0V
All Other Inputs	-0.3V to the higher of V _{CC} or V _{BATT}
Continuous Input Current	
V _{CC}	200mA
V _{BATT}	50mA
GND	20mA
Output Current	
V _{OUT}	200mA
All Other Outputs	20mA

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.17V to 5.5V for the MAX793T/MAX795T, V_{CC} = 3.02V to 5.5V for the MAX793S/MAX795S, V_{CC} = 2.72V to 5.5V for the MAX793R/MAX794/MAX795R, V_{BATT} = 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V _{CC} , V _{BATT} (Note 1)		MAX79_C	1.0	5.5	5.5	V
		MAX79_E	1.1	5.5	5.5	
V _{CC} Supply Current (excluding I _{OUT} , I _{CE} OUT)	I _{SUPPLY}	MAX793/MAX794, MR = V _{CC}	V _{CC} < 3.6V	46	60	μA
			V _{CC} < 5.5V	62	80	
		MAX795	V _{CC} < 3.6V	35	50	
			V _{CC} < 5.5V	49	70	
V _{CC} Supply Current in Battery-Backup Mode (excluding I _{OUT})	I _{SUPPLY}	V _{CC} = 2.1V, V _{BATT} = 2.3V	MAX793/MAX794	32	45	μA
			MAX795	24	35	
BATT Supply Current (excluding I _{OUT}) (Note 2)					1	μA
BATT Leakage Current, Freshness Seal Enabled		V _{CC} = 0V, V _{OUT} = 0V			1	μA
Battery Leakage Current (Note 3)					0.5	μA
OUT Output Voltage in Normal Mode	V _{OUT}	I _{OUT} = 75mA	V _{CC} - 0.3	V _{CC} - 0.125		V
		I _{OUT} = 30mA (Note 4)	V _{CC} - 0.12	V _{CC} - 0.050		
		I _{OUT} = 250μA (Note 4)	V _{CC} - 0.001	V _{CC} - 0.5mV		
OUT Output Voltage in Battery-Backup Mode	V _{OUT}	V _{BATT} = 2.3V	I _{OUT} = 250μA	V _{BATT} - 0.1	V _{BATT} - 0.034	V
			I _{OUT} = 1mA		V _{BATT} - 0.14	
Battery Switch Threshold (V _{CC} falling)	V _{CC} - V _{BATT}	V _{SW} > V _{CC} > 1.75V (Note 5)		20	65	mV
			MAX793T/MAX795T	2.69	2.82	
		V _{BATT} > V _{CC} (Note 6)	MAX793S/MAX795S	2.55	2.68	
			MAX793R/MAX795R/MAX794	2.30	2.41	
Battery Switch Threshold (V _{CC} rising) (Note 7)	V _{CC} - V _{BATT}	This value is identical to the reset threshold, V _{CC} rising for V _{BATT} > V _{RST}				mV
		V _{BATT} < V _{RST}		25	65	

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.17V to 5.5V for the MAX793T/MAX795T, V_{CC} = 3.02V to 5.5V for the MAX793S/MAX795S, V_{CC} = 2.72V to 5.5V for the MAX793R/MAX794/MAX795R, V_{BATT} = 3.6V, TA = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Threshold (Note 8)	VRST	V _{CC} falling	MAX793T/MAX795T	3.00	3.075	3.15
			MAX793S/MAX795S	2.85	2.925	3.00
			MAX793R/MAX795R	2.55	2.625	2.70
		V _{CC} rising	MAX793T/MAX795T	3.00	3.085	3.17
			MAX793S/MAX795S	2.85	2.935	3.02
			MAX793R/MAX795R	2.55	2.635	2.72
RESET IN Threshold (MAX794 only)	VRST IN	V _{CC} falling	1.212	1.240	1.262	V
		V _{CC} rising	1.212	1.250	1.282	
RESET IN Leakage Current (MAX794 only)			-25	2	25	nA
Reset Timeout Period	t _{RP}	V _{CC} < 3.6V	140	200	280	ms
LOWLINE-to-Reset Threshold, (V _{LOWLINE} - VRST), V _{CC} Falling	V _{LR}	MAX793	30	45	60	mV
		MAX794	5	15	25	
Low-Line Comparator Hysteresis		MAX793		10		mV
		MAX794		10		mV
LOWLINE Threshold, V _{CC} Rising	V _{LL}	MAX793T/MAX795T		3.23		V
		MAX793S/MAX795S		3.08		
		MAX793R/MAX795R		2.78		
		MAX794		1.317		
PFI Input Threshold	V _{TH}	V _{PFI} falling	1.212	1.240	1.262	V
		V _{PFI} rising	1.212	1.250	1.287	
PFI Input Current			-25	2	25	nA
PFI Hysteresis, PFI Rising				10	20	mV
BATT OK Threshold (MAX793)	V _{BOK}		2.00	2.25	2.50	V
INPUT AND OUTPUT LEVELS						
RESET Output-Voltage High	V _{OH}	I _{SOURCE} = 300µA, V _{CC} = VRST min	0.8V _{CC}	0.86V _{CC}		V
BATT OK, BATT ON, WDO, LOWLINE Output-Voltage High	V _{OH}	I _{SOURCE} = 300µA, V _{CC} = VRST max	0.8V _{CC}	0.86V _{CC}		V
PFO Output-Voltage High	V _{OH}	I _{SOURCE} = 65µA, V _{CC} = VRST max	0.8V _{CC}			V
BATT ON Output-Voltage High	V _{OH}	I _{SOURCE} = 100µA, V _{CC} = 2.3V, V _{BATT} = 3V	0.8V _{BATT}			V
RESET Output Leakage Current (Note 9)	I _{LEAK}	V _{CC} = VRST max	-1	-1		µA
PFO Output Short to GND Current	I _{SC}	V _{CC} = 3.3V, V _{PFO} = 0V		180	500	µA
PFO, RESET, RESET, WDO, LOWLINE Output-Voltage Low	V _{OL}	I _{SINK} = 1.2mA; RESET, LOWLINE tested with V _{CC} = VRST min; RESET, BATOK, WDO tested with V _{CC} = VRST max		0.08	0.2V _{CC}	V

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.17V to 5.5V for the MAX793T/MAX795T, V_{CC} = 3.02V to 5.5V for the MAX793S/MAX795S, V_{CC} = 2.72V to 5.5V for the MAX793R/MAX794/MAX795R, V_{BATT} = 3.6V, TA = T_{MIN} to T_{MAX} , unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET Output-Voltage Low	V_{OL}	MAX79_C, $V_{BATT} = V_{CC}$ = 1.0V, I_{SINK} = 40 μ A	0.13	0.3	0.3	V
		MAX79_E, $V_{BATT} = V_{CC}$ = 1.2V, I_{SINK} = 200 μ A	0.17	0.3	0.3	
BATT ON Output-Voltage Low	V_{OL}	I_{SINK} = 3.2mA, V_{CC} = V_{RST} max			0.2 V_{CC}	V
All Inputs Including <u>PFO</u> (Note 10)	V_{IH}	V_{RST} max < V_{CC} < 5.5V			0.7 V_{CC}	V
	V_{IL}		0.3 V_{CC}			
MANUAL RESET INPUT						
MR Pulse Width	t_{MR}	MAX793/MAX794 only	100			ns
MR-to-Reset Delay	t_{MD}	MAX793/MAX794 only	75	250	250	ns
MR Pullup Current		MAX793/MAX794 only, \overline{MR} = 0V	25	70	250	μ A
CHIP-ENABLE GATING						
\overline{CE} IN Leakage Current	I_{LEAK}	Disable mode		± 10		nA
\overline{CE} IN-to- \overline{CE} OUT Resistance		Enable mode, V_{CC} = V_{RST} max		46		Ω
\overline{CE} IN-to- \overline{CE} OUT Propagation Delay		V_{CC} = V_{RST} max, Figure 9	2	7	7	ns
\overline{CE} OUT Drive from \overline{CE} IN	V_{OH}	V_{CC} = V_{RST} max, I_{OUT} = -1mA, $V_{\overline{CE} IN}$ = V_{CC}	0.8 V_{CC}			V
	V_{OL}	V_{CC} = V_{RST} max, I_{OUT} = 1.6mA, $V_{\overline{CE} IN}$ = 0V			0.2 V_{CC}	
Reset to \overline{CE} OUT High Delay				10		μ s
\overline{CE} OUT Output-Voltage High (reset active)	V_{OH}	I_{OH} = 500 μ A, V_{CC} < 2.3V	0.8 V_{BATT}			V
WATCHDOG (MAX793/MAX794 only)						
WDI Input Current		0V < V_{CC} < 5.5V	-1	0.01	1	μ A
Watchdog Timeout Period	t_{WD}		1.00	1.60	2.25	s
WDI Pulse Width			100			ns

Note 1: V_{CC} supply current, logic-input leakage, watchdog functionality (MAX793/MAX794), \overline{MR} functionality (MAX793/MAX794), PFI functionality (MAX793/MAX794), and state of RESET and RESET (MAX793/MAX794) tested at V_{BATT} = 3.6V and V_{CC} = 5.5V. The state of RESET is tested at V_{CC} = V_{CC} min.

Note 2: Tested at V_{BATT} = 3.6V, V_{CC} = 3.5V and 0V. The battery current rises to 10 μ A over a narrow transition window around V_{CC} = 1.9V.

Note 3: Leakage current into the battery is tested under the worst-case conditions at V_{CC} = 5.5V, V_{BATT} = 1.8V and V_{CC} = 1.5V, V_{BATT} = 1.0V.

Note 4: Guaranteed by design.

Note 5: When $V_{SW} > V_{CC} > V_{BATT}$, OUT remains connected to V_{CC} until V_{CC} drops below V_{BATT} . The V_{CC} -to- V_{BATT} comparator has a small 15mV typical hysteresis to prevent oscillation. For $V_{CC} < 1.75V$ (typical), OUT switches to BATT regardless of V_{BATT} .

Note 6: When $V_{BATT} > V_{CC} > V_{SW}$, OUT remains connected to V_{CC} until V_{CC} drops below the battery switch threshold (V_{SW}).

Note 7: OUT switches from BATT to V_{CC} when V_{CC} rises above the reset threshold, if $V_{BATT} > V_{RST}$. In this case, switchover back to V_{CC} occurs at the exact voltage that causes reset to be asserted, however, switchover occurs 200ms prior to reset. If $V_{BATT} < V_{RST}$, OUT switches from BATT to V_{CC} when V_{CC} exceeds V_{BATT} .

Note 8: The reset threshold tolerance is wider for V_{CC} rising than for V_{CC} falling to accommodate the 10mV typical hysteresis, which prevents internal oscillation.

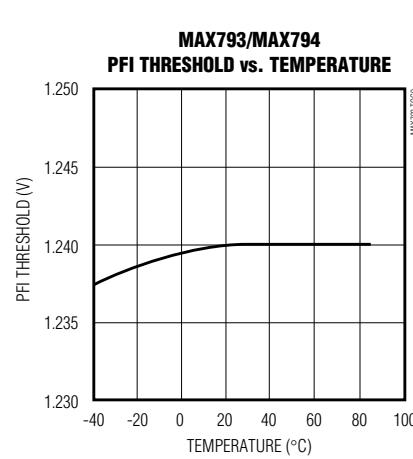
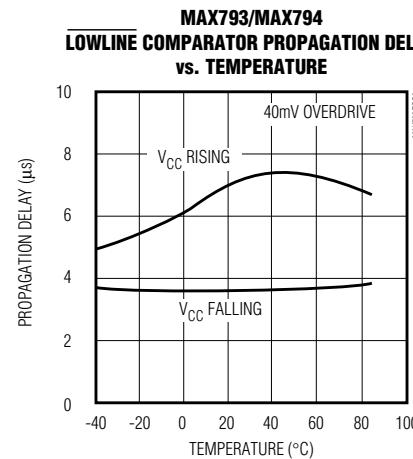
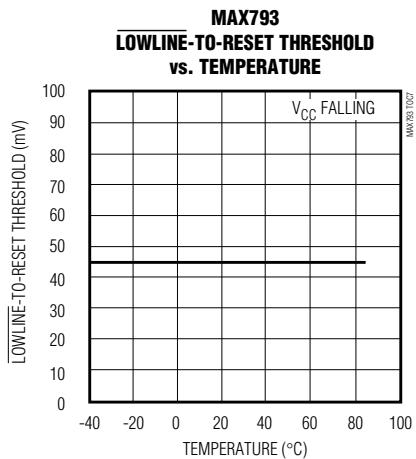
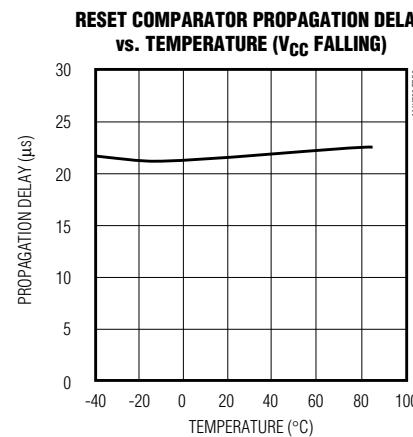
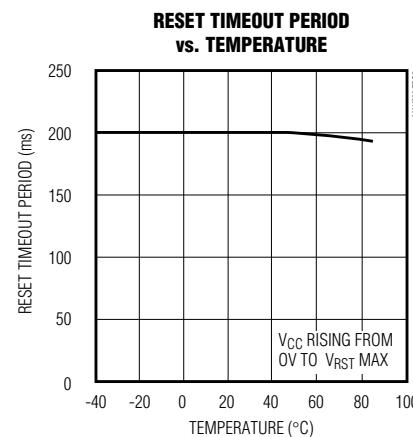
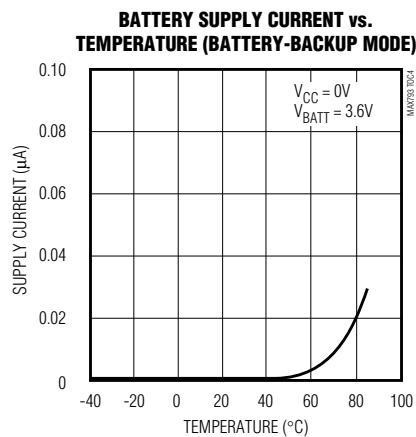
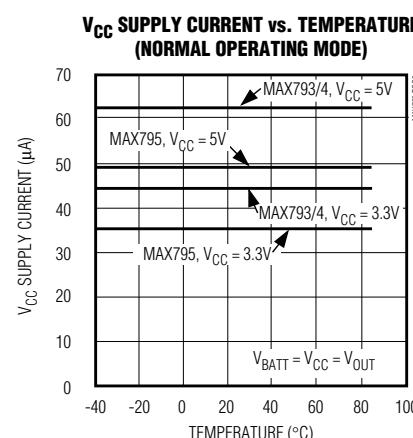
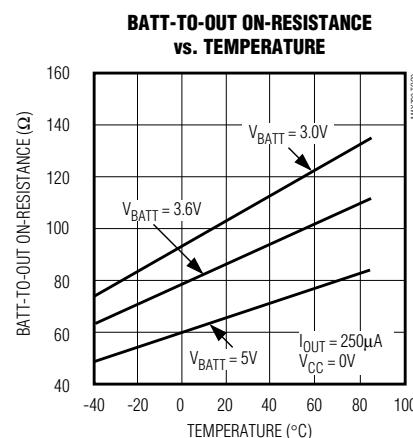
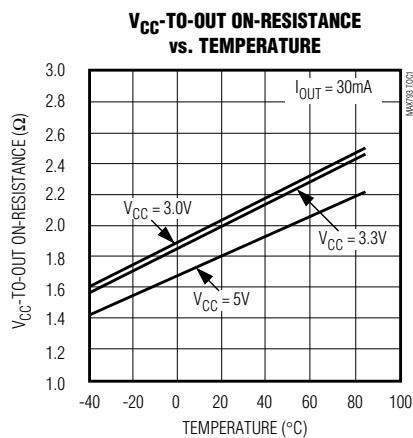
Note 9: The leakage current into or out of the RESET pin is tested with RESET not asserted (RESET output high impedance).

Note 10: PFO is normally an output, but is used as an input when activating the battery freshness seal.

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Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

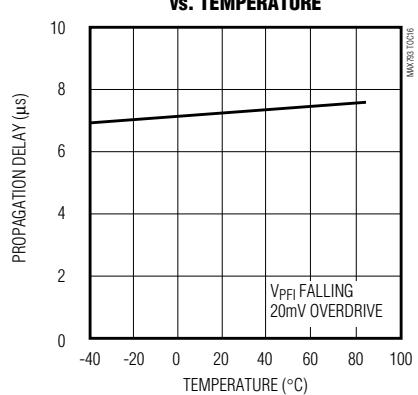
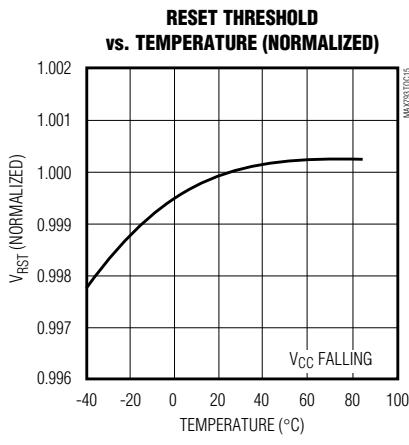
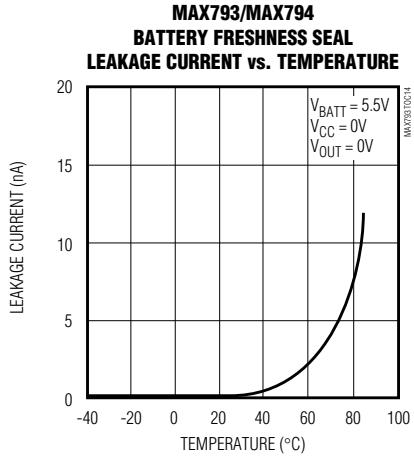
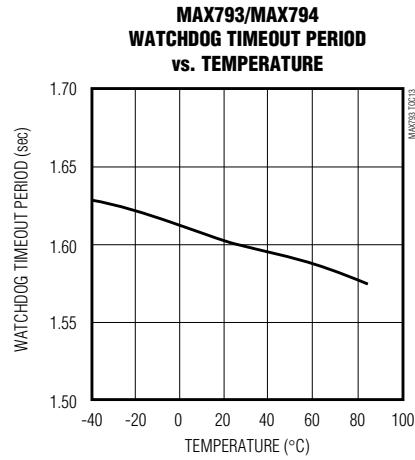
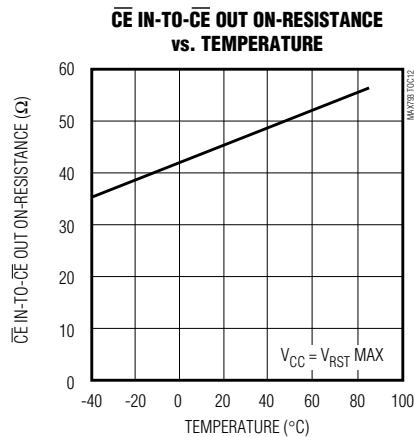
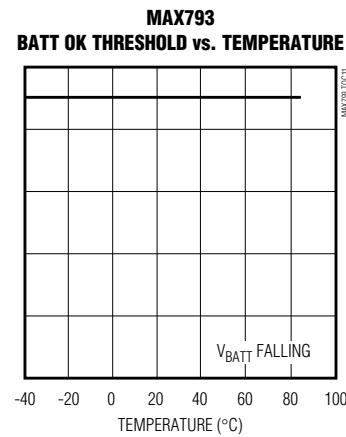
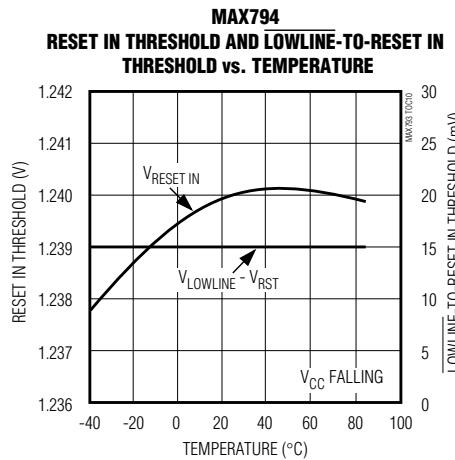


MAX793/MAX794/MAX795

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Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



3.0V/3.3V Adjustable Microprocessor Supervisory Circuits

Pin Description

PIN		NAME	FUNCTION
MAX793/ MAX794	MAX795		
1	1	OUT	Supply Output for CMOS RAM. When Vcc rises above the reset threshold or above VBATT, OUT is connected to Vcc through an internal p-channel MOSFET switch. When Vcc falls below Vsw and VBATT, BATT connects to OUT.
2	2	Vcc	Main Supply Input
3	—	BATT OK (MAX793)	Battery Status Output. High in normal operating mode when VBATT exceeds VBOK, otherwise low. VBATT is checked continuously. Disabled and logic low while Vcc is below Vsw.
		RESET IN (MAX794)	Reset Input. Connect to an external resistor-divider to select the reset threshold. The reset threshold can be programmed anywhere in the Vsw to 5.5V range.
4	—	PFI	Power-Fail Comparator Input. When PFI is less than VPFT or when Vcc falls below Vsw, \overline{PFO} goes low; otherwise, \overline{PFO} remains high (see <i>Power-Fail Comparator</i> section). Connect to Vcc if unused.
5	3	BATT ON	Logic Output/External Bypass Switch-Driver Output. High when OUT switches to BATT. Low when OUT switches to Vcc. Connect the base/gate of PNP/PMOS transistor to BATT ON for IOUT requirements exceeding 75mA.
6	4	GND	Ground
7	—	\overline{PFO}	Power-Fail Comparator Output. When PFI is less than VPFT or when Vcc falls below Vsw, \overline{PFO} goes low; otherwise, \overline{PFO} remains high. \overline{PFO} is also used to enable the battery freshness seal (see <i>Battery Freshness Seal</i> and <i>Power-Fail Comparator</i> sections).
8	—	\overline{MR}	Manual Reset Input. A logic low on \overline{MR} asserts reset. Reset remains asserted as long as \overline{MR} is low and for 200ms after \overline{MR} returns high. The active-low input has an internal 70 μ A pullup current. It can be driven from a TTL- or CMOS-logic line or shorted to ground with a switch. Leave open if unused.
9	—	\overline{WDO}	Watchdog Output. \overline{WDO} goes low if WDI remains either high or low for longer than the watchdog timeout period. \overline{WDO} returns high on the next transition of WDI. \overline{WDO} is a logic high for Vsw < Vcc < VRST, and low when Vcc is below Vsw.
10	—	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and WDO goes low. WDO returns high on the next transition of WDI. Connect \overline{WDO} to \overline{MR} to generate a reset due to a watchdog fault.
11	5	\overline{CE} IN	Chip-Enable Input. The input to the chip-enable gating circuit. Connect to GND if unused.
12	6	\overline{CE} OUT	Chip-Enable Output. \overline{CE} OUT goes low only when \overline{CE} IN is low and reset is not asserted. If \overline{CE} IN is low when reset is asserted, \overline{CE} OUT remains low for 10 μ s or until \overline{CE} IN goes high, whichever occurs first. \overline{CE} OUT is pulled up to OUT.
13	—	RESET	Active-High Reset Output. Sources and sinks current. RESET is the inverse of \overline{RESET} .
14	—	LOWLINE	Early Power-Fail Warning Output. Low when Vcc falls to VLR. This output can be used to generate an NMI to provide early warning of imminent power failure.
15	7	\overline{RESET}	Open-Drain, Active-Low Reset Output. Pulses low for 200ms when triggered, and stays low whenever Vcc is below the reset threshold or when \overline{MR} is a logic low. It remains low for 200ms after either Vcc rises above the reset threshold, the watchdog triggers a reset (\overline{WDO} connected to \overline{MR}), or \overline{MR} goes low to high.
16	8	BATT	Backup-Battery Input. When Vcc falls below Vsw and VBATT, OUT switches from Vcc to BATT. When Vcc rises above the reset threshold or above VBATT, OUT reconnects to Vcc. VBATT can exceed Vcc. Connect Vcc, OUT, and BATT together if no battery is used.

MAX793/MAX794/MAX795

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Detailed Description

General Timing Characteristics

The MAX793/MAX794/MAX795 are designed for 3.3V and 3V systems, and provide a number of supervisory functions (see the *Selector Guide* on the front page). Figures 1 and 2 show the typical timing relationships of the various outputs during power-up and power-down with typical V_{CC} rise and fall times.

Manual Reset Input (MAX793/MAX794)

Many microprocessor-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the MAX793/MAX794, a logic low on \overline{MR} asserts reset. Reset remains asserted while \overline{MR} is low, and for t_{RP} (200ms) after it returns high. During the first half of the reset time-

out period (t_{RP}), the state of \overline{MR} is ignored if \overline{PFO} is externally forced low to facilitate enabling the battery freshness seal. \overline{MR} has an internal 70 μ A pullup current, so it can be left open if it is not used. This input can be driven with TTL- or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from \overline{MR} to GND to create a manual-reset function; external debounce circuitry is not required. If \overline{MR} is driven from long cables or the device is used in a noisy environment, connect a 0.1 μ F capacitor from \overline{MR} to ground to provide additional noise immunity.

Reset Outputs

A microprocessor's (μ P's) reset input starts the μ P in a known state. These MAX793/MAX794/MAX795 μ P supervisory circuits assert a reset to prevent code execution errors during power-up, power-down, and

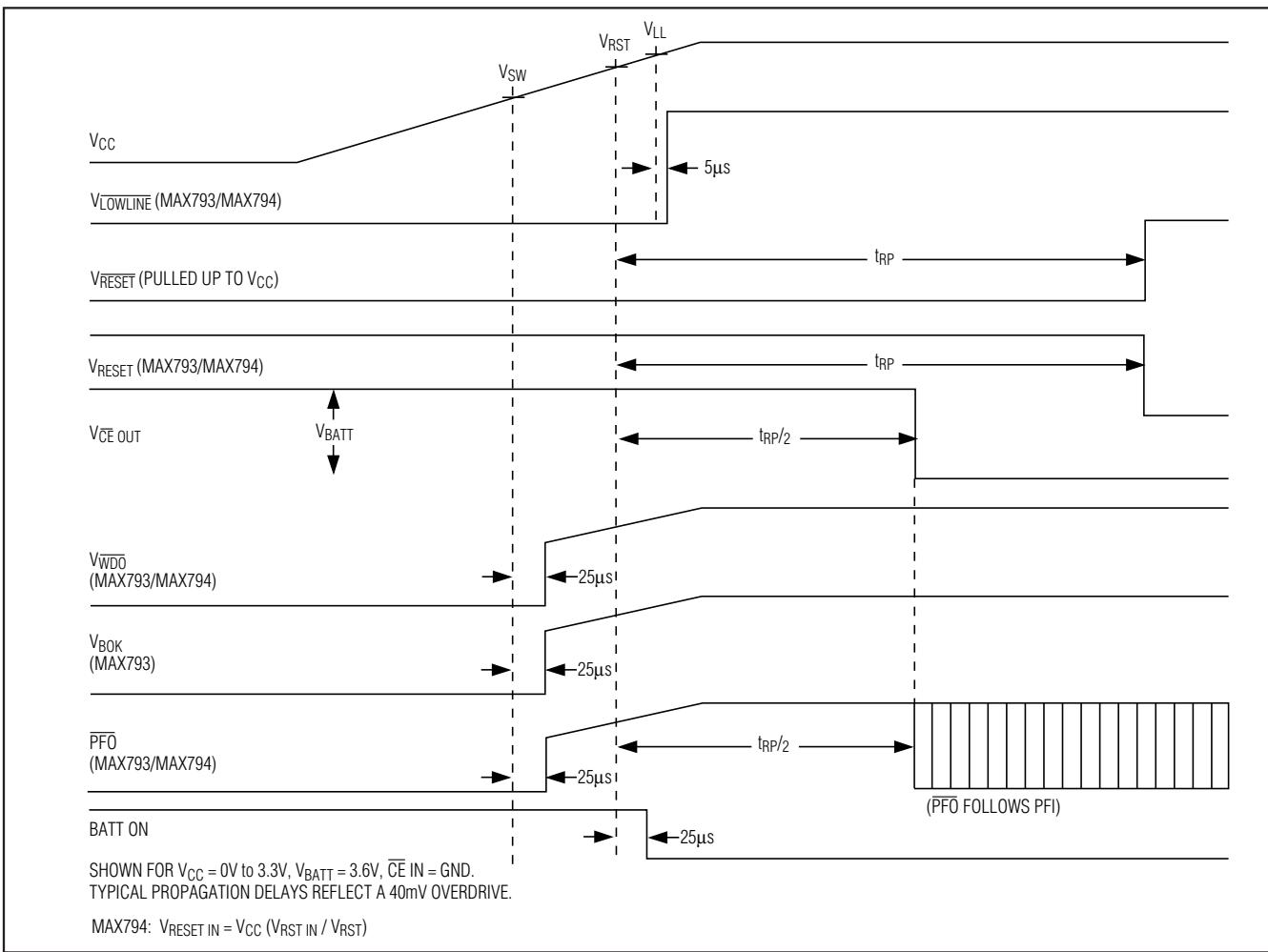


Figure 1. Timing Diagram, V_{CC} Rising

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brownout conditions. RESET is guaranteed to be a logic low for $0V < V_{CC} < V_{RST}$, provided V_{BATT} is greater than 1V. Without a backup battery ($V_{BATT} = V_{CC} = V_{OUT}$), RESET is guaranteed valid for $V_{CC} \geq 1V$. Once V_{CC} exceeds the reset threshold, an internal timer keeps RESET low for the reset timeout period (t_{RP}); after this interval, RESET becomes high impedance (Figure 2). RESET is an open-drain output, and requires a pullup resistor to V_{CC} (Figure 3). Use a $4.7k\Omega$ to $1M\Omega$ pullup resistor that provides sufficient current to assure the proper logic levels to the μ P.

If a brownout condition occurs (V_{CC} dips below the reset threshold), RESET goes low. Each time RESET is asserted, it stays low for the reset timeout period. Any time V_{CC} goes below the reset threshold, the internal timer restarts.

The watchdog output (\overline{WDO}) can also be used to initiate a reset. See the *Watchdog Output* section.

The RESET output is the inverse of the \overline{RESET} output, and it can both source and sink current.

MAX793/MAX794/MAX795

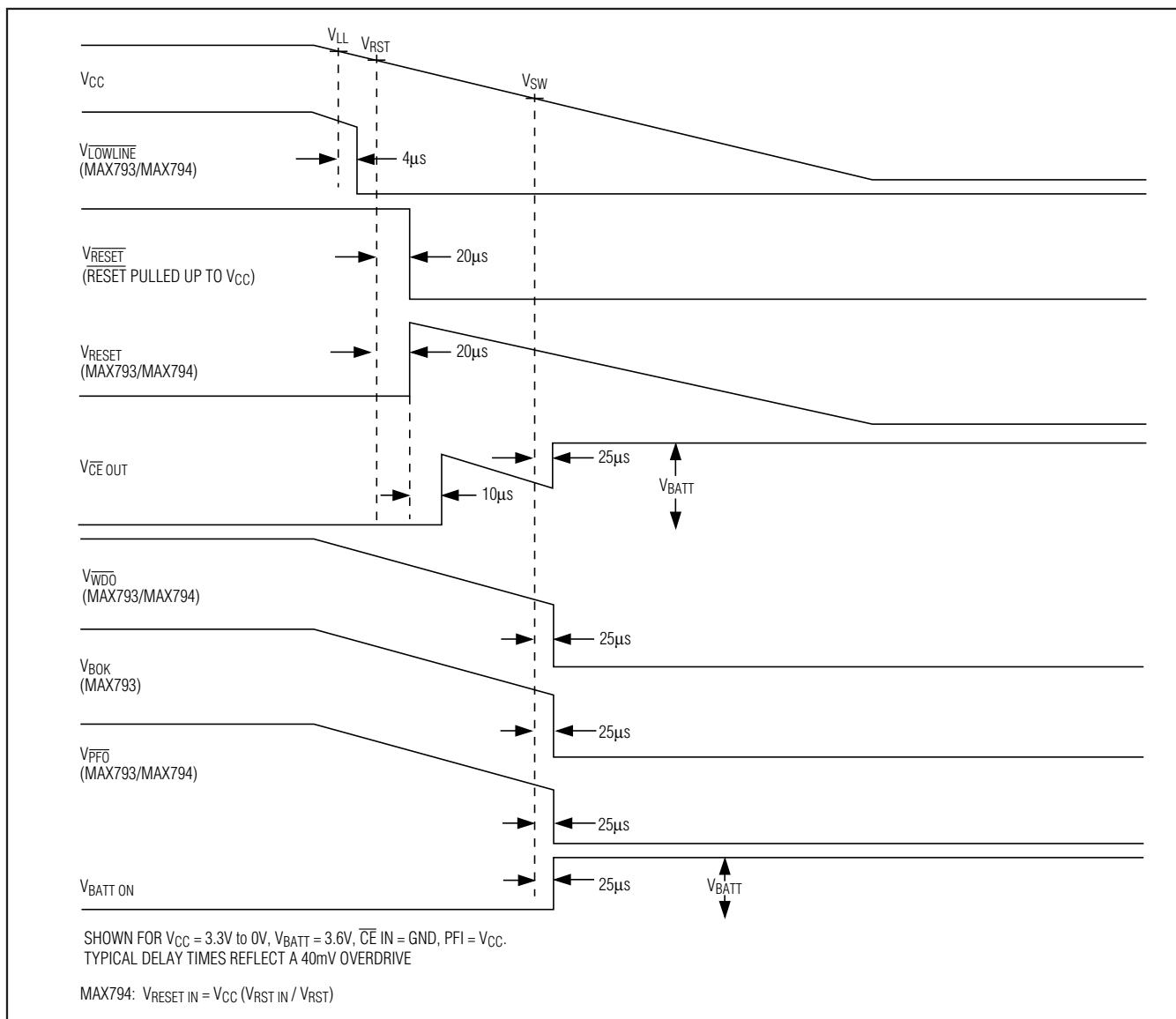


Figure 2. Timing Diagram, V_{CC} Falling

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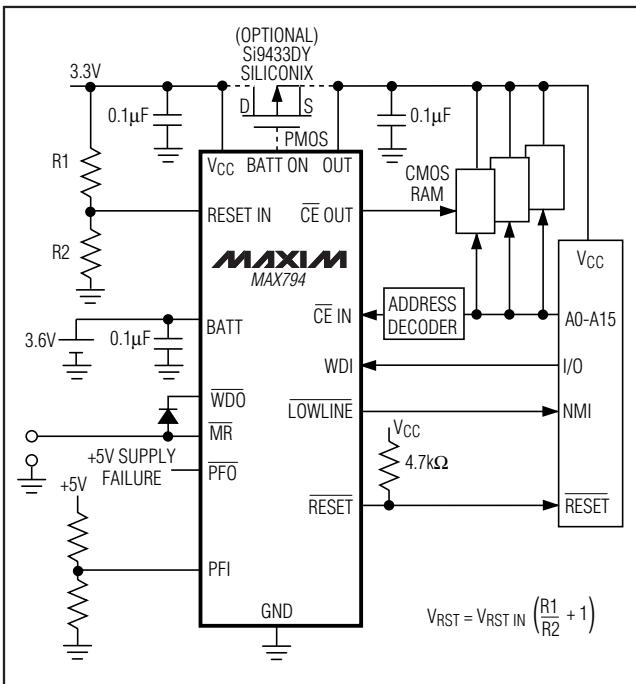


Figure 3. MAX794 Standard Application Circuit

Reset Threshold

The MAX793T/MAX795T are intended for 3.3V systems with a $\pm 5\%$ power-supply tolerance and a 10% systems tolerance. Except when **MR** is asserted, reset does not assert as long as the power supply remains above 3.15V (3.3V - 5%). Reset is guaranteed to assert before the power supply falls below 3.0V (3.3V - 10%).

The MAX793S/MAX795S are designed for 3.3V $\pm 10\%$ power supplies. Except when **MR** is asserted, they are guaranteed not to assert reset as long as the supply remains above 3.0V (3.0V is just above 3.3V - 10%). Reset is guaranteed to assert before the power supply falls below 2.85V (3.3V - 14%).

The MAX793R/MAX795R are optimized to monitor 3.0V $\pm 10\%$ power supplies. Reset does not occur until **Vcc** falls below 2.7V (3.0V - 10%), but is guaranteed to occur before the supply falls below 2.55V (3.0V - 15%).

Program the MAX794's reset threshold with an external voltage divider to **RESET IN**. The reset-threshold tolerance is a combination of the **RESET IN** tolerance and the tolerance of the resistors used to make the external voltage divider. Calculate the reset threshold as follows:

$$VRST = VRST IN (R1 / R2 + 1)$$

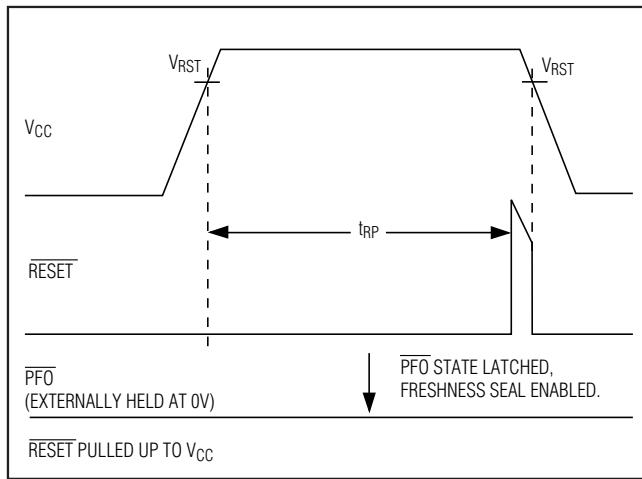


Figure 4. Battery Freshness Seal Enable Timing

Using the standard application circuit (Figure 3), the reset threshold can be programmed anywhere in the range of **Vsw** (the battery switch threshold) to 5.5V. Reset is asserted when **Vcc** falls below **Vsw**.

Battery Freshness Seal

The MAX793/MAX794's battery freshness seal disconnects the backup battery from internal circuitry until it is needed. This allows an OEM to ensure that the backup battery connected to **BATT** is fresh when the final product is put to use. To enable the freshness seal, connect a battery to **BATT**, ground **PFO**, bring **Vcc** above the reset threshold, and hold it there until reset is deasserted following the reset timeout period, then bring **Vcc** back down again (Figure 4). Once the battery freshness seal is enabled (disconnecting the backup battery from the internal circuitry and anything connected to **OUT**), it remains enabled until **Vcc** is brought above **VRST**. Note that connecting **PFO** to **MR** does not interfere with battery freshness seal operation.

BATT OK Output (MAX793)

BATT OK indicates the status of the backup battery. When reset is not asserted, the MAX793 checks the battery voltage continuously. If **VBATT** is below **VBOK** (2.0V min), **BATT OK** goes low; otherwise, it remains pulled up to **Vcc**. **BATT OK** also goes low when **Vcc** goes below **Vsw**.

Watchdog Input (MAX793/MAX794)

In the MAX793/MAX794, the watchdog circuit monitors the **μP**'s activity. If the **μP** does not toggle the watchdog input (**WDI**) within 1.6s, **WDO** goes low. The internal 1.6s timer is cleared and **WDO** returns high either when

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MAX793/MAX794/MAX795

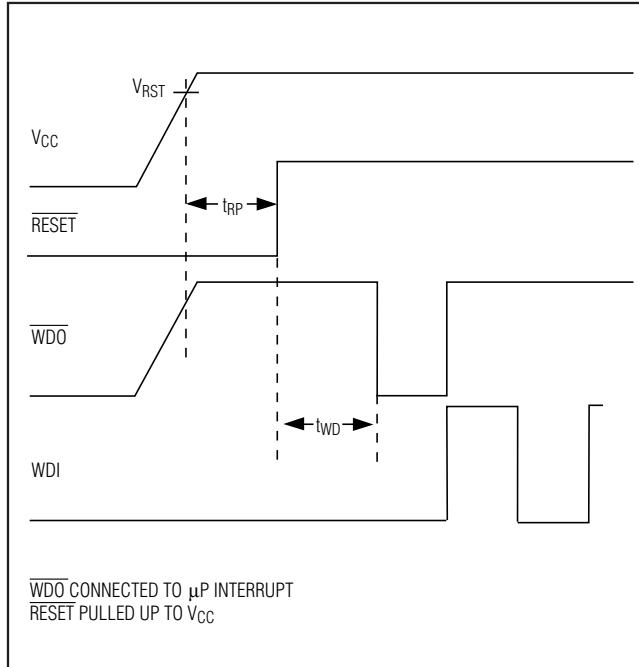


Figure 5. Watchdog Timing Relationship

a reset occurs or when a transition (low-to-high or high-to-low) takes place at WDI. As long as reset is asserted, the timer remains cleared and does not count. As soon as reset is released or WDI changes state, the timer starts counting (Figure 5). WDI can detect pulses as short as 100ns. Unlike the 5V MAX690 family, the watchdog function **cannot** be disabled.

Watchdog Output (MAX793/MAX794)

In the MAX793/MAX794, WDO remains high (WDO) if there is a transition or pulse at WDI during the watchdog timeout period. WDO goes low if no transition occurs at WDI during the watchdog timeout period. The watchdog function is disabled and WDO is a logic high when reset is asserted if VCC is above Vsw. WDO is a logic low when VCC is below Vsw.

If a system reset is desired on every watchdog fault, simply diode-OR connect WDO to MR (Figure 6). When a watchdog fault occurs in this mode, WDO goes low, pulling MR low, which causes a reset pulse to be issued. Ten microseconds after reset is asserted, the watchdog timer clears and WDO returns high. This delay results in a 10μs pulse at WDO, allowing external circuitry to capture a watchdog fault indication. A continuous high or low on WDI causes 200ms reset pulses to be issued every 1.6s.

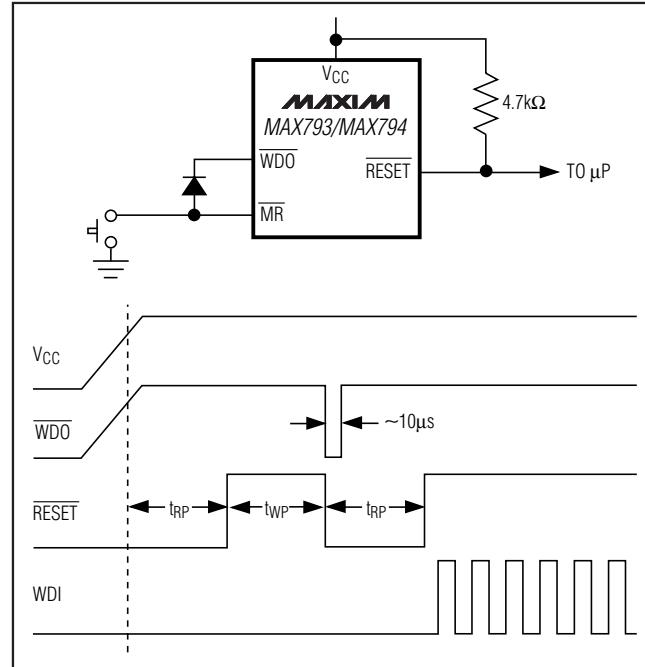


Figure 6. Generating a Reset on Each Watchdog Fault

Chip-Enable Signal Gating

Internal gating of chip-enable (CE) signals prevents erroneous data from corrupting CMOS RAM in the event of an undervoltage condition. The MAX793/MAX794/MAX795 use a series transmission gate from \overline{CE} IN to \overline{CE} OUT. During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from \overline{CE} IN to \overline{CE} OUT enables these μ P supervisors to be used with most μ Ps. If \overline{CE} IN is low when reset asserts, \overline{CE} OUT remains low for typically 10μs to permit completion of the current write cycle.

Chip-Enable Input

The CE transmission gate is disabled and \overline{CE} IN is high impedance (disabled mode) while reset is asserted. During a power-down sequence when VCC passes the reset threshold, the CE transmission gate disables and \overline{CE} IN immediately becomes high impedance if the voltage at \overline{CE} IN is high. If \overline{CE} IN is low when reset asserts, the CE transmission gate disables at the moment \overline{CE} IN goes high, or 10μs after reset asserts, whichever occurs first (Figure 8). This permits the current write cycle to complete during power-down.

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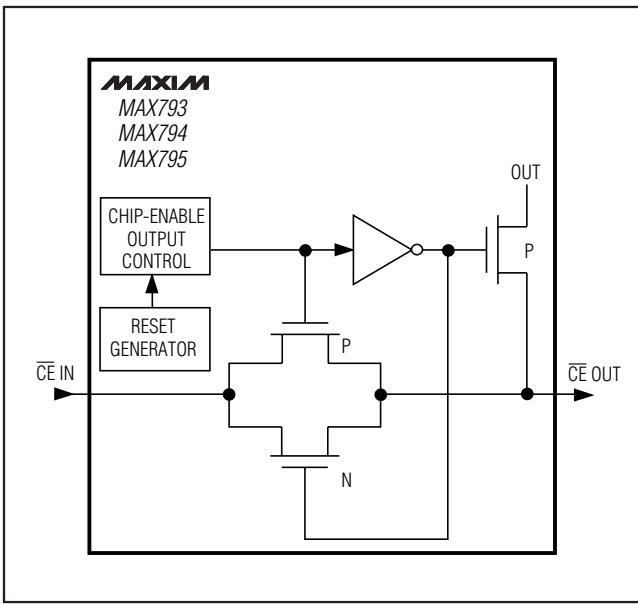


Figure 7. Chip-Enable Transmission Gate

The CE transmission gate remains disabled and \overline{CE} IN remains high impedance (regardless of \overline{CE} IN activity) for the first half of the reset timeout period ($t_{RP} / 2$), any time a reset is generated. While disabled, \overline{CE} IN is high impedance. When the CE transmission gate is enabled, the impedance of \overline{CE} IN appears as a 46Ω resistor in series with the load at \overline{CE} OUT.

The propagation delay through the CE transmission gate depends on V_{CC} , the source impedance of the drive connected to CE IN, and the loading on \overline{CE} OUT. The CE propagation delay is production tested from the 50% point on \overline{CE} IN to the 50% point on \overline{CE} OUT using a 50Ω driver and 50pF of load capacitance (Figure 9). For minimum propagation delay, minimize the capacitive load at \overline{CE} OUT and use a low-output-impedance driver.

Chip-Enable Output

When the CE transmission gate is enabled, the impedance of \overline{CE} OUT is equivalent to a 46Ω resistor in series with the source driving \overline{CE} IN. In the disabled mode, the transmission gate is off and an active pullup connects \overline{CE} OUT to OUT (Figure 8). This pullup turns off when the transmission gate is enabled.

Early Power-Fail Warning (MAX793/MAX794)

Critical systems often require an early warning indicating that power is failing. This warning provides time for the μ P to store vital data and take care of any additional "housekeeping" functions, before the power supply gets too far out of tolerance for the μ P to operate reliably. The MAX793/MAX794 offer two methods of achieving this early warning. If access to the unregulated supply is feasible, the power-fail comparator input (PFI) can be connected to the unregulated supply through a voltage divider, with the power-fail comparator output (PFO) providing the NMI to the μ P (Figure

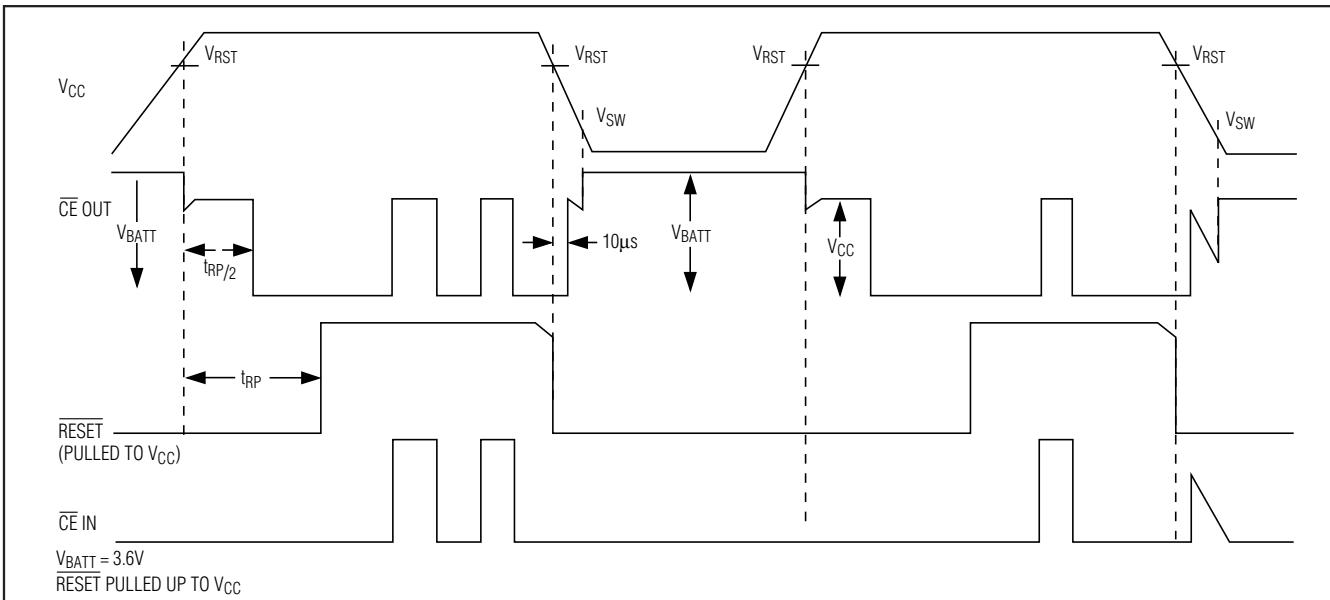


Figure 8. Chip-Enable Timing

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MAX793/MAX794/MAX795

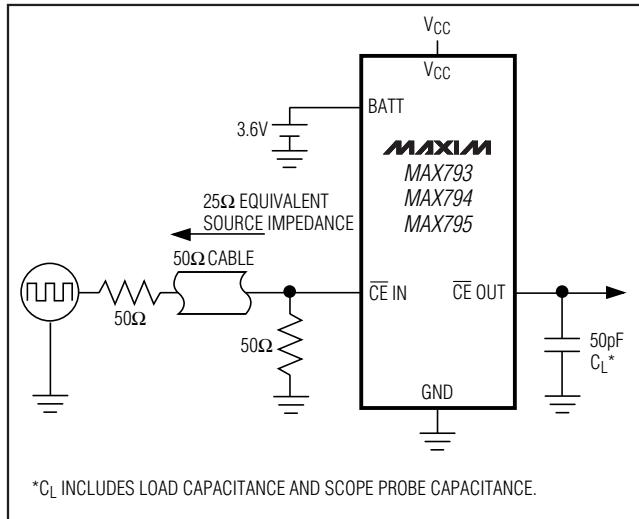


Figure 9. CE Propagation Delay Test Circuit

10). If there is no easy access to the unregulated supply, the LOWLINE output can be used to generate an NMI to the μ P (see LOWLINE Output section).

LOWLINE Output (MAX793/MAX794)

The low-line comparator monitors Vcc with a threshold voltage typically 45mV above the reset threshold (10mV of hysteresis) for the MAX793, and 15mV above RESET IN (4mV of hysteresis) for the MAX794. For normal operation (Vcc above the reset threshold), LOWLINE is pulled to Vcc. Use LOWLINE to provide an NMI to the μ P when power begins to fall.

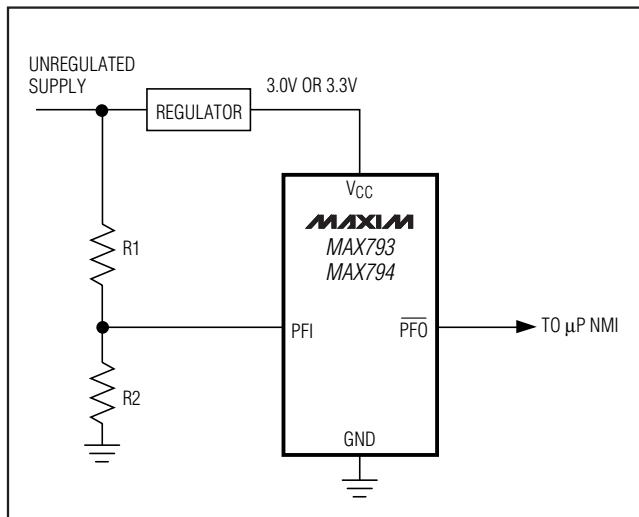


Figure 10. Using the Power-Fail Comparator to Generate Power-Fail Warning

In most battery-operated portable systems, reserve energy in the battery provides ample time to complete the shutdown routine once the low-line warning is encountered and before reset asserts. If the system must also contend with a more rapid Vcc fall time, such as when the main battery is disconnected or a high-side switch is opened during normal operation, use capacitance on the Vcc line to provide time to execute the shutdown routine (Figure 11).

First, calculate the worst-case time required for the system to perform its shutdown routine. Then, with the worst-case shutdown time, the worst-case load current, and the minimum low-line to reset threshold (VLR min), calculate the amount of capacitance required to allow the shutdown routine to complete before reset is asserted:

$$C_{HOLD} > I_{LOAD} \times t_{SHDN} / V_{LR}$$

where I_{LOAD} is the current being drained from the capacitor, V_{LR} is the low-line to reset threshold difference ($V_{LL} - V_{RST}$), and t_{SHDN} is the time required for the system to complete an orderly shutdown routine.

Power-Fail Comparator (MAX793/MAX794)

The MAX793/MAX794's PFI input is compared to an internal reference. If PFI is less than the power-fail threshold (VPFT), \overline{PFO} goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply (Figure 12). However, the comparator does not need to be dedicated to this function because it is completely separate from the rest of the circuitry.

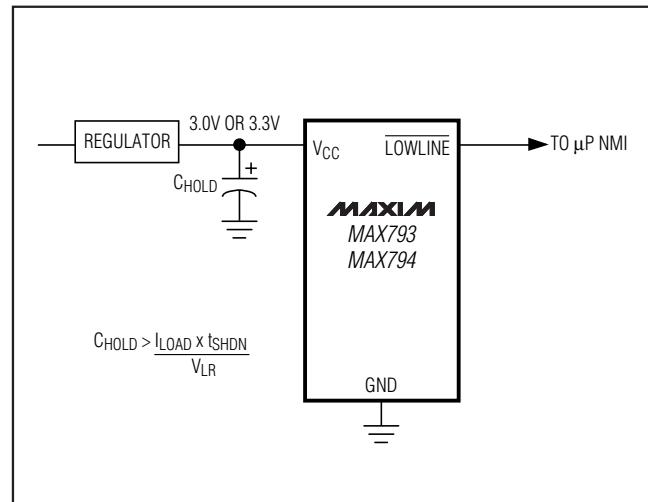


Figure 11. Using LOWLINE to Provide Power-Fail Warning to the μ P

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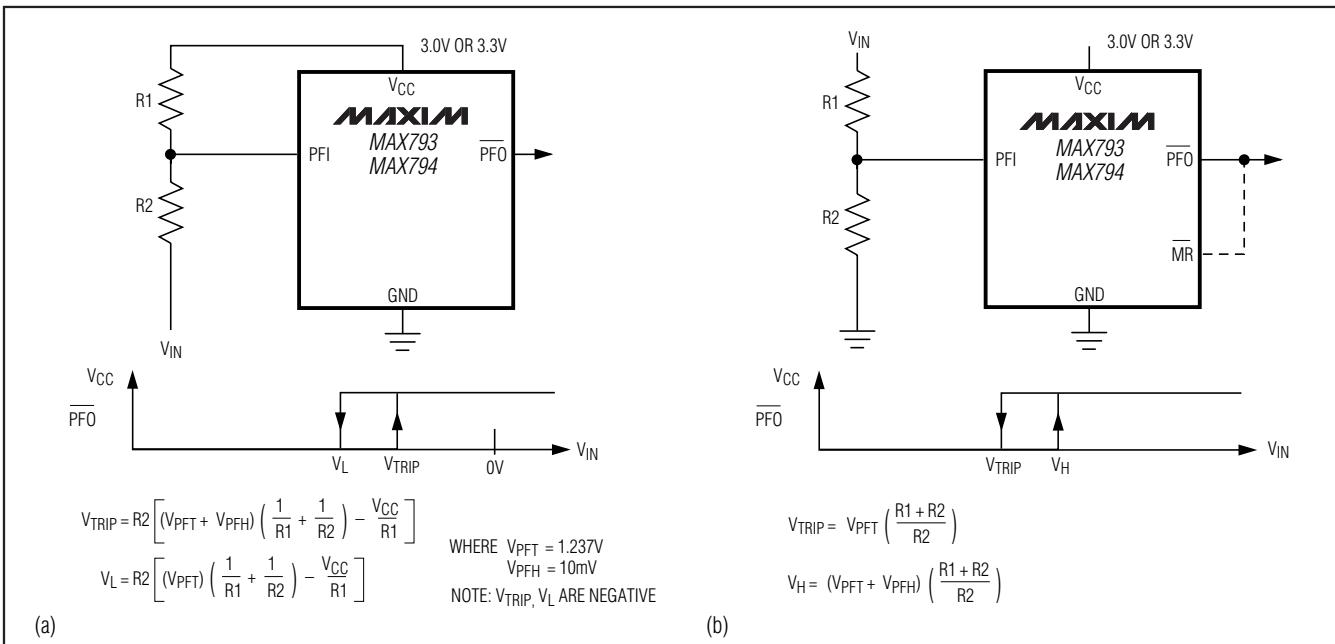


Figure 12. Using the Power-Fail Comparator to Monitor an Additional Power Supply: (a) V_{IN} Is Negative, (b) V_{IN} Is Positive

The power-fail comparator turns off and $\overline{\text{PFO}}$ goes low when VCC falls below Vsw on power-down. During the first half of the reset timeout period (t_{RP}), $\overline{\text{PFO}}$ is forced high, irrespective of VPFI . At the beginning of the second half of t_{RP} , the power-fail comparator is enabled and $\overline{\text{PFO}}$ follows PFI . If the comparator is unused, connect PFI to VCC and leave $\overline{\text{PFO}}$ unconnected. $\overline{\text{PFO}}$ can be connected to MR so that a low voltage on PFI generates a reset (Figure 12b). In this configuration, when the monitored voltage causes PFI to fall below VPFT , $\overline{\text{PFO}}$ pulls $\overline{\text{MR}}$ low, causing a reset to be asserted. Reset remains asserted as long as $\overline{\text{PFO}}$ holds $\overline{\text{MR}}$ low, and for 200ms after $\overline{\text{PFO}}$ pulls $\overline{\text{MR}}$ high when the monitored supply is above the programmed threshold.

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at BATT, the devices automatically switch RAM to backup power when V_{CC} falls. In order to allow the backup battery (e.g., a 3.6V lithium cell) to have a higher voltage than V_{CC} , this family of μ P supervisors (designed for 3.3V and 3V systems) does not always connect BATT to OUT when $VBATT$ is greater than V_{CC} . BATT connects to OUT (through a 140Ω switch) either when V_{CC} falls below V_{SW} and

VBATT is greater than VCC, or when VCC falls below 1.75V (typ) regardless of the BATT voltage.

Switchover at Vsw ensures that battery-backup mode is entered before Vout gets too close to the 2.0V minimum required to reliably retain data in most CMOS RAM, (switchover at higher Vcc voltages would decrease backup-battery life). When Vcc recovers, switchover is deferred either until Vcc crosses VBATT if VBATT is below VRST, or when Vcc rises above the reset threshold (VRST) if VBATT is above VRST. This power-up switchover technique prevents Vcc from charging the backup battery through OUT when using an external transistor driven by BATT ON. OUT connects to Vcc through a 4Ω (max) PMOS power switch when Vcc crosses the reset threshold (Figure 13).

BATT ON (MAX793/MAX794)

BATT ON is high when OUT is connected to BATT. Although BATT ON can be used as a logic output to indicate the battery switchover status, it is most often used as a gate or base drive for an external pass transistor for high-current applications (see *Driving an External Switch with BATT ON* in the *Applications Information* section). When VCC exceeds VRST on power-up, BATT ON sinks 3.2mA at 0.4V. In battery-backup mode, this terminal sources 100 μ A from BATT.

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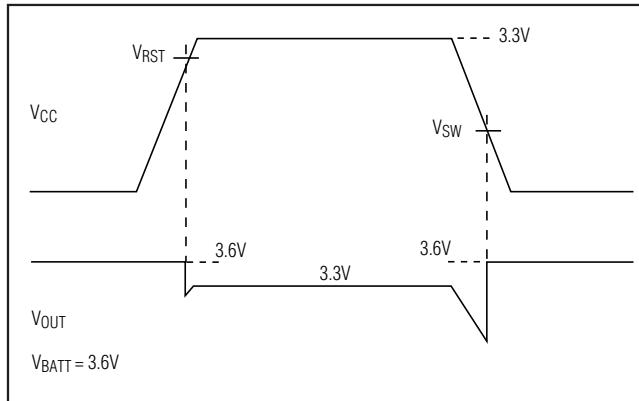


Figure 13. Battery Switchover Timing

Table 1. Input and Output Status in Battery-Backup Mode

PIN NAME	STATUS
OUT	Connected to BATT through an internal 140 Ω switch
V _{CC}	Disconnected from OUT
BATT ON	Pulled up to BATT
BATT OK	Logic low
PFI	Disabled
PFO	Logic low
MR	Disabled, but still pulled up to V _{CC}
WDO	Logic low
WDI	Disabled
RESET	Logic low
RESET	Pulled up to V _{CC}
BATT	Connected to OUT
LOWLINE	Logic low
CE IN	High impedance
CE OUT	Pulled to BATT

Applications Information

These μ P supervisory circuits are not short-circuit protected. Shorting V_{OUT} to ground, excluding power-up transients such as charging a decoupling capacitor, destroys the device. Decouple both V_{CC} and BATT pins to ground by placing 0.1 μ F ceramic capacitors as close to the device as possible.

Driving an External Switch with BATT ON

BATT ON can be directly connected to the base of a PNP transistor or the gate of a PMOS transistor. The PNP connection is straightforward: connect the emitter

to V_{CC}, the collector to OUT, and the base to BATT ON (Figure 14a). No current-limiting resistor is required, but a resistor connecting the base of the PNP to BATT ON can be used to limit the current drawn from V_{CC}, prolonging battery life in portable equipment.

If you are using a PMOS transistor, however, it must be connected backwards from the traditional method. Connect the gate to BATT ON, the drain to V_{CC}, and the source to OUT (Figure 14b). This method orients the body diode from V_{CC} to OUT and prevents the backup battery from discharging through the FET when its gate is high. Two PMOS transistors in the Siliconix LITTLE FOOT® series are specified with V_{GS} down to -2.7V. The Si9433DY has a maximum 100m Ω drain-source on-resistance with 2.7V of gate drive and a 2A drain-source current. The Si9434DY specifies a 60m Ω drain-source on-resistance with 2.7V of gate drive and a 5.1A drain-source current.

Using a Super Cap as a Backup Power Source

Super caps are capacitors with extremely high capacitance values (e.g., order of 0.47F) for their size. Figure 15 shows two ways to use a super cap as a backup power source. The super cap can be connected through a diode to the 3V input (Figure 15a); or, if a 5V supply is also available, the super cap can be charged up to the 5V supply (Figure 15b), allowing a longer backup period. Since V_{BATT} can exceed V_{CC} while V_{CC} is above the reset threshold, there are no special precautions when using these μ P supervisors with a super cap.

Operation without a Backup Power Source

These μ P supervisors were designed for battery-backed applications. If a backup battery is not used, connect BATT, OUT, and V_{CC} together, or use a different μ P supervisor.

Replacing the Backup Battery

The backup power source can be removed while V_{CC} remains valid, without danger of triggering a reset pulse, provided that BATT is decoupled with a 0.1 μ F capacitor to ground. As long as V_{CC} stays above the reset threshold, battery-backup mode cannot be entered.

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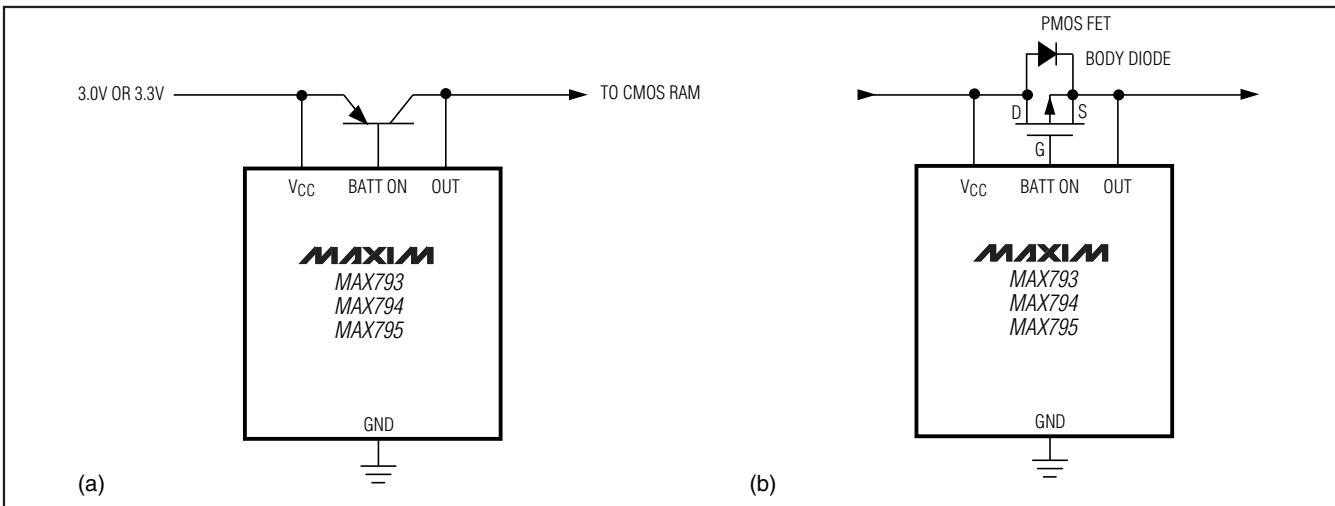


Figure 14. Driving an External Transistor with BATT ON

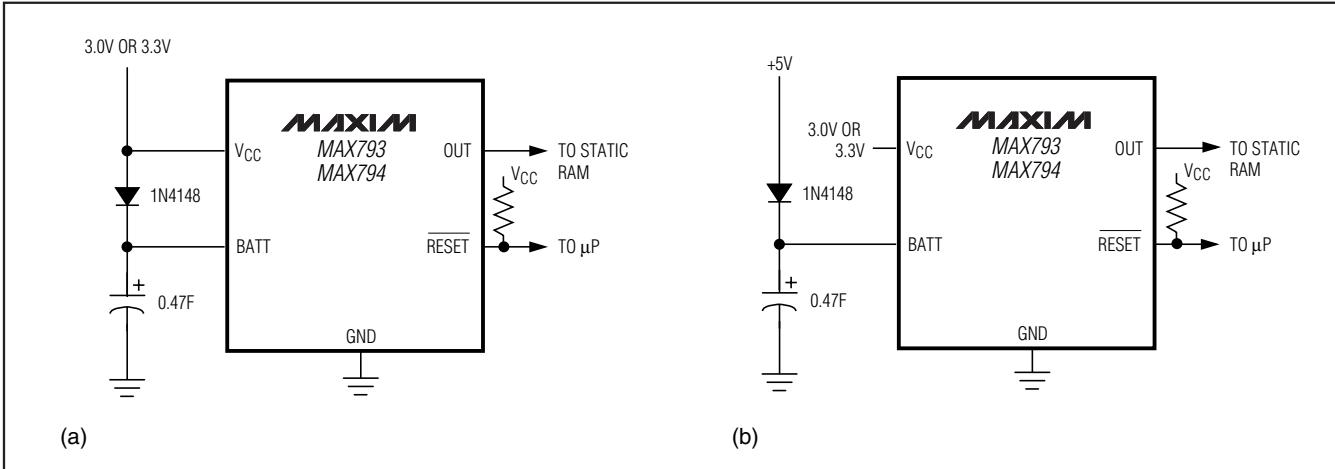


Figure 15. Using a Super Cap as a Backup Source

Adding Hysteresis to the Power-Fail Comparator (MAX793/MAX794)

The power-fail comparator has a typical input hysteresis of 10mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage divider (see the section *Monitoring an Additional Power Supply*).

If additional noise margin is desired, connect a resistor between PFO and PFI as shown in Figure 16a. Select the ratio of R1 and R2 such that PFI sees VPFT when V_{IN} falls to its trip point (V_{TRIP}). R3 adds the additional hysteresis and should typically be more than 10 times the value of R1 or R2. The hysteresis window extends

both above (V_H) and below (V_L) the original trip point (V_{TRIP}).

Connecting an ordinary signal diode in series with R3, as shown in Figure 16b, causes the lower trip point (V_L) to coincide with the trip point without hysteresis (V_{TRIP}), so the entire hysteresis window occurs above V_{TRIP} . This method provides additional noise margin without compromising the accuracy of the power-fail threshold when the monitored voltage is falling. It is useful for accurately detecting when a voltage falls past a threshold. The current through R1 and R2 should be at least $1\mu A$ to ensure that the $25nA$ (max over temperature) PFI input current does not shift the trip point. R3 should be larger than $82k\Omega$ so it does not load down the PFO pin. Capacitor C1 is optional, and adds noise rejection.

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MAX793/MAX794/MAX795

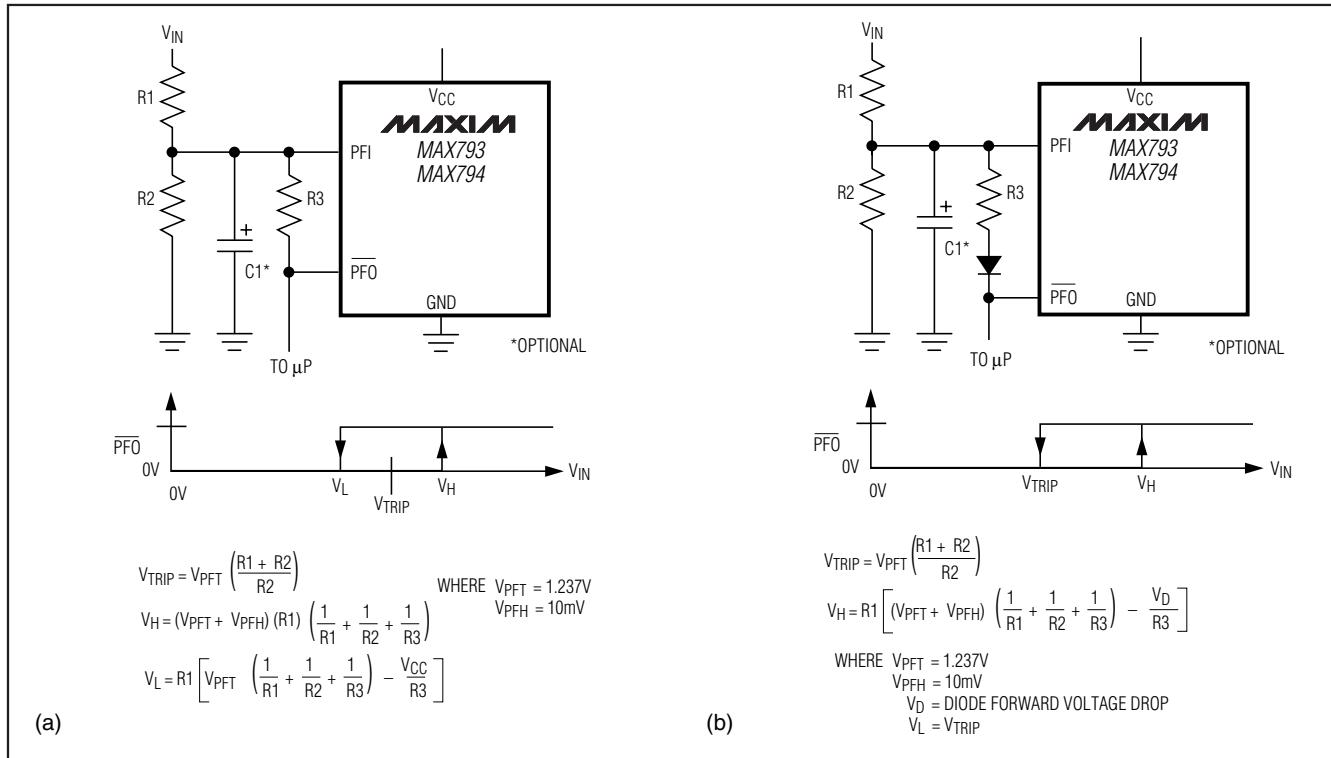


Figure 16. Adding Hysteresis to the Power-Fail Comparator: (a) Symmetrical Hysteresis, (b) Hysteresis Only on Rising V_{IN}

Monitoring an Additional Power Supply

These μ P supervisors can monitor either positive or negative supplies using a resistor voltage divider to PFI. PFO can be used to generate an interrupt to the μ P or to cause reset to assert (Figure 12).

Interfacing to μ Ps with Bidirectional Reset Pins

Since the $\overline{\text{RESET}}$ output is open drain, the MAX793/MAX794/MAX795 interface easily with μ Ps that have bidirectional reset pins, such as the Motorola 68HC11. Connecting the $\overline{\text{RESET}}$ output of the μ P supervisor directly to the $\overline{\text{RESET}}$ input of the microcontroller with a single pullup resistor allows either device to assert reset (Figure 17).

Negative-Going VCC Transients

These supervisors are relatively immune to short-duration negative-going V_{CC} transients (glitches) while issuing resets to the μ P during power-up, power-down, and brownout conditions. Therefore, resetting the μ P when V_{CC} experiences only small glitches is usually not recommended.

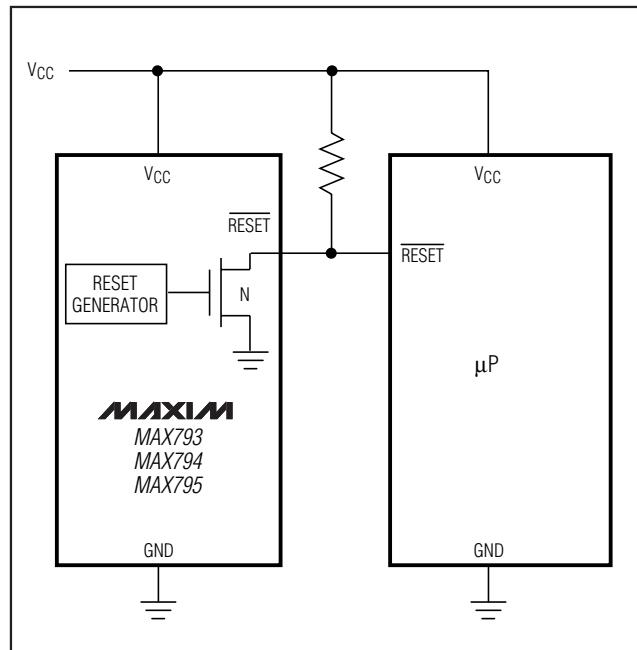


Figure 17. Interfacing to μ Ps with Bidirectional Reset I/O

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Figure 18 shows maximum transient duration vs. reset comparator overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going VCC pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going VCC transient can typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a VCC transient that goes 40mV below the reset threshold and lasts for 10µs or less does not cause a reset pulse to be issued.

A 0.1µF bypass capacitor mounted close to the VCC pin provides additional transient immunity.

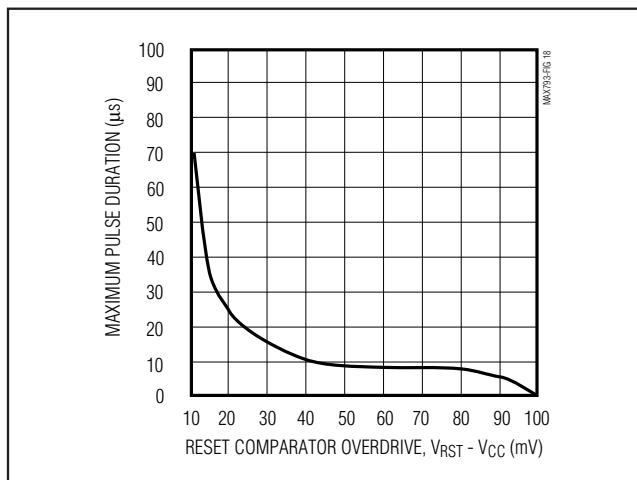


Figure 18. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

Watchdog Software Considerations

There is a way to help the watchdog timer monitor software execution more closely, which involves setting and resetting the watchdog input at different points in the program rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset within the loop, keeping the watchdog from timing out. Figure 19 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

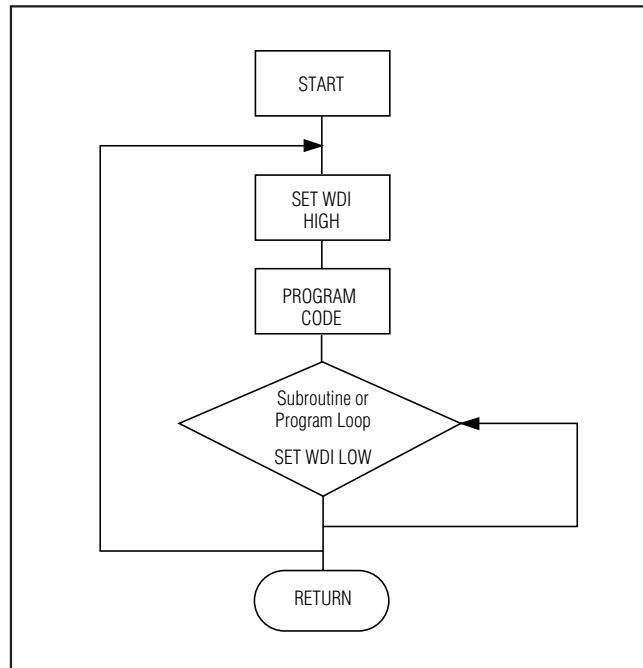


Figure 19. Watchdog Flow Diagram

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Ordering Information (continued)

PART*	TEMP RANGE	PIN-PACKAGE
MAX793_EPE	-40°C to +85°C	16 Plastic DIP
MAX793_ESE	-40°C to +85°C	16 Narrow SO
MAX794CPE	0°C to +70°C	16 Plastic DIP
MAX794CSE	0°C to +70°C	16 Narrow SO
MAX794EPE	-40°C to +85°C	16 Plastic DIP
MAX794ESE	-40°C to +85°C	16 Narrow SO
MAX795_CPA	0°C to +70°C	8 Plastic DIP
MAX795_CSA	0°C to +70°C	8 SO
MAX795_EPA	-40°C to +85°C	8 Plastic DIP
MAX795_ESA	-40°C to +85°C	8 SO

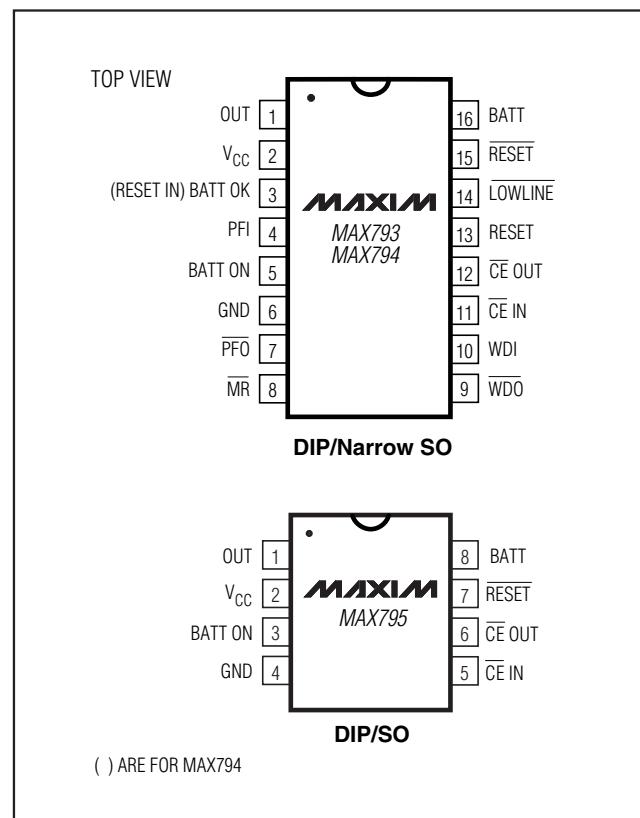
*The MAX793/MAX795 offer a choice of reset threshold voltage. Select the letter corresponding to the desired reset threshold voltage range ($T = 3.00V$ to $3.15V$, $S = 2.85V$ to $3.00V$, $R = 2.55V$ to $2.70V$) and insert it into the blank to complete the part number. The MAX794's reset threshold is adjustable.

Devices are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering.

Chip Information

TRANSISTOR COUNT: 1271

Pin Configurations



Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 SO	S8-2	21-0041
8 Plastic Dip	R8-1	21-0043
16 Plastic Dip	P16-1	21-0043
16 Narrow SO	S16-1	21-0041

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/95	Initial release	—
5	2/07	Revised <i>Electrical Characteristics</i> .	4
6	3/10	Revised <i>Absolute Maximum Ratings</i> and <i>Chip-Enable Input</i> section.	1, 2

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