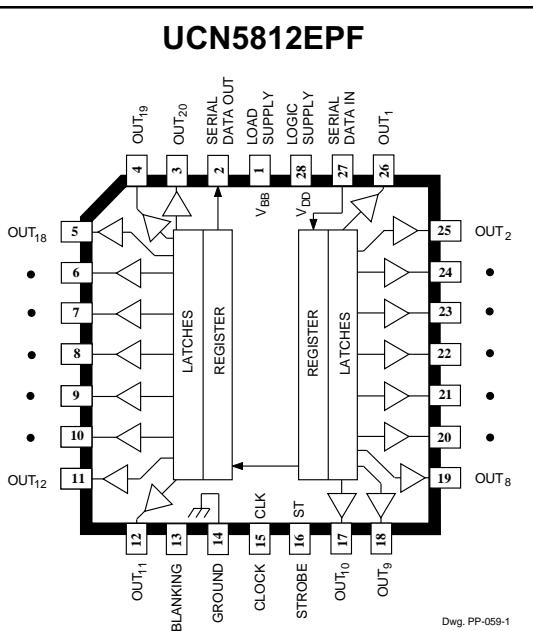


BiMOS II 20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS



ABSOLUTE MAXIMUM RATINGS

at $T_A = 25^\circ\text{C}$

| | |
|--|----------------------------|
| Logic Supply Voltage, V_{DD} | 15 V |
| Driver Supply Voltage, V_{BB} | 60 V |
| Continuous Output Current Range, I_{OUT} | -40 to +15 mA |
| Input Voltage Range, V_{IN} | -0.3 V to $V_{DD} + 0.3$ V |
| Package Power Dissipation, P_D | |
| (UCN5812AF) | 3.12 W* |
| (UCN5812EPF) | 1.84 W† |
| Operating Temperature Range, T_A | -20°C to +85°C |
| Storage Temperature Range, T_S | -55°C to +150°C |

* Derate at rate of 22 mW/°C above $T_A = +25^\circ\text{C}$

† Derate at rate of 15 mW/°C above $T_A = +25^\circ\text{C}$

Caution: Allegro CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Note that the UCN5812AF (dual in-line package) and UCN5812EPF (PLCC package) are electrically identical and share a common terminal number assignment.

The UCN5812AF/EPF combine a 20-bit CMOS shift register, data latches, and control circuitry with high-voltage bipolar source drivers and active DMOS pull-downs for reduced supply current requirements. Although designed primarily for vacuum-fluorescent displays, the high-voltage, high-current outputs also allow them to be used in other peripheral power driver applications. They are improved versions of the original UCN5812A/EP.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 5 V supply, they will operate to at least 3.3 MHz. At 12 V, higher speeds are possible. Especially useful for inter-digit blanking, the BLANKING input disables the output source drives and turns on the DMOS sink drivers. Use with TTL may require the use of appropriate pull-up resistors to ensure an input logic high.

A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Similar devices are available as the UCN5810AF/LWF (10 bits), UCN5811A (12 bits), and UCN5818AF/EPF (32 bits).

The output source drivers are high-voltage pnp-npn Darlingtons with a minimum breakdown of 60 V and are capable of sourcing up to 40 mA. The DMOS active pull-downs are capable of sinking up to 15 mA.

The UCN5812AF is supplied in a 28-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. For surface mounting, the UCN5812EPF is furnished in 28-lead plastic chip carrier (quad pack) with 0.050" (1.22 mm) centers. Copper lead-frames, reduced supply current requirements and lower output saturation voltages, allow continuous operation, with all outputs sourcing 25 mA, of the UCN5812AF over the operating temperature range, and the UCN5812EPF up to +75°C. All devices are also available for operation between -40°C and +85°C. To order, change the prefix from 'UCN' to 'UCQ'.

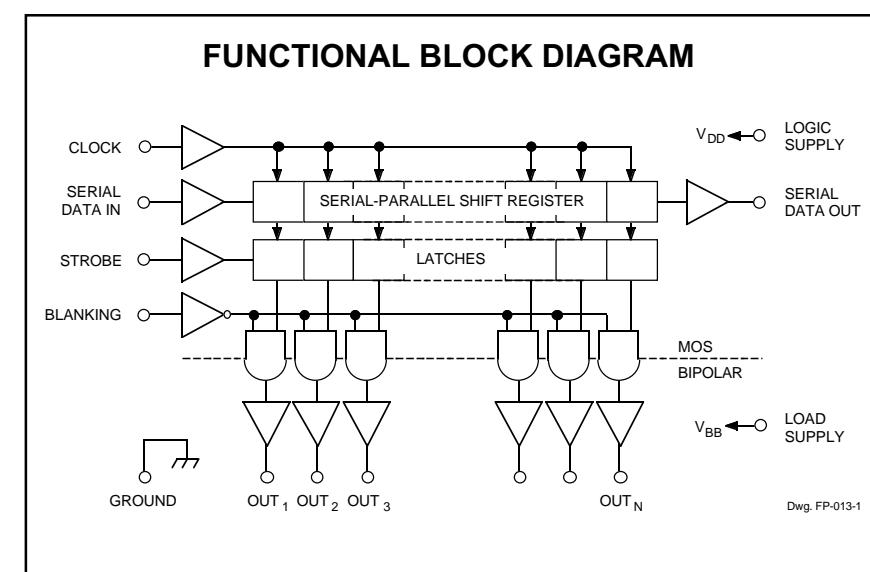
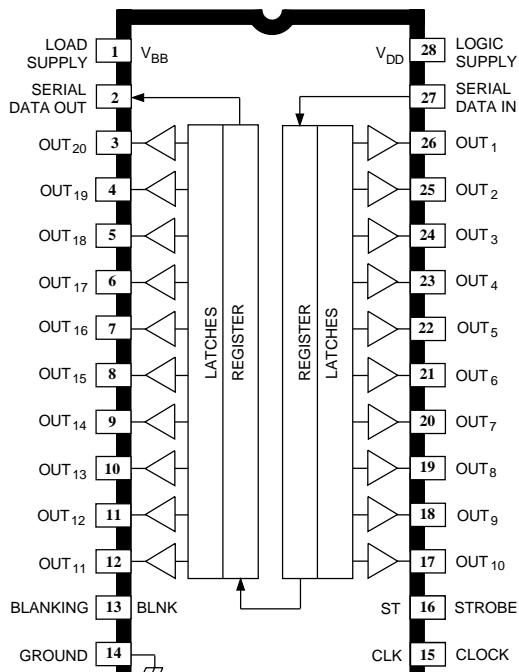
FEATURES

- High-Speed Source Drivers
- 60 V Source Outputs
- To 3.3 MHz Data Input Rate
- Low Output-Saturation Voltages
- Low-Power CMOS Logic and Latches
- Active DMOS Pull-Downs
- Reduced Supply Current Requirements
- Improved Replacement for TL5812

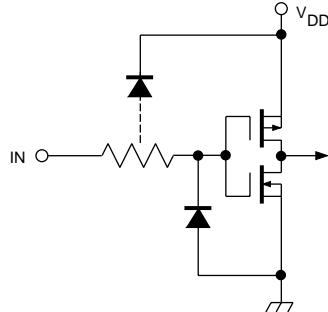
Always order by complete part number, e.g., **UCN5812AF**.

5812-F
20-BIT SERIAL-INPUT,
LATCHED SOURCE DRIVERS
WITH ACTIVE-DMOS PULL-DOWNS

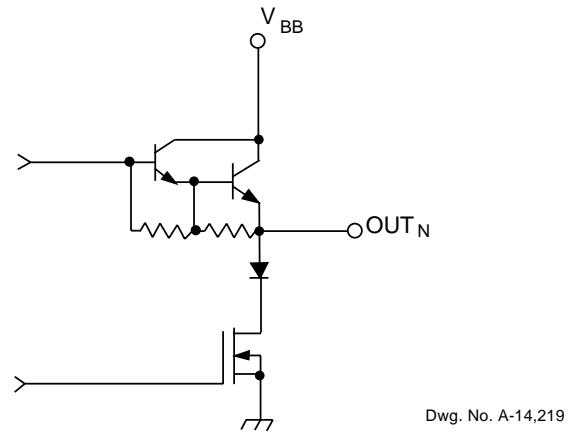
UCN5812AF



TYPICAL INPUT CIRCUIT



TYPICAL OUTPUT DRIVER



5812-F
20-BIT SERIAL-INPUT,
LATCHED SOURCE DRIVERS
WITH ACTIVE-DMOS PULL-DOWNS

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $V_{BB} = 60\text{ V}$ (unless otherwise noted).

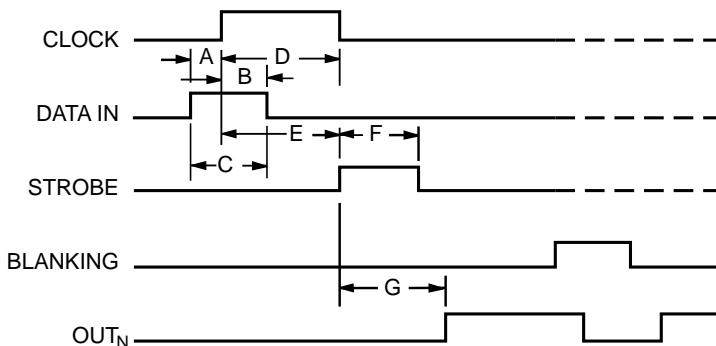
| Characteristic | Symbol | Test Conditions | Limits @ $V_{DD} = 5\text{ V}$ | | | Limits @ $V_{DD} = 12\text{ V}$ | | | Units |
|--------------------------|--------------|--|--------------------------------|-------|------|---------------------------------|------|------|---------------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Output Leakage Current | I_{CEX} | $V_{OUT} = 0\text{ V}$, $T_A = +70^\circ\text{C}$ | — | -5.0 | -15 | — | -5.0 | -15 | μA |
| Output Voltage | $V_{OUT(1)}$ | $I_{OUT} = -25\text{ mA}$, $V_{BB} = 60\text{ V}$ | 58 | 58.5 | — | 58 | 58.5 | — | V |
| | $V_{OUT(0)}$ | $I_{OUT} = 1\text{ mA}$ | — | 2.0 | 3.0 | — | — | — | V |
| | | $I_{OUT} = 2\text{ mA}$ | — | — | — | — | 2.0 | 3.5 | V |
| Output Pull-Down Current | $I_{OUT(0)}$ | $V_{OUT} = 5\text{ V}$ to V_{BB} | 2.0 | 3.5 | — | — | — | — | mA |
| | | $V_{OUT} = 20\text{ V}$ to V_{BB} | — | — | — | 8.0 | 13 | — | mA |
| Input Voltage | $V_{IN(1)}$ | | 3.5 | — | 5.3 | 10.5 | — | 12.3 | V |
| | $V_{IN(0)}$ | | -0.3 | — | +0.8 | -0.3 | — | +0.8 | V |
| Input Current | $I_{IN(1)}$ | $V_{IN} = V_{DD}$ | — | 0.05 | 0.5 | — | 0.1 | 1.0 | μA |
| | $I_{IN(0)}$ | $V_{IN} = 0.8\text{ V}$ | — | -0.05 | -0.5 | — | -0.1 | -1.0 | μA |
| Serial Data | $V_{OUT(1)}$ | $I_{OUT} = -200\text{ }\mu\text{A}$ | 4.5 | 4.7 | — | 11.7 | 11.8 | — | V |
| | $V_{OUT(0)}$ | $I_{OUT} = 200\text{ }\mu\text{A}$ | — | 200 | 250 | — | 100 | 200 | mV |
| Maximum Clock Frequency | f_{clk} | | 3.3* | — | — | — | — | — | MHz |
| Supply Current | $I_{DD(1)}$ | All Outputs High | — | 100 | 300 | — | 200 | 500 | μA |
| | $I_{DD(0)}$ | All Outputs Low | — | 100 | 300 | — | 200 | 500 | μA |
| | $I_{BB(1)}$ | Outputs High, No Load | — | 1.5 | 4.0 | — | 1.5 | 4.0 | mA |
| | $I_{BB(0)}$ | Outputs Low | — | 10 | 100 | — | 10 | 100 | μA |
| Blanking to Output Delay | t_{PHL} | $C_L = 30\text{ pF}$, 50% to 50% | — | 2000 | — | — | 1000 | — | ns |
| | t_{PLH} | $C_L = 30\text{ pF}$, 50% to 50% | — | 1000 | — | — | 850 | — | ns |
| Output Fall Time | t_f | $C_L = 30\text{ pF}$, 90% to 10% | — | 1450 | — | — | 650 | — | ns |
| Output Rise Time | t_r | $C_L = 30\text{ pF}$, 10% to 90% | — | 650 | — | — | 700 | — | ns |

Negative current is defined as coming out of (sourcing) the specified device pin.

* Operation at a clock frequency greater than the specified minimum value is possible but not warranted.

5812-F

20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS



Dwg. No. 12,649A

TIMING REQUIREMENTS

($T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, Logic Levels are V_{DD} and Ground)

| | |
|--|--------|
| A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) | 75 ns |
| B. Minimum Data Active Time After Clock Pulse (Data Hold Time) | 75 ns |
| C. Minimum Data Pulse Width | 150 ns |
| D. Minimum Clock Pulse Width | 150 ns |
| E. Minimum Time Between Clock Activation and Strobe | 300 ns |
| F. Minimum Strobe Pulse Width | 100 ns |
| G. Typical Time Between Strobe Activation and Output Transition | 500 ns |

Timing is representative of a 3.3 MHz clock. Higher speeds may be attainable with increased supply voltage; operation at high temperatures will reduce the specified maximum clock frequency.

TRUTH TABLE

| Serial Data Input | Clock Input | Shift Register Contents | | | | | Serial Data Output | Strobe Input | Latch Contents | | | | | Blanking | Output Contents | | | | | | | |
|-------------------------|----------------|-------------------------|----------------|----------------|-----|------------------|--------------------------|------------------|----------------|----------------|----------------|----------------|------------------|------------------|-----------------|----------------|----------------|----------------|------------------|----------------|------------------|----------------|
| | | I ₁ | I ₂ | I ₃ | ... | I _{N-1} | I _N | | I ₁ | I ₂ | I ₃ | ... | I _{N-1} | I _N | I ₁ | I ₂ | I ₃ | ... | I _{N-1} | I _N | | |
| H | ⊤ | H | R ₁ | R ₂ | ... | R _{N-2} | R _{N-1} | R _{N-1} | | | | | | | | | | | | | | |
| L | ⊤ | L | R ₁ | R ₂ | ... | R _{N-2} | R _{N-1} | R _{N-1} | | | | | | | | | | | | | | |
| X | ⊤ | R ₁ | R ₂ | R ₃ | ... | R _{N-1} | R _N | R _N | | | | | | | | | | | | | | |
| | | X | X | X | ... | X | X | X | L | R ₁ | R ₂ | R ₃ | ... | R _{N-1} | R _N | | | | | | | |
| | | P ₁ | P ₂ | P ₃ | ... | P _{N-1} | P _N | P _N | H | P ₁ | P ₂ | P ₃ | ... | P _{N-1} | P _N | L | P ₁ | P ₂ | P ₃ | ... | P _{N-1} | P _N |
| | | | | | | | | | | X | X | X | ... | X | X | H | L | L | L | ... | L | L |

L = Low Logic Level H = High Logic Level X = Irrelevant

P = Present State R = Previous State

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

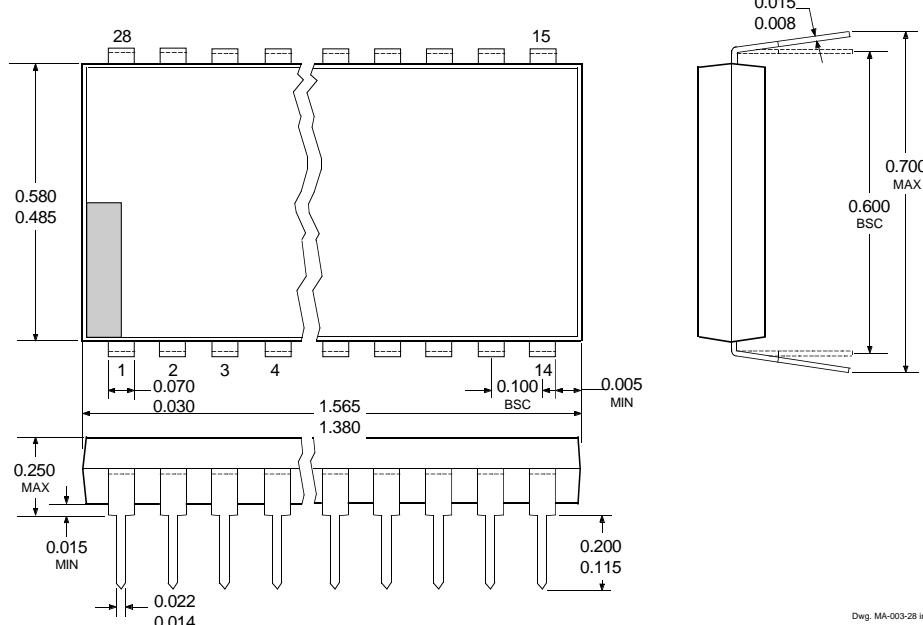
Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON, the information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

5812-F
20-BIT SERIAL-INPUT,
LATCHED SOURCE DRIVERS
WITH ACTIVE-DMOS PULL-DOWNS

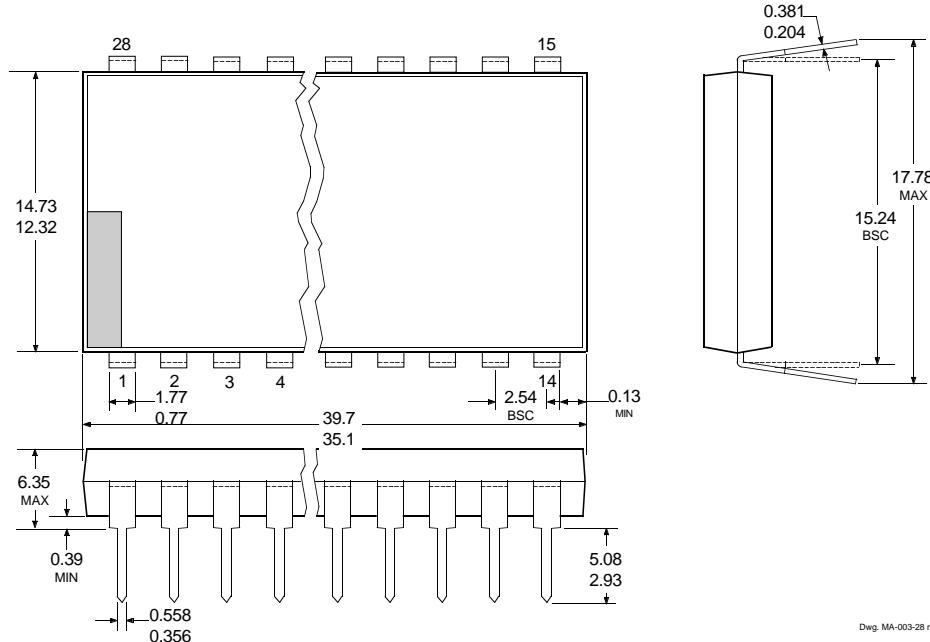
UCN5812AF

Dimensions in Inches
 (controlling dimensions)



Dwg. MA-003-28 in

Dimensions in Millimeters
 (for reference only)



Dwg. MA-003-28 mm

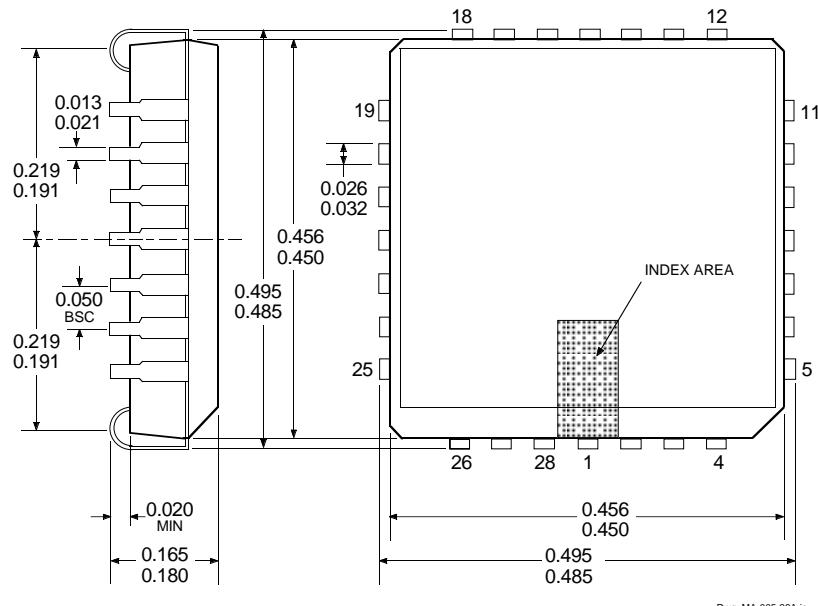
NOTES:

1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.
4. Supplied in standard sticks/tubes of 12 devices.

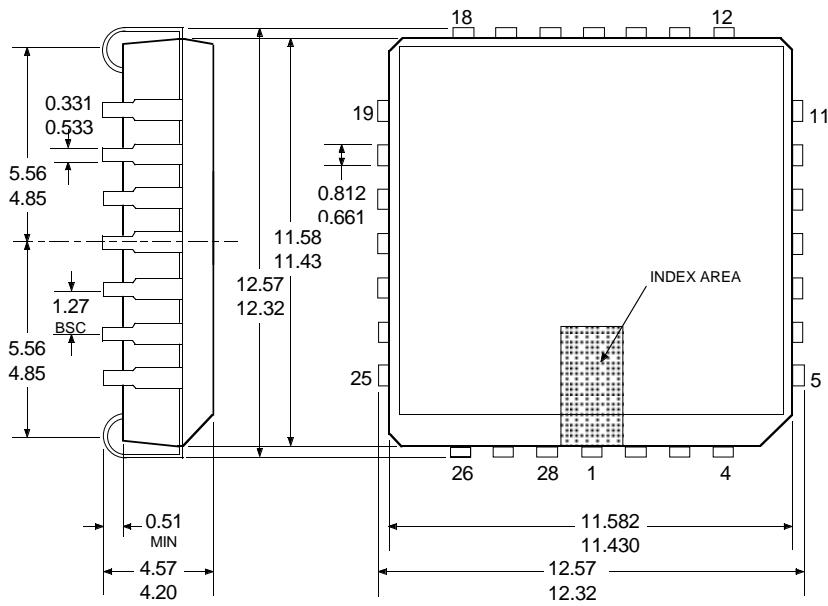
5812-F
20-BIT SERIAL-INPUT,
LATCHED SOURCE DRIVERS
WITH ACTIVE-DMOS PULL-DOWNS

UCN5812EPF

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters (for reference only)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 38 devices or add "TR" to part number for tape and reel.

5812-F
20-BIT SERIAL-INPUT,
LATCHED SOURCE DRIVERS
WITH ACTIVE-DMOS PULL-DOWNS

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5812-F
**20-BIT SERIAL-INPUT,
LATCHED SOURCE DRIVERS
WITH ACTIVE-DMOS PULL-DOWNS**

**POWER
*INTERFACE DRIVERS***

| Function | Output Ratings* | | Part Number† |
|--|-----------------|-------|-----------------|
| SERIAL-INPUT LATCHED DRIVERS | | | |
| 8-Bit (saturated drivers) | -120 mA | 50 V‡ | 5895 |
| 8-Bit | 350 mA | 50 V | 5821 |
| 8-Bit | 350 mA | 80 V | 5822 |
| 8-Bit | 350 mA | 50 V‡ | 5841 |
| 8-Bit | 350 mA | 80 V‡ | 5842 |
| 8-Bit (constant-current LED driver) | 75 mA | 17 V | 6275 |
| 8-Bit (constant-current LED driver) | 120 mA | 24 V | 6277 |
| 8-Bit (DMOS drivers) | 250 mA | 50 V | 6595 |
| 8-Bit (DMOS drivers) | 350 mA | 50 V‡ | 6A595 |
| 8-Bit (DMOS drivers) | 100 mA | 50 V | 6B595 |
| 10-Bit (active pull-downs) | -25 mA | 60 V | 5810-F and 6810 |
| 12-Bit (active pull-downs) | -25 mA | 60 V | 5811 |
| 16-Bit (constant-current LED driver) | 75 mA | 17 V | 6276 |
| 20-Bit (active pull-downs) | -25 mA | 60 V | 5812-F and 6812 |
| 32-Bit (active pull-downs) | -25 mA | 60 V | 5818-F and 6818 |
| 32-Bit | 100 mA | 30 V | 5833 |
| 32-Bit (saturated drivers) | 100 mA | 40 V | 5832 |
| PARALLEL-INPUT LATCHED DRIVERS | | | |
| 4-Bit | 350 mA | 50 V‡ | 5800 |
| 8-Bit | -25 mA | 60 V | 5815 |
| 8-Bit | 350 mA | 50 V‡ | 5801 |
| 8-Bit (DMOS drivers) | 100 mA | 50 V | 6B273 |
| 8-Bit (DMOS drivers) | 250 mA | 50 V | 6273 |
| SPECIAL-PURPOSE DEVICES | | | |
| Unipolar Stepper Motor Translator/Driver | 1.25 A | 50 V‡ | 5804 |
| Addressable 8-Bit Decoder/DMOS Driver | 250 mA | 50 V | 6259 |
| Addressable 8-Bit Decoder/DMOS Driver | 350 mA | 50 V‡ | 6A259 |
| Addressable 8-Bit Decoder/DMOS Driver | 100 mA | 50 V | 6B259 |
| Addressable 28-Line Decoder/Driver | 450 mA | 30 V | 6817 |

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits.
 Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.