



PRELIMINARY

CY7C1011

128K x 16 Static RAM

Features

- **High speed**
— $t_{AA} = 15 \text{ ns}$
- **Low active power**
— 1150 mW (max.)
- **Low CMOS standby power (L version)**
— 40 mW (max.)
- **2.0V Data Retention (4 mW at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**

Functional Description

The CY7C1011 is a high-performance CMOS static RAM organized as 131,072 words by 16 bits.

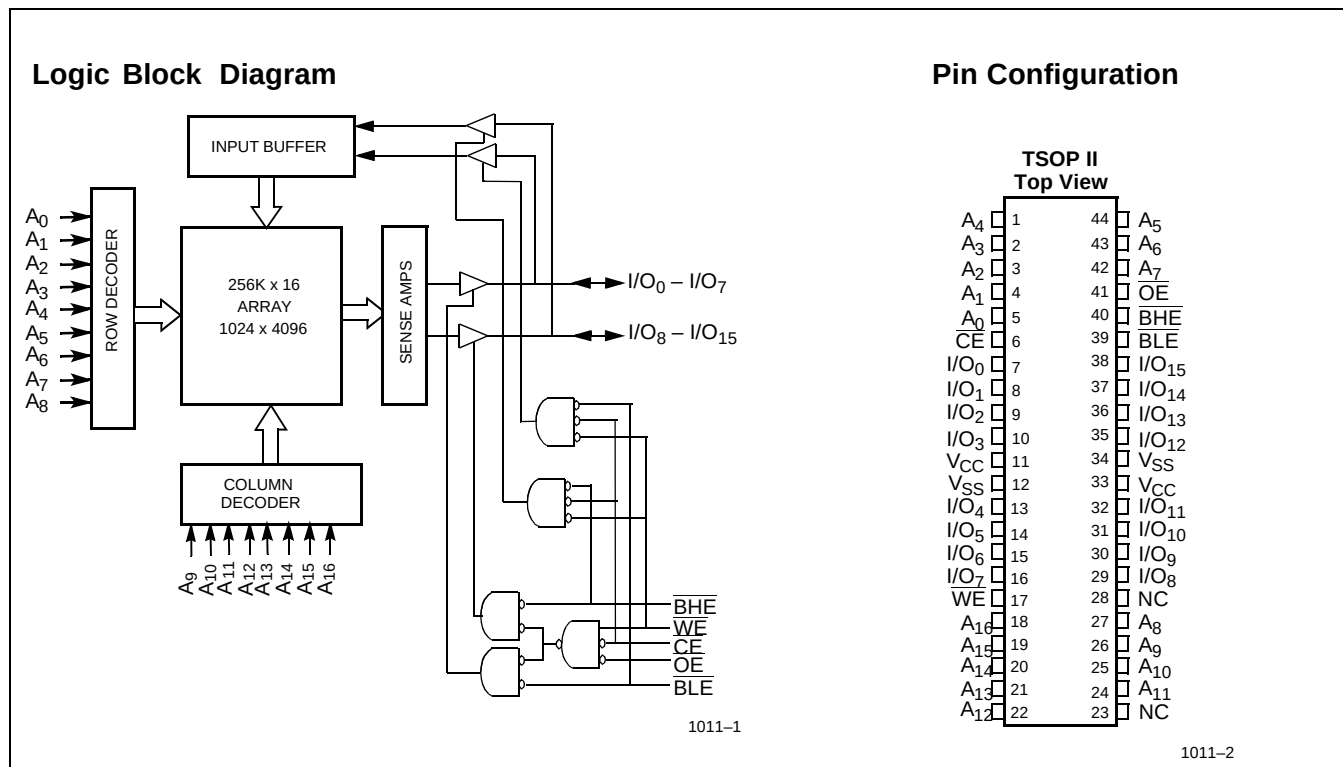
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. If byte low enable

($\overline{BLE}$) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₆). If byte high enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₆).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing the write enable ($\overline{WE}$) HIGH. If byte low enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If byte high enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this datasheet for a complete description of read and write modes.

The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1011 is available in a standard 44-pin TSOP II package with center power and ground (revolutionary) pinout.



Selection Guide

	7C1011-15	7C1011-20	7C1011-25
Maximum Access Time (ns)	15	20	25
Maximum Operating Current (mA)	230	220	200
Maximum CMOS Standby Current (mA)	Com'l	8	8

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to +70°C	5V $\pm$ 0.5

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1011-15		7C1011-20		7C1011-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$, Output Disabled	-1	+1	-1	+1	-1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}$, $f = f_{MAX} = 1/t_{RC}$		230		220		200	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		40		40		40	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f=0$	Com'l	8		8		8	mA

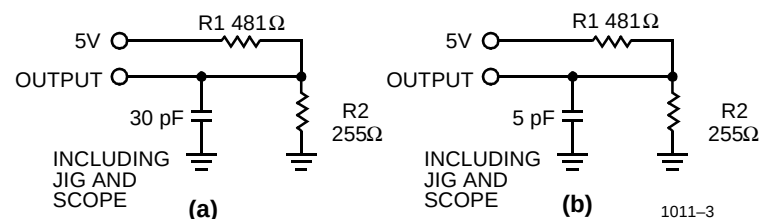
Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 5.0V$	8	pF
C_{OUT}	I/O Capacitance		8	pF

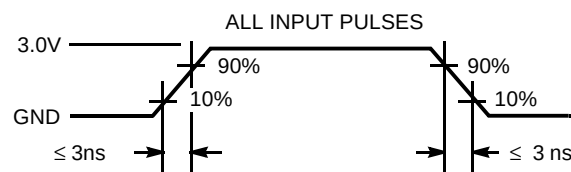
Notes:

- $V_{IL}(\text{min.}) = -2.0V$ for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT
 167Ω
 OUTPUT $\rightarrow$ $1.73V$



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Switching Characteristics^[4] Over the Operating Range

Parameter	Description	7C1011-15		7C1011-20		7C1011-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	15		20		25		ns
t _{AA}	Address to Data Valid		15		20		25	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		7		8		10	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[5]	0		0		0		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[5, 6]		7		8		10	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[5]	3		3		5		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[5, 6]		7		8		10	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		25	ns
t _{DBE}	Byte Enable to Data Valid		7		8		10	ns
t _{LZBE}	Byte Enable to Low Z	0		0		0		ns
t _{HZBE}	Byte Disable to High Z		7		8		10	ns
WRITE CYCLE ^[7,8]								
t _{WC}	Write Cycle Time	15		20		25		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	12		13		15		ns
t _{AW}	Address Set-Up to Write End	12		13		15		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	12		13		15		ns
t _{SD}	Data Set-Up to Write End	8		9		10		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[5]	3		3		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[5, 6]		7		8		10	ns
t _{BW}	Byte Enable to End of Write	12		13		15		ns

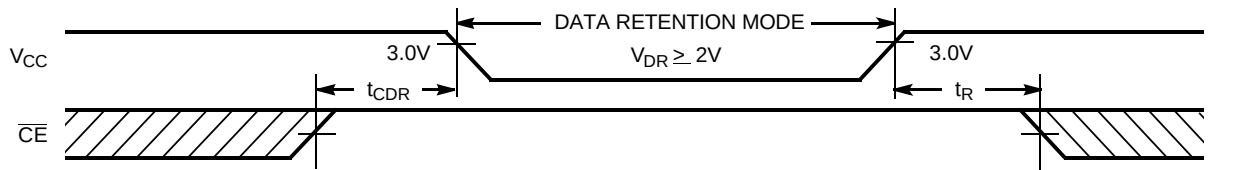
Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics Over the Operating Range

Parameter	Description		Conditions ^[10]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	Com'I	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		2	mA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time			0		ns
$t_R^{[9]}$	Operation Recovery Time			t_{RC}		ns

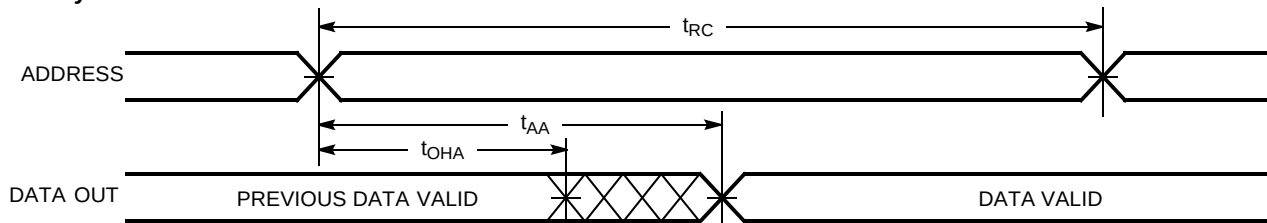
Data Retention Waveform



1011-5

Switching Waveforms

Read Cycle No. 1 ^[11, 12]



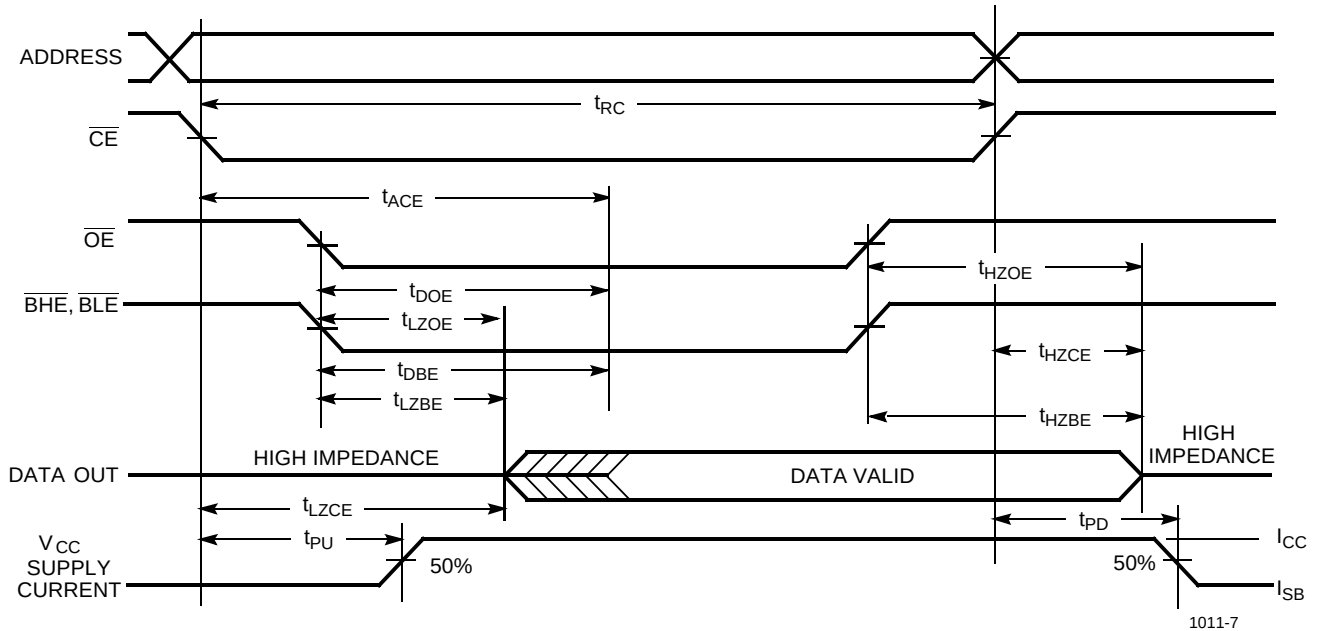
1011-6

Notes:

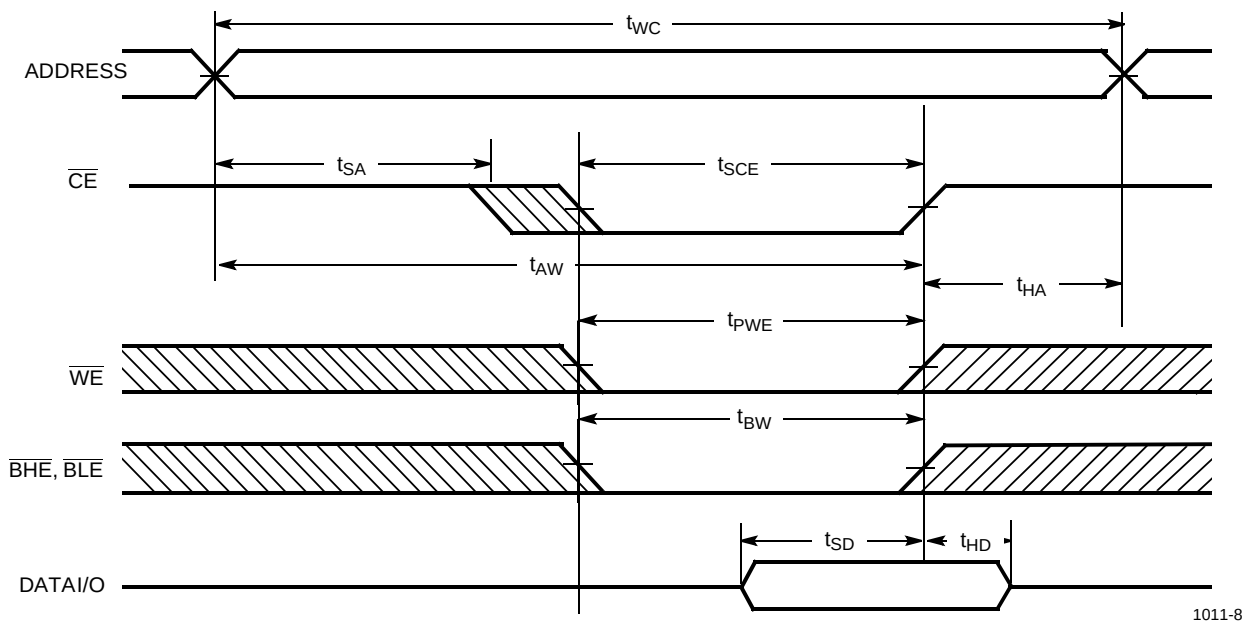
9. $t_r \leq 3$ ns for the -12 and -15 speeds. $t_r \leq 5$ ns for the -20 and slower speeds.
10. No input may exceed $V_{CC} + 0.5V$.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and/or $\overline{BHE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ($\overline{OE}$ Controlled) [12, 13]



Write Cycle No. 1 ($\overline{CE}$ Controlled) [14, 15]

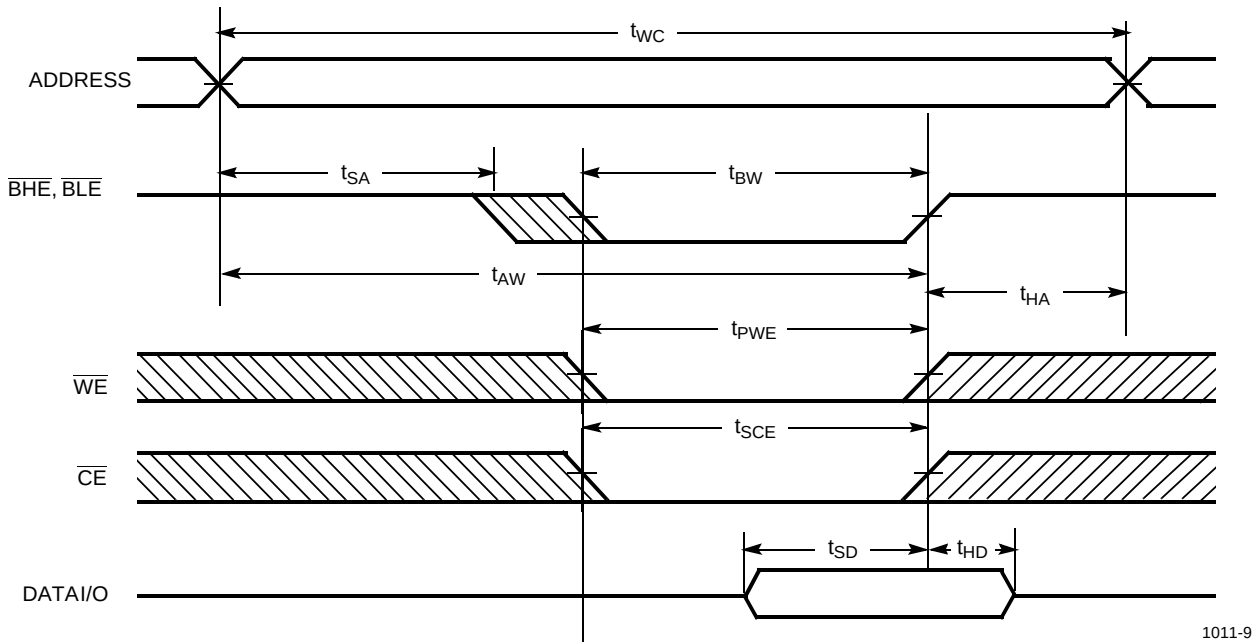


Notes:

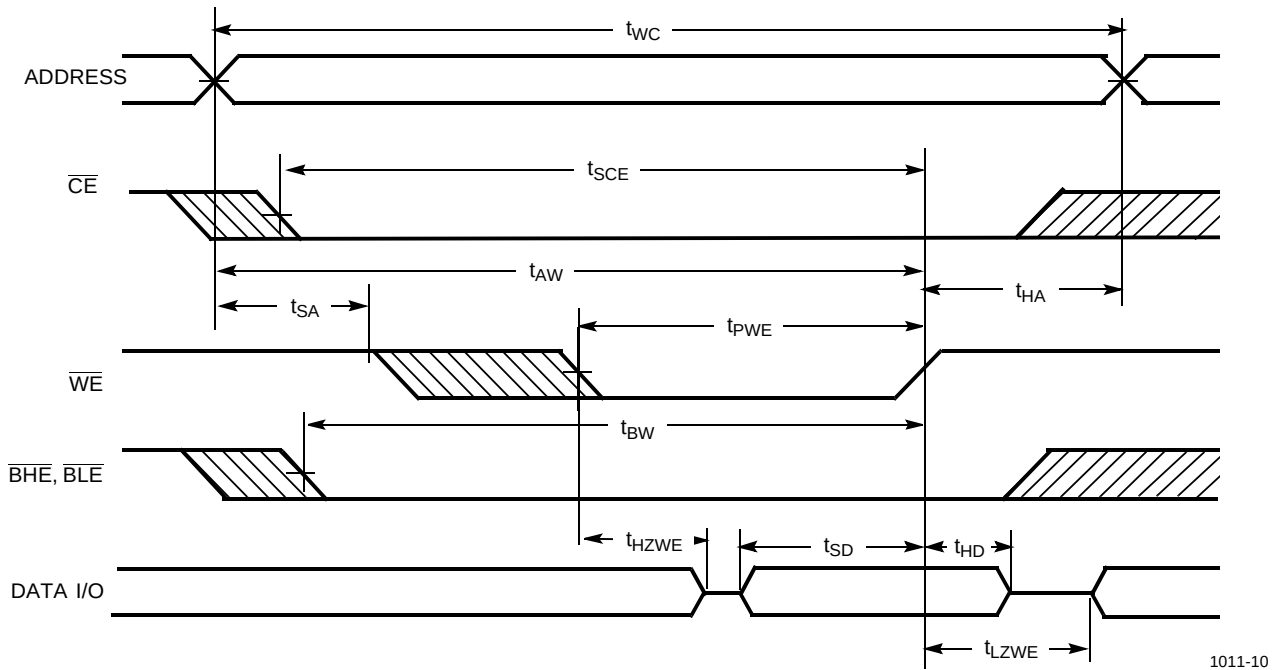
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE} = V_{IH}$.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



Write Cycle No.3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)



Truth Table

CE	OE	WE	BLE	BHE	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I _{SB})
L	L	H	L	L	Data Out	Data Out	Read All bits	Active (I _{CC})
L	L	H	L	H	Data Out	High Z	Read Lower bits only	Active (I _{CC})
L	L	H	H	L	High Z	Data Out	Read Upper bits only	Active (I _{CC})
L	X	L	L	L	Data In	Data In	Write All bits	Active (I _{CC})
L	X	L	L	H	Data In	High Z	Write Lower bits only	Active (I _{CC})
L	X	L	H	L	High Z	Data In	Write Upper bits only	Active (I _{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})

Ordering Information

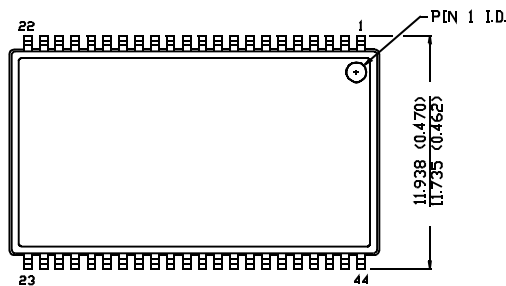
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1011-15VC	Z44	44-Lead TSOP Type II	Commercial
20	CY7C1011-20VC	Z44	44-Lead TSOP Type II	
25	CY7C1011-25ZC	Z44	44-Lead TSOP Type II	

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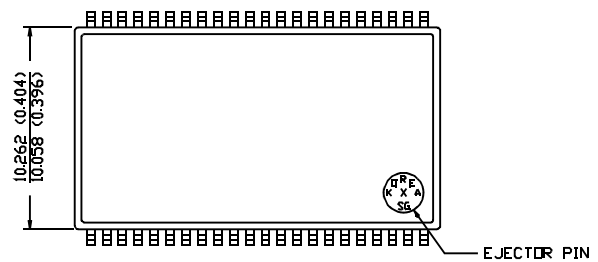
Package Diagram

44-Pin TSOP II Z44

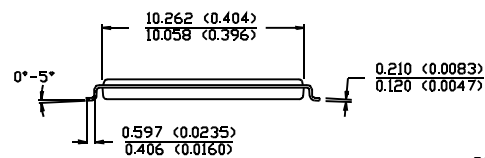
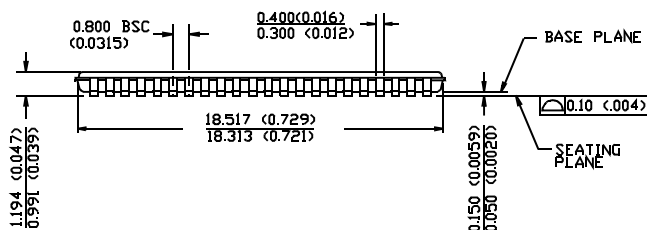
DIMENSION IN MM (INCH)
MAX
MIN



TOP VIEW



BOTTOM VIEW



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