



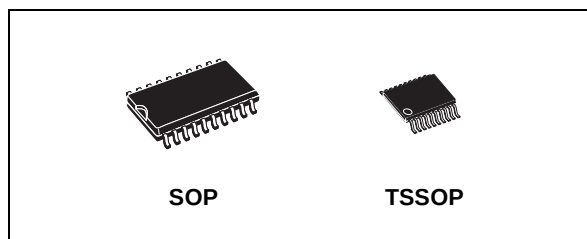
74VHC245

OCTAL BUS TRANSCEIVER (3-STATE)

- HIGH SPEED: $t_{PD} = 4.0 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu A$ (MAX.) at $T_A = 25^\circ C$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- POWER DOWN PROTECTION ON CONTROL INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(\text{OPR}) = 2V \text{ to } 5.5V$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 245
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP} = 0.9V$ (MAX.)

DESCRIPTION

The 74VHC245 is an advanced high-speed CMOS OCTAL BUS TRANSCEIVER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. This IC is intended for two-way asynchronous communication between data busses; the



ORDER CODES

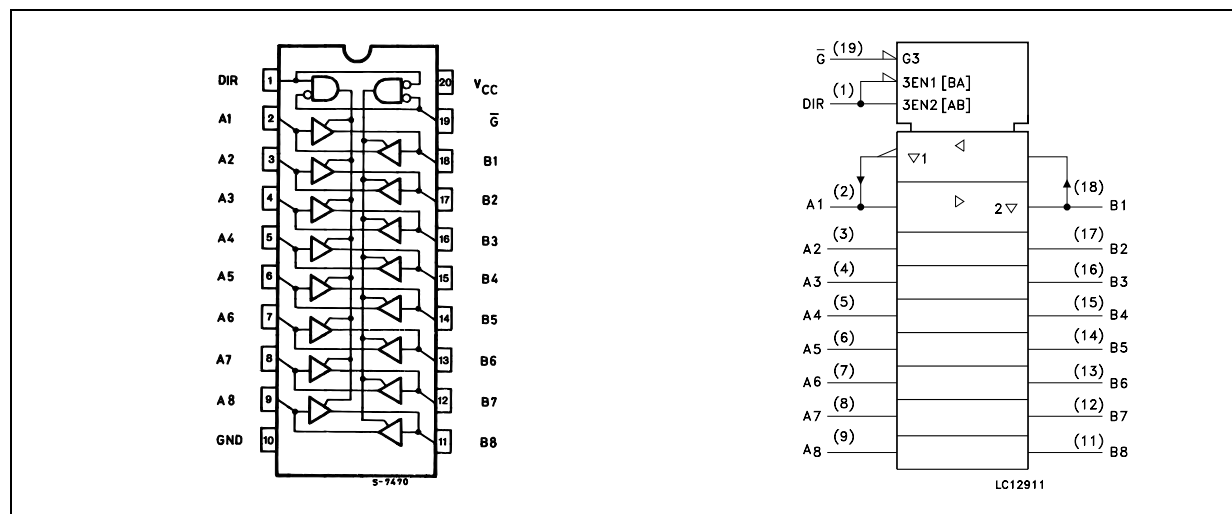
PACKAGE	TUBE	T & R
SOP	74VHC245M	74VHC245MTR
TSSOP		74VHC245TTR

direction of data transmission is determined by DIR input. The enable input $\bar{G}$ can be used to disable the device so that the busses are effectively isolated.

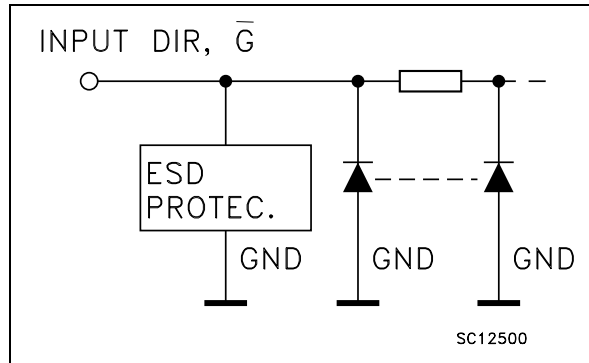
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

All floating bus terminals during High Z State must be held HIGH or LOW.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	DIR	Directional Control
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs/Outputs
18, 17, 16, 15, 14, 13, 12, 11	B1 to B8	Data Inputs/Outputs
19	$\overline{G}$	Output Enable Input
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS		FUNCTION		OUTPUT
$\overline{G}$	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	Z	Z	Z

X : Don't Care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage (DIR, $\overline{G}$)	-0.5 to +7.0	V
V _{I/O}	Bus I/O Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	- 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 75	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2 to 5.5	V
V _I	Input Voltage (DIR, $\overline{G}$)	0 to 5.5	V
V _{I/O}	Bus I/O Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 1) (V _{CC} = 3.3 ± 0.3V) (V _{CC} = 5.0 ± 0.5V)	0 to 100 0 to 20	ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value								Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V	
		3.0 to 5.5		0.7V _{CC}			0.7V _{CC}		0.7V _{CC}			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		3.0 to 5.5				0.3V _{CC}		0.3V _{CC}		0.3V _{CC}		
V _{OH}	High Level Output Voltage	2.0	I _O =-50 μA	1.9	2.0		1.9		1.9		V	
		3.0	I _O =-50 μA	2.9	3.0		2.9		2.9			
		4.5	I _O =-50 μA	4.4	4.5		4.4		4.4			
		3.0	I _O =-4 mA	2.58			2.48		2.4			
		4.5	I _O =-8 mA	3.94			3.8		3.7			
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1		0.1	V	
		3.0	I _O =50 μA		0.0	0.1		0.1		0.1		
		4.5	I _O =50 μA		0.0	0.1		0.1		0.1		
		3.0	I _O =4 mA			0.36		0.44		0.55		
		4.5	I _O =8 mA			0.36		0.44		0.55		
I _{OZ}	High Impedance Output Leakage Current	5.5	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.25		± 2.5		± 2.5	μA	
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			± 0.1		± 1		± 1	μA	
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40		40	μA	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

Symbol	Parameter	Test Condition			Value						Unit	
		V _{CC} (V)	C _L (pF)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time	3.3 ^(*)	15			5.8	8.4	1.0	10.0	1.0	10.0	ns
		3.3 ^(*)	50			8.3	11.9	1.0	13.5	1.0	13.5	
		5.0 ^(**)	15			4.0	5.5	1.0	6.5	1.0	6.5	
		5.0 ^(**)	50			5.5	7.5	1.0	8.5	1.0	8.5	
t _{PZL} t _{PZH}	Output Disable Time	3.3 ^(*)	15	R _L = 1KΩ		8.5	13.2	1.0	15.5	1.0	15.5	ns
		3.3 ^(*)	50	R _L = 1KΩ		11.0	16.7	1.0	19.0	1.0	19.0	
		5.0 ^(**)	15	R _L = 1KΩ		5.8	8.5	1.0	10.0	1.0	10.0	
		5.0 ^(**)	50	R _L = 1KΩ		7.3	10.6	1.0	12.0	1.0	12.0	
t _{PLZ} t _{PHZ}	Output Enable Time	3.3 ^(*)	50	R _L = 1KΩ		11.5	15.8	1.0	18.0	1.0	18.0	ns
		5.0 ^(**)	50	R _L = 1KΩ		7.0	9.7	1.0	11.0	1.0	11.0	
t _{OSLH} t _{OSHL}	Output to Output Skew time (note 1)	3.3 ^(*)	50				1.5		1.5		1.5	ns
		5.0 ^(**)	50				1.0		1.0		1.0	

(*) Voltage range is $3.3\text{V} \pm 0.3\text{V}$ (**) Voltage range is $5.0\text{V} \pm 0.5\text{V}$ Note 1 : Parameter guaranteed by design. $t_{soLH} = |t_{pLHm} - t_{pLHn}|$, $t_{soHL} = |t_{pHLm} - t_{pHLn}|$ **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Condition	Value								Unit
			T _A = 25°C			-40 to 85°C		-55 to 125°C			
			Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
C _{IN}	Input Capacitance			4	10		10		10	pF	
C _{I/O}	Output Capacitance			8						pF	
C _{PD}	Power Dissipation Capacitance (note 1)			21						pF	

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per circuit)

DYNAMIC SWITCHING CHARACTERISTICS

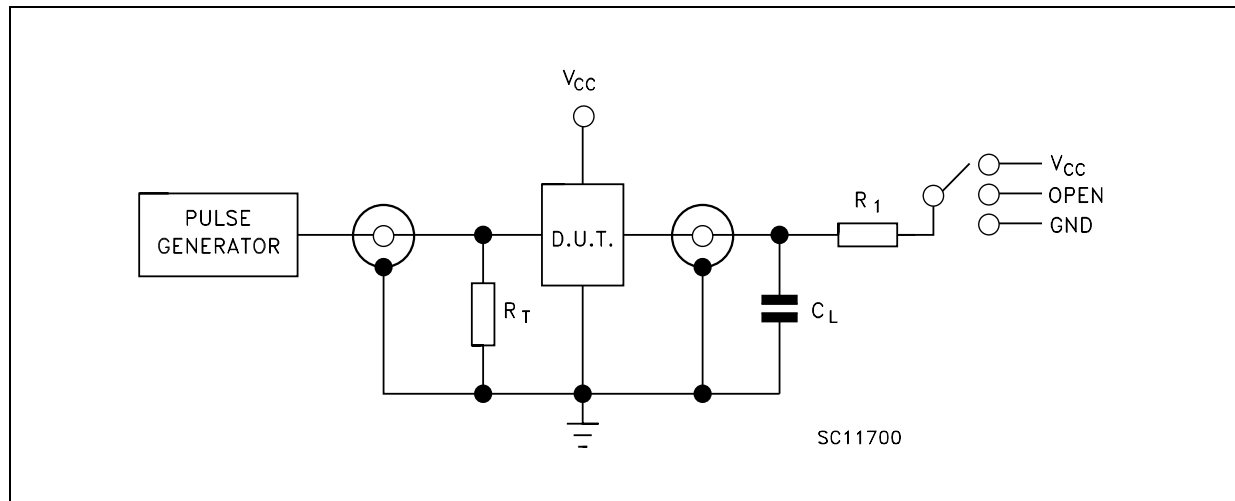
Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C _L = 50 pF		0.6	0.9					V
V _{OLV}				-0.9	-0.6						
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	5.0		3.5							V
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	5.0					1.5				

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

TEST CIRCUIT

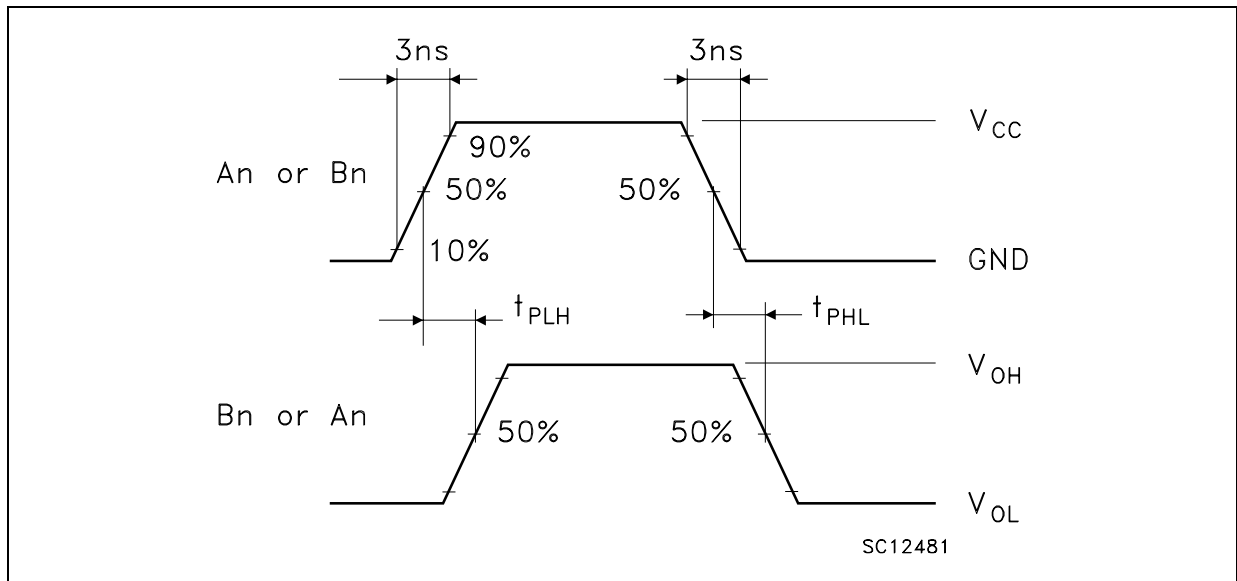
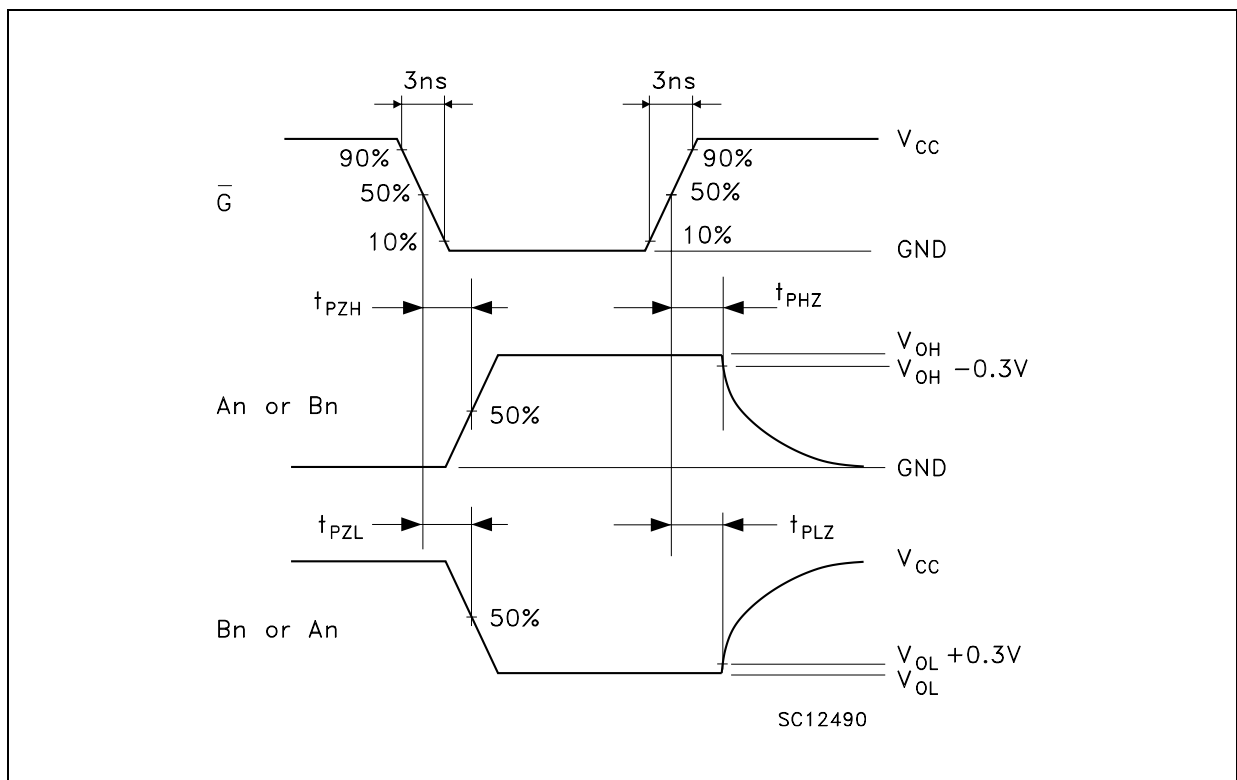


TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	V _{CC}
t _{PZH} , t _{PHZ}	GND

C_L = 15/ 50pF or equivalent (includes jig and probe capacitance)

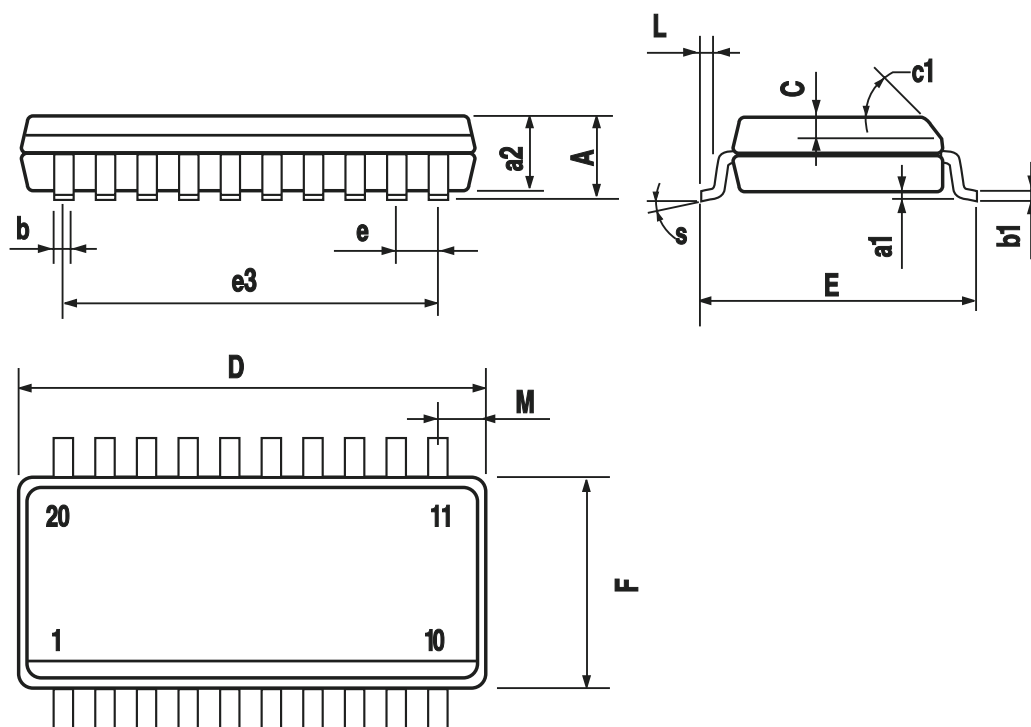
R_L = R₁ = 1KΩ or equivalent

R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME** ($f=1\text{MHz}$; 50% duty cycle)

SO-20 MECHANICAL DATA

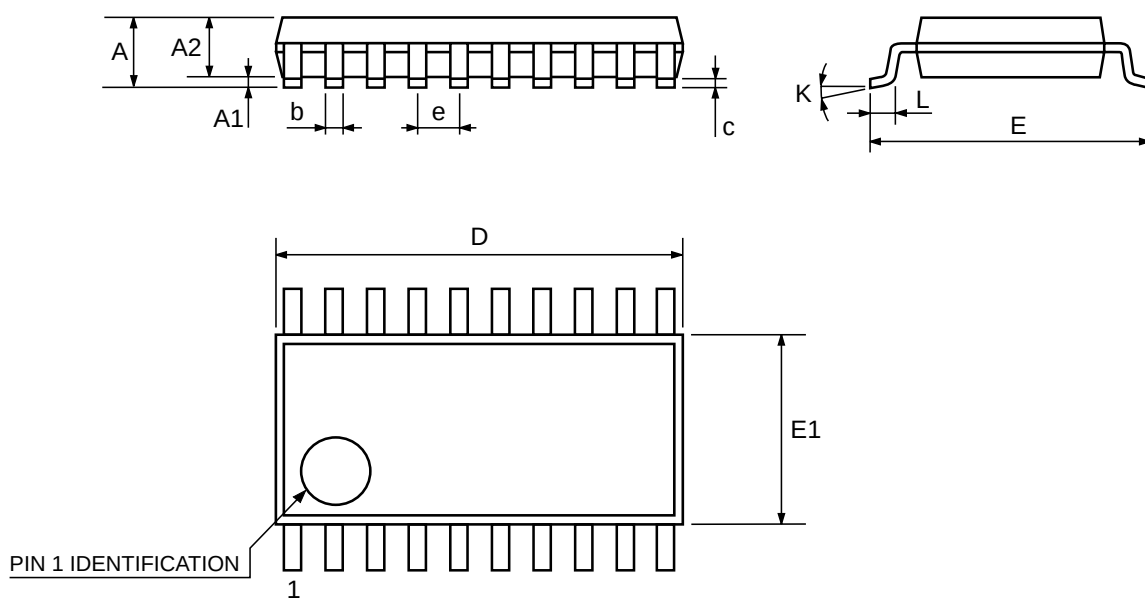
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					



PO13L

TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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