- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages**

DGG OR DL PACKAGE
(TOP VIEW)

S0	1	56	S1
1A1	2	55	S2
1A2	3	54	1B1
2A1	4	53	1B2
2A2	5	52	2B1
3A1	6	51	2B2
3A2	7	50	3B1
GND	8	49	GND
4A1	9	48	3B2
4A2	10	47	4B1
5A1	11	46	4B2
5A2	12	45	5B1
6A1	13	44	5B2
6A2	14	43	6B1
7A1	15	42	6B2
7A2	16	41	7B1
V_{CC}	17	40	7B2
8A1	18	39	8B1
GND	19	38	GND
8A2	20	37	8B2
9A1	21	36	9B1
9A2	22	35	9B2
10A1	23	34	10B1
10A2	24	33	10B2
11A1	25	32	11B1
11A2	26	31	11B2
12A1	27	30	12B1
12A2	28	29	12B2

description

The SN74CBT16212 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.
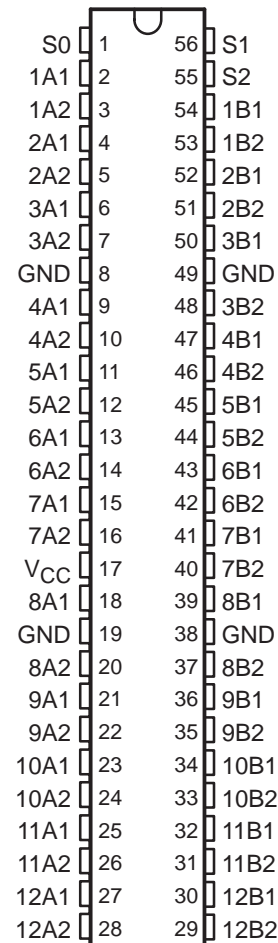
The device operates as a 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0–S2) terminals.

The SN74CBT16212 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 = B1
L	H	L	B2	Z	A1 = B2
L	H	H	Z	B1	A2 = B1
H	L	L	Z	B2	A2 = B2
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 = B1, A2 = B2
H	H	H	B2	B1	A1 = B2, A2 = B1

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TEXAS INSTRUMENTS

SN74CBT16212
24-BIT BUS-EXCHANGE SWITCH

logic diagram
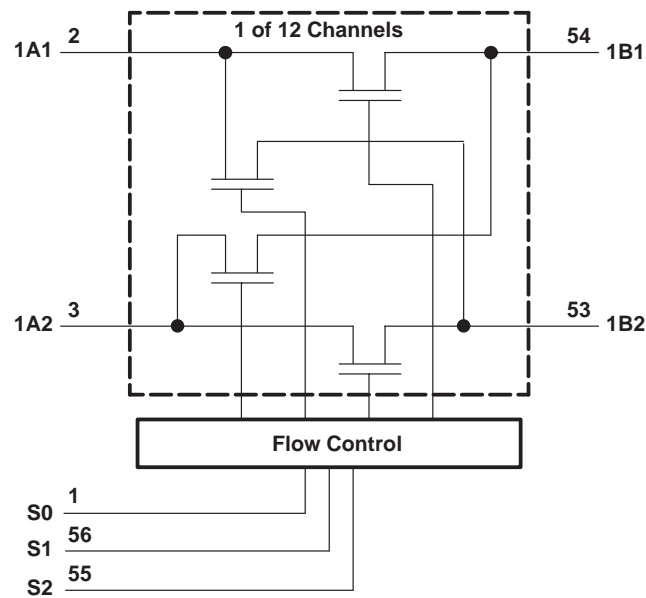
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Continuous channel current .... 128 mA
Input clamp current, I_{IK} (V_I < 0) .... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package .... 1 W
DL package .... 1.4 W
Storage temperature range, T_{stg} .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = − 18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	S0, S1, or S2 = V_{CC}			7.5		pF
r_{on}§		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA				Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		4	7	
				I_I = 30 mA		4	7	
			V_I = 2.4 V,	I_I = 15 mA		6	12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

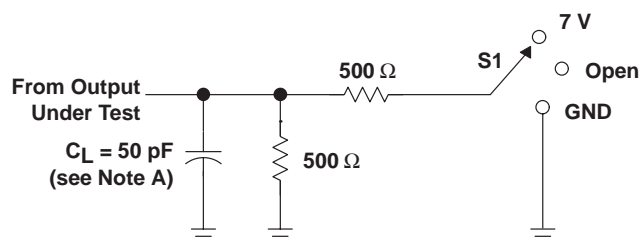| PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		V_{CC} = 4 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.25		0.25	ns
t_{pd}	S		2.6	10.2		11.3	
t_{en}	S	A or B	2.7	10.6		11.5	ns
t_{dis}	S	A or B	1.2	11.3		12.1	ns

¶ This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT

From Output Under Test — $500\ \Omega$ — S1 — 7 V / Open / GND

$C_L = 50$ pF (see Note A) $500\ \Omega$
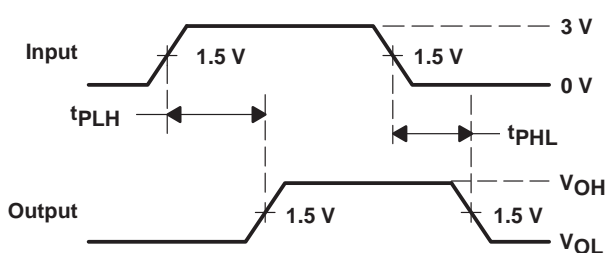
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

Input — 1.5 V ... 1.5 V — 3 V / 0 V
t_{PLH} t_{PHL}
Output — 1.5 V ... 1.5 V — V_{OH} / V_{OL}
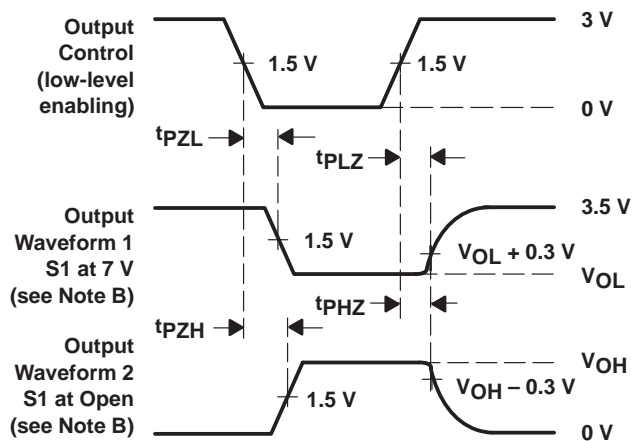
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

Output Control (low-level enabling) — 1.5 V ... 1.5 V — 3 V / 0 V
t_{PZL} t_{PLZ}

Output Waveform 1 S1 at 7 V (see Note B) — 1.5 V — 3.5 V / $V_{OL} + 0.3$ V / V_{OL}
t_{PZH} t_{PHZ}

Output Waveform 2 S1 at Open (see Note B) — 1.5 V ... $V_{OH} - 0.3$ V — V_{OH} / 0 V

NOTES: A. C_L includes probe and jig capacitance.
    B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
    C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
    D. The outputs are measured one at a time with one transition per measurement.
    E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
    F. t_{PZL} and t_{PZH} are the same as t_{en}.
    G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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