AS3916

868 MHz and 433 MHz ISM Band ASK FSK Transceiver

Preliminary Data Sheet

1 Key Features

- ❒ Supports triple band operation: Europe 868 MHz and 433 MHz.
- ❒ Designed to be conform to EN 300 220.
- ❒ Maximum available TX power 4 mW in 400Ω load.
- ❒ Strongly duty-cycled RX operation for low polling mode current possible.
- ❒ Wide supply range between 2,2 to 3.6 V.
- ❒ Low current consumption, TX typ. 23 mA @ 2,2 V at 6 dBm available TX power, RX: typ. 14 mA @ 2,2 V.
- ❒ Supports clock for an external µC and allows clock free total shut down of the whole system.
- ❒ Provides clock free system wake-up by buttons as well as conventional wake-up by µC.
- ❒ Low standby current, typical <0,5 µA.
- ❒ Wide operating temperature range from -40 °C to +85 °C.
- ❒ Only 25 ppm (at 868 MHz) or 50 ppm (at 433 MHz) tolerance of reference frequency required.
- ❒ Provides on chip XTAL oscillator and allows use of an external reference frequency.
- ❒ Typically only 1 XTAL, 8 capacitors and 2 inductors externally required.

Filtered Frequency Shift Keying (FFSK)

- ❑ Performs transparent Filtered Frequency Shift Keying (FFSK) data transmission.
- ❑ Provides highly stable FSK frequency deviation.
- ❑ Data rate range for FSK from 0 to 20 kbit/s. No data synchronization required.
- ❑ RX sensitivity typical -100 dBm @ 20 kbit/s.

Amplitude Shift Keying (ASK)

- ❑ Performs Amplitude Shift Keying (ASK), on off keying
- ❑ Data rate range for ASK from 0 to 10 kbit/s.
- ❑ RX sensitivity typical -110 dBm @ 10 kbit/s.

2 General Description

The AS3916 is a low power, double ISM band (868 / 433 MHz), single channel ASK/FSK transceiver designed to work in a remote control links together other AS3916.

In TX mode the AS3916 performs direct FFSK modulated or ASK modulated data transmission. The FSK frequency deviation is of XTAL controlled precision, and no synchronization between the transmit datastream and the AS3916 processing clock is required.

In RX mode the AS3916 performs transparent data reception without any synchronization between the received stream and the AS3916 processing clock and without data decoding.

To save battery power the AS3916 can be operated in a duty cycled RX mode where it periodically checks if a valid transmission is ongoing. The trade-off between current consumption and reaction time can be selected in a wide range by a programmable repetition interval of the wake-up sequences.

The AS3916 contains a general bi-directional 9 line micro-controller (µC) interface to support the µC with clock-reset- and control- signals and to operate the highly efficient power up/down management including a clock-free total shut-down of the whole transmitter system.

As external components the AS3916 needs at minimum only a reference XTAL, 8 capacitors and up to 2 inductors.

3 Applications

- ❒ Key-less car entry systems.
- ❒ Short range packet oriented data transmission.
- ❒ Security applications and alarm systems.
- ❒ Domestic remote control systems.
- ❒ Industrial remote control systems.
- ❒ Remote metering.

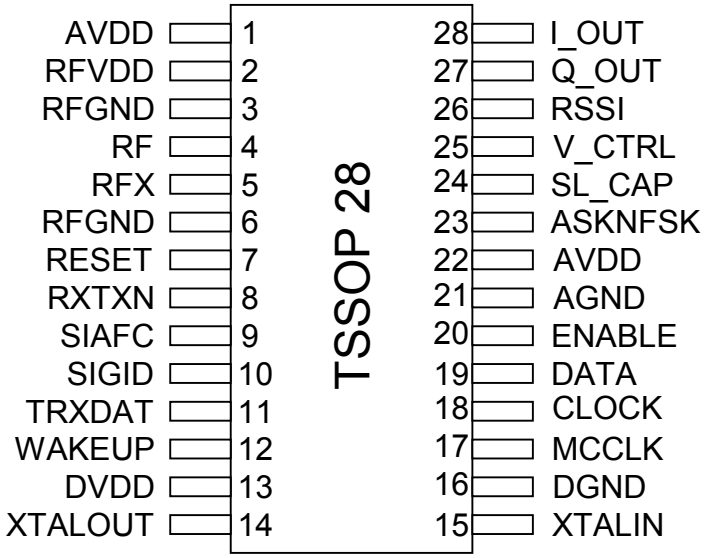

Figure 1: Preliminary pin-out of the AS3916.

4 Functional Description

The AS3916 contains a direct I/Q modulated FFSK transmitter. Data transmission is transparent. The TX data rate may vary in wide range, given by the application. The transmit data stream is converted in an I/Q conversion block into a pair of analog FSK I/Q base-band signals. After a smooth filtering for bandwidth control an I/Q based direct up converter shifts the base-band signals with the help of a LO signal at carrier frequency directly up to RF. Finally a driving amplifier provides a programmable RF output power.

The AS3916 contains a direct conversion receiver for Frequency Shift Keying (FSK) modulated RF signals with a frequency deviation Δf of $\approx$60 kHz around a carrier frequency fc. Data reception is transparent in a range of 0 to 20 kbit/s without any synchronization or decoding.

The received RF-signal is amplified in an LNA, and converted in a quadrature down converter directly to baseband. After low-pass filtering for channel selection and amplification, the data signal is reconstructed in a digital implemented demodulator. The demodulated data is directly delivered to the data output.

A double band single channel RF- synthesizer supports TX and RX part with the required LO signal. As frequency reference for the RF synthesizer and the digital part, an on board XTAL oscillator (XO) is available.

A transceiver control block containing a sophisticated power up/down circuitry, which allows clock-free low-power standby. For wake-up of the transceiver system in TX mode (AS3916 and µC) and configuration download, a µC interface which also supports the µC clock is implemented.

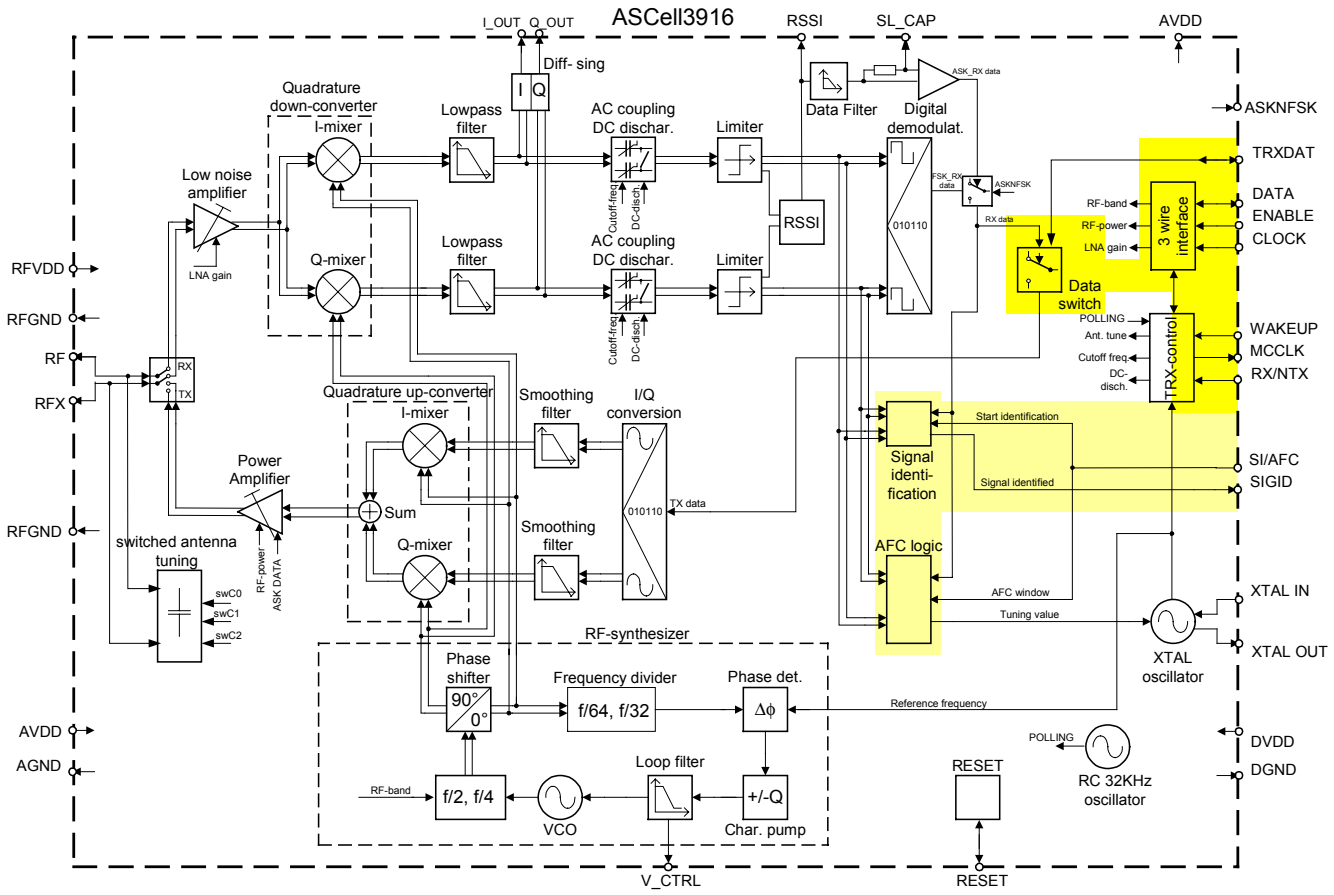

Figure 2: Block diagram of the AS3916. The customizable blocks are shaded.

The AS3916 can be switched between ASK and FSK (Pin23= ASKNFSK).

ASKNFSK	RXNTX	Function
0	0	Transmitting ASK data
0	1	Receiving ASK data
1	0	Transmitting FSK data
1	1	Receiving FSK data

Table 0: ASK FSK and RX TX programming

4.1 Transmit Path

The AS3916 provides transparent data transmission. The data rate range is 0 to 20 kbit/s. No error-protection or channel coding or further signalization is provided.

4.1.1 Modulation

The transmit-data with a data rate RTX in a range of 0 to 20 kbit/s enters the AS3916 via the TRXDAT pin. No bit synchronization of the data stream to the AS3916 processing clocks is required. The AS3916 generates Filtered FSK (FFSK) modulation. Therefore the data is transformed into a complex FSK base-band signals in an I/Q conversion block.

The FSK frequency deviation Δf_{TX} of ≈60 kHz is crystal controlled and slightly dependent of the ISM band, as given in Table 1.

f_{CTX} / MHz	Δf_{TX} / kHz
433,920	60,54
868,300	60,57

Table 1: Nominal transmit frequency deviations for the different ISM frequency bands.

After filtering in smoothing filters for spectrum control, the base-band FFSK signals are delivered to the I/Q direct conversion mixer.

4.1.2 Direct Up-Conversion Mixer

The modulation base-band signals are converted to RF band with the help of an I/Q local oscillator signal. The direct up conversion mixer is optimized for high linearity and low carrier leakage.

4.1.3 Driving Amplifier

The driving amplifier has a differential open collector output optimized for driving typical SAW filters or symmetrical medium-impedance (loop) antennas. The amplifier drives a maximum RF current of 3.5 mA_{RMS}. The maximal differential voltage swing is about 4 V_{PP}. Therefore, the output power is a function of the connected load impedance. With a R_{LOAD} = 400 Ω differential load a maximum peak output power (to the antenna) of ≈4 mW is obtained. The output power can be set in steps of 6 dB with the means of the PWR [1..0] control word.

PWR1	PWR0	Available output power	Comment
0	0	6	Default
0	1	0	
1	0	-6	
1	1	-12	

Table 2: Output power programming value and available output power in R_{LOAD} = 400 Ω.

Please note that the final radiated power (from antenna) is lower and strongly dependent on the efficiency of the antenna (function of the size).

To combat influences from temperature changes, the driving amplifier can be operated in a level control loop which tries to keep the voltage swing across the load resonance circuit constant (working for a limited range around the nominal impedance). Setting the Level ContRol bit (LCR) to “1” turns on the level control.

4.1.4 Switched Antenna Tuning

The ASCell3916 is optimized to drive small, symmetrical loop antennas. These antennas have usually a high quality factor and therefore sometimes suffer sub optimum antenna tuning caused by manufacturing tolerances of the antenna (PCB) and objects close to the antenna. To combat these effects the ASCell3916 contains a switched antenna tuning.

SwC2	SwC1	SwC0	Variable parallel capacitance C_T / fF	Comment
0	0	0	0	
0	0	1	200	
0	1	0	400	Default
0	1	1	600	
1	0	0	800	
1	0	1	1000	
1	1	0	1200	
1	1	1	1400	

Table 3 Antenna tuning factor and corresponding tuning capacitance value.

4.1.5 ASK Transmitter

The transmitted ASK date are generated by switching the power amplifier on off.

There is a kind of power ramping implemented.

There is an offset of 60KHz from the carrier.

4.2 Receive Path

The AS3916 provides transparent data reception. The data rate range is 0 to 20 kbit/s. No error-protection or channel decoding is provided.

4.2.1 Low-Noise Amplifier

The LNA performs the first amplification of the RF signal. The gain of the LNA can be switched between two 10 dB different states. The gain switching is performed by the “LNA” bit of the configuration command, where LNA = 1 is default and means high gain.

4.2.2 I/Q Down Converter

The AS3916 contains a high performance quadrature down converter which converts the RF signal in I and Q component down to baseband. The mixer is designed for low output DC offset and low LO leakage through the RF input port, to minimize the well known direct-conversion DC offset- and LO-leakage problems.

4.2.3 Base Band Filter

To achieve optimum blocking performance, two 7th order low pass filters with butterworth charakteristic are designed for I/Q channel.

4.2.4 DC-Cancellation and Adjustment of Lower Cut-Off Frequency

Generally, AC coupling (first order high-pass filters) with selectable cut-off frequency removes the DC offset of the quadrature down converter and the following baseband filters. This AC coupling is performed in three steps, optimized for the carrier frequency tolerance.

Step 1: Power up

After the receiver analog part power-up, the outputs of the AC coupling capacitors are shorted for a short time, to minimize the DC settling time of the limiter. This is performed automatically at any turn on of the AS3916.

Step 2: RF reception prior AFC

Operating without AFC and after any power up, the cut-off frequency of the AC coupling is kept low (about 10 kHz). This allows the RX signal to pass more or less undistorted, because of the frequency offset between the received carrier at f_{CTX}, and the RX nominal carrier frequency f_{CRX}. Disadvantage of this state is the longer DC settling time after strong burst interferers.

Step 3: RF reception after AFC

After the AFC procedure, the received spectrum is symmetrical with respect the RX LO. The lower cut-off frequency of the AC coupling is automatically set to about 40 kHz. This reduces the IF noise bandwidth and reduces the DC settling time of the base-band chain due to dynamic DC changes after strong burst interferers.

4.2.5 I/Q Limiter

The IQ limiters are AC coupled multistage amplifiers with a gain of about 80dB. Receive Signal Strength Indicator (RSSI) generators are included for the I/Q channel. The RSSI signal is used for detection of input power.

4.2.6 FSK Demodulator

The FSK demodulator reconstructs a raw data stream from the limited I and Q signals which corresponds to the pattern of frequency deviations around the carrier. The demodulator incorporates a digital post-demodulator (anti-glitch) filter, optimized for data rates from 10 to 20 kbit/s. In RX mode the output of the demodulator is switched to the TRXDAT pin.

For lower data rates some additional post demodulator filter, e.g. implemented in the µC will increase the performance.

4.2.7 AFC Logic

During an interval, given by the Signal Identification / Automatic Frequency Control (SIAFC) line = 1, the automatic frequency control (AFC) block measures the frequency deviation between the received signal and the local oscillator. From this it calculates and XO Set value (XOS) for the XO, to tune the frequency difference to a small value.

For the AFC operation no special data pattern is required. The AFC works properly as long as the average high to low time of the investigated data segment is in the range of 3/1 to 1/3.

Please note that the signal identification procedure is performed in parallel to AFC operation.

4.2.8 Signal Identification Block

Using the AS3916 signal identification is responsibility of the microcontroller.

To shorten and ease the µC the identification of a valid signal the AS3916 can provide a rough pre-selection by the signal identification block. During an interval given by the Signal Identification / Automatic Frequency Control (SIAFC) line = 1 the signal identification block checks if the limited I/Q signals are corresponding to a FSK frequency deviation ΔfRX is in the range of the nominal frequency ΔfTX deviation provided by an AS3916 or ASCell3913.

For the signal identification no special data pattern is required. Signal identification is possible as long as the average high to low time ratio of the investigated data segment is in the range of 3/1 to 1/3.

If the result is positive, the signal identification block sets the SIGnal IDentified (SIGID) output to 1 to indicate a possibly valid signal. The µC may only proceed further signal identification if this result is positive. The AFC operation may be executed multiple times during reception.

Please note, if enabled, the AFC procedure is performed in parallel to signal identification.

4.2.9 ASK Receiver

The RSSI Signal is used for demodulation.

4.3 Shared Blocks

The shared blocks support both, the AS3916 TX and RX blocks.

4.3.1 XTAL Oscillator (XO)

The AS3916 contains a tunable dual-pin XO. It is used as frequency reference for the AS3916 synthesizer, the digital blocks, the wake-up timer, the receiver control block, the I/Q conversion and the three wire interface.

Tuning can be performed:

1. Manual by configuration download of the XOP [3..0] word via the three wire interface or
2. Automatically by running an Automatic Frequency Control (AFC) cycle by the digital controller.

If an external frequency reference shall be used, the XTALIN pin can be overwritten by a standard CMOS digital signal.

Due to the XO is supporting the clock to the wake-up timer in polling mode it has to be permanently tuned on after the power-on reset.

4.3.2 RF Synthesizer

The synthesis of the transmit carrier frequency is performed by a fully integrated single channel synthesizer. It consists of a voltage-controlled oscillator (VCO), a feedback frequency divider, a phase detector, a charge pump, and an integrated loop filter. The VCO is working at 1.736GHz. The feedback divider divides by 128, and is inherently generating 0° and 90° shifted LO signals. The different ISM bands are selected by the frequency control bit “RANGE”. A truth table for the selection of the different frequencies is given in Table 4.

f_{XO} / MHz	RANGE	f_{CTX} / MHz
13,5672	1	868,300
13,5600	0	433,920

Table 4: Transmitter configuration for different RF output frequencies. “RANGE” is the bit of the configuration information.

4.3.3 Microprocessor Clock Generation

The AS3916 control block provides a clock for use in an external microcontroller. To provide a rather constant clock frequency f_{MCLK} in all ISM frequency bands, the XTAL frequency f_{XO} is divided by 4. Therefore the use of common software in all ISM frequency bands is envisaged. The AS3916 configuration for the µC clock is given in *Table 5*.

f_{XO} / MHz	Division factor	f_{MCLK} / MHz
13,5600	4	3,3900
13,5672	4	3,3918

Table 5: µC clock frequencies in different frequency bands.

4.3.4 Polling Mode

A 32KHz oscillator has been implemented for generating an internal wakeup signal. This mode can be activated with the control bits POLL0 and POLL1. A truth table for the selection of the different modes is given in *Table 5*.

POLL0	POLL1	Polling intervall
0	0	disabled
0	1	20ms
1	0	50ms
1	1	100ms

Table 5: specifies the polling interval.

Working in the polling mode the receiver wakes up periodically. During an interval given by the polling control bits the signal identification block checks if the limited I/Q signals are corresponding to a FSK frequency deviation. If the result is positive, the signal identification block sets the SIGnal IDentified (SIGID) output to 1 to indicate a possibly valid signal. The µC may only proceed further signal identification if this result is positive. Then the µC have to set the “WAKEUP” pin to 1 otherwise the receiver goes sleeping.

4.4 Three Wire Interface

The three-wire interface is a synchronous serial interface and is compatible with microcontroller SPI and USART interfaces. The interface consists of the lines:

1. Data input DATA.
2. Enable input ENABLE.
3. Clock input CLOCK.

They are used for download of configuration data and readout of the AS3916 status data. The three wire interface is completely independent of the wake-up and shut down. This means data can be download independent if the AS3916 is in standby, or transmitting.

4.4.1 Interface Timing

Timings are drawn in Figure 3 and Figure 4 as seen from the microcontroller. DATA bits are sampled on the falling edge of CLOCK.

Write Cycle

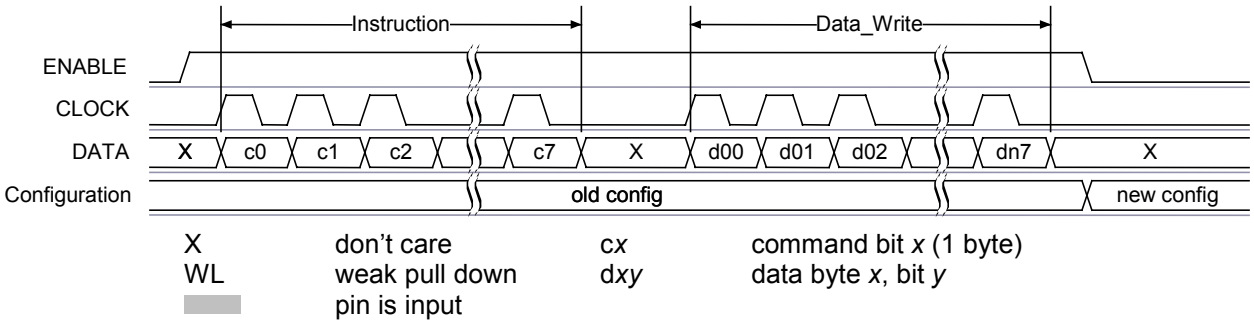

Figure 3: Three-wire interface write cycle.

Figure 3 shows the timing for a write cycle. The instruction byte is transmitted followed by the data bytes. After the falling edge of ENABLE the new data is valid.

Read Cycle

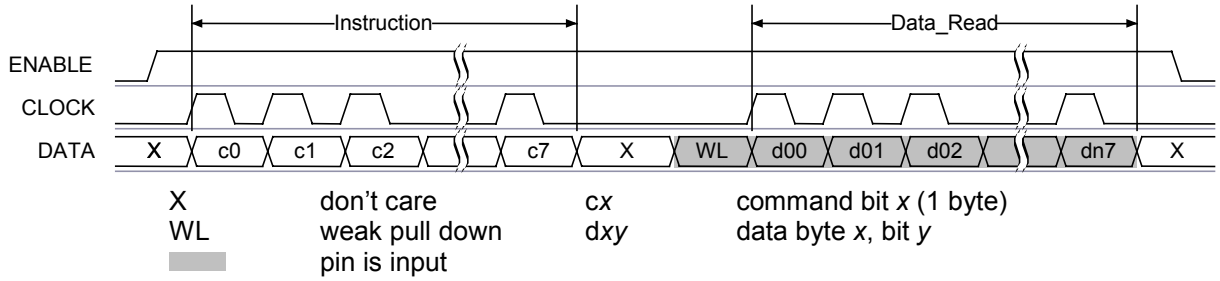

Figure 4: Three-wire interface read cycle.

Figure 4 shows the timing for a read cycle. After writing the instruction to the AS3916, the microcontroller switches to reading mode. With the rising edge of the first data bit the AS3916 starts driving the DATA wire and continues driving till the falling edge of ENABLE. A weak pull down is included in the AS3916 DATA port.

4.4.2 Instruction Byte

The first byte of a three-wire interface communication is an instruction byte determining the rest of communication

Bit #	Name	Description
0	W/RN	0: Write operation 1: Read operation
1.. 3	TY[0:1]	Register selection: 000: Device configuration (read/write possible) 001: Device status (read only) 101: test analog 010: not used 011: not used
4		not used
5..7		Not used

Table 6: AS3916 instruction byte.

4.4.3 Implementation Notes

The ENABLE signal has to be set manually in the microcontroller program before and after the communication since this signal is usually not provided with SPI/USART interfaces.

Since the DATA port is bi-directional and the microcontroller SPI interface has separated SDI/SDO ports it can only be used if the ports are shorted and SDO is programmed high resistive during SPI reception.

4.5 Transceiver Control Block

4.5.1 Transmitter

The transceiver control block of the AS3916 manages all internal state switching and timings, which are necessary for all operation. It also incorporates two interface wires for wake-up, button management, power management and clock handling together with a microcontroller. The lines are:

1. Active 1 Wake Up Input with turn-off reaction delay to allow the µC button scanning (WAKEUP).
2. Microcontroller Clock output (MCCLK).

The WAKEUP line incorporates a wake up time-out of t_{WTO} which allows is together with the MCCLK output a sophisticated wake-up and button scanner function, which a suitable for button or microcontroller initiated system wake-ups.

4.5.2 Receiver

The principal function of the RX control block is to control the transition between the AS3916 internal states, which are:

1. Sleep mode.
2. Data reception.

It has to in-time start sub-functions like:

1. Data transfer to and from the 3-wire interface.

It also has to manage external interrupt and control signals:

1. MCCLK
2. WAKEUP

5 Transceiver Operation and Timing

The transmit operation can be started under button control or under µC control.

5.1 Button Initiated Wake-Up.

Figure 5 shows the interconnection of the ASCell3913 with a typical µC for button initiated wake-up, and button or µC controlled stop of transmit, which is assumed to be the typical application in most remote control cases.

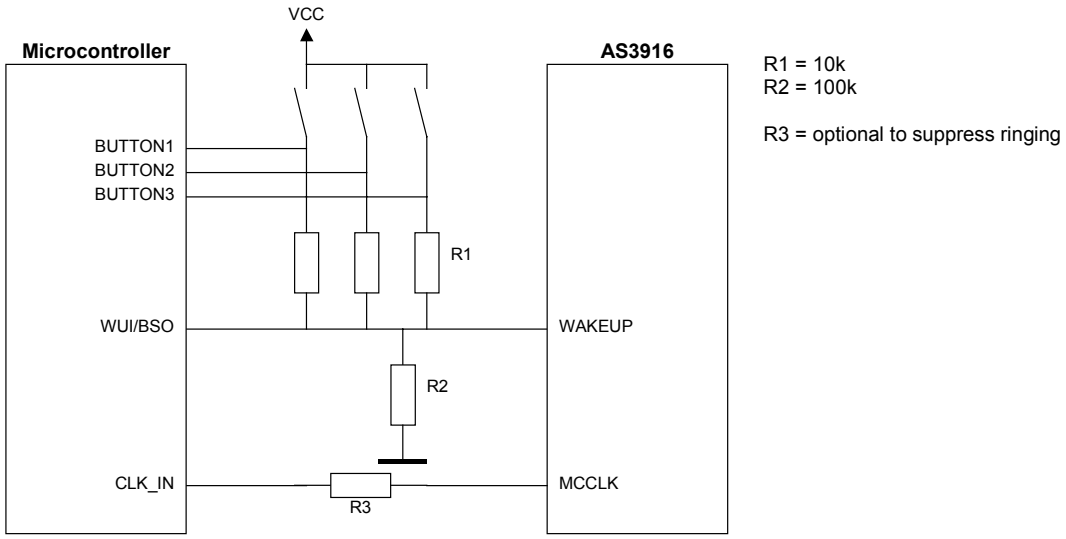

Figure 5: Interconnection example of the AS3916 with a typical µC, where pressing of a button wakes up the AS3916 which wakes up the µC by starting its clock. The µC may scan which button is pressed when it sets its WUI/BSO pin temporarily as 0-level output. The release of the button or the µC may stop the transmit activity.

5.1.1.1 Button Initiated Wake-Up - µC controlled Transmit Stop

Figure 6 shows a typical timing for AS3916 button initiated Wake-Up - µC controlled transmit stop.

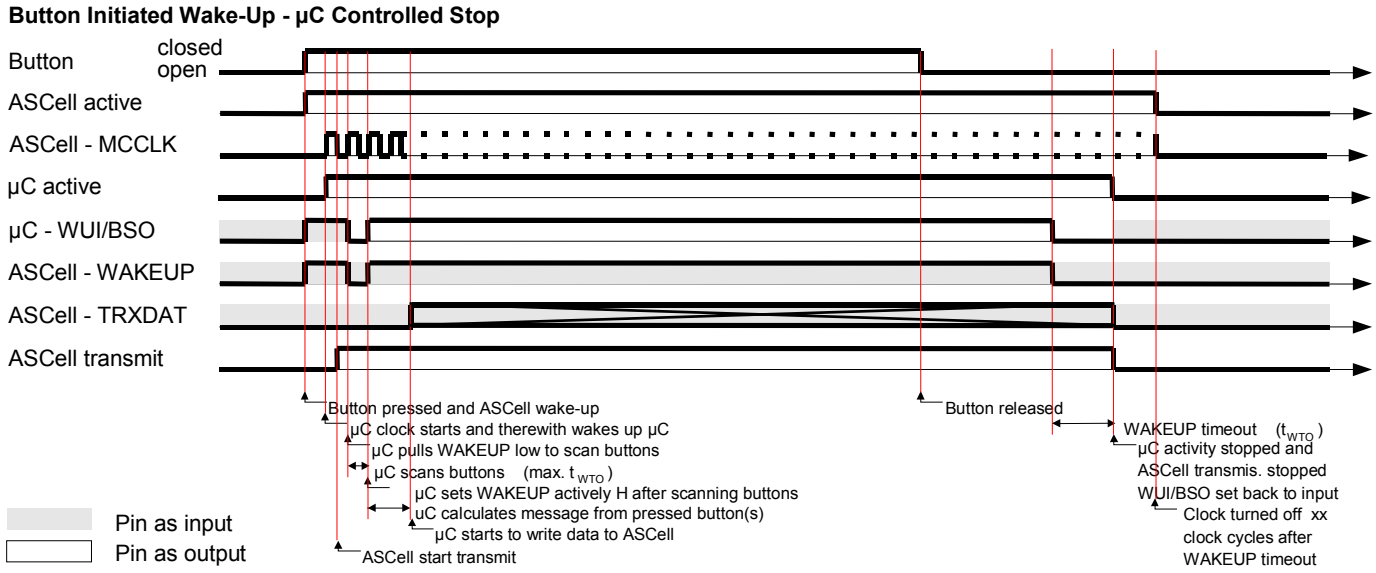

Figure 6: Typical AS3916 µC interface timing for button initiated wake-up and µC controlled power down.

The AS3916 and the µC are in clock-free standby mode, no clock is running. The AS3916 WAKEUP pin as well as the µC Wake Up Input / Button Scan Output (WUI/BSO) pin are configured as inputs.

If one button is closed the WAKEUP inputs of the AS3916 and the WUI/BSO pin of µC are forced to 1. The AS3916 wakes up and powers up its XO. After T_{XOON} it starts to support µC clock at the MCCLK pin.

The µC is activated by WUI/BSC = 1 and starts to operate with the µC clock from the AS3916. After initialization the µC changes the WUI/BSC pin for at maximum t_{WTO} to output and sets it to low. During this time the µC is able to scan (identify) the pressed button(s). Then it sets the WUI/BSC pin to 1 for the duration of sending data plus at least the wakeup to the AS3916.

After the message establishment in the µC, the µC writes the transmit-message to the TRXDAT pin of the AS3916. When the complete message has been transmitted the µC sets the WUI/BSO output to 0 and this shuts down the AS3916 after the wakeup timeout t_{WTO}.

After this the µC has to shut down within TCLK clock cycles and to set the WUI/BSO pin back to input. The whole system is now again in clock-fee standby. The provided additional clock cycles are programmed by the TCLK[4..0] programming word.

5.1.1.2 Button Initiated Wake-Up - Button controlled Transmit Stop

Figure 7 shows a typical timing for AS3916 button initiated Wake-Up – button controlled transmit stop.

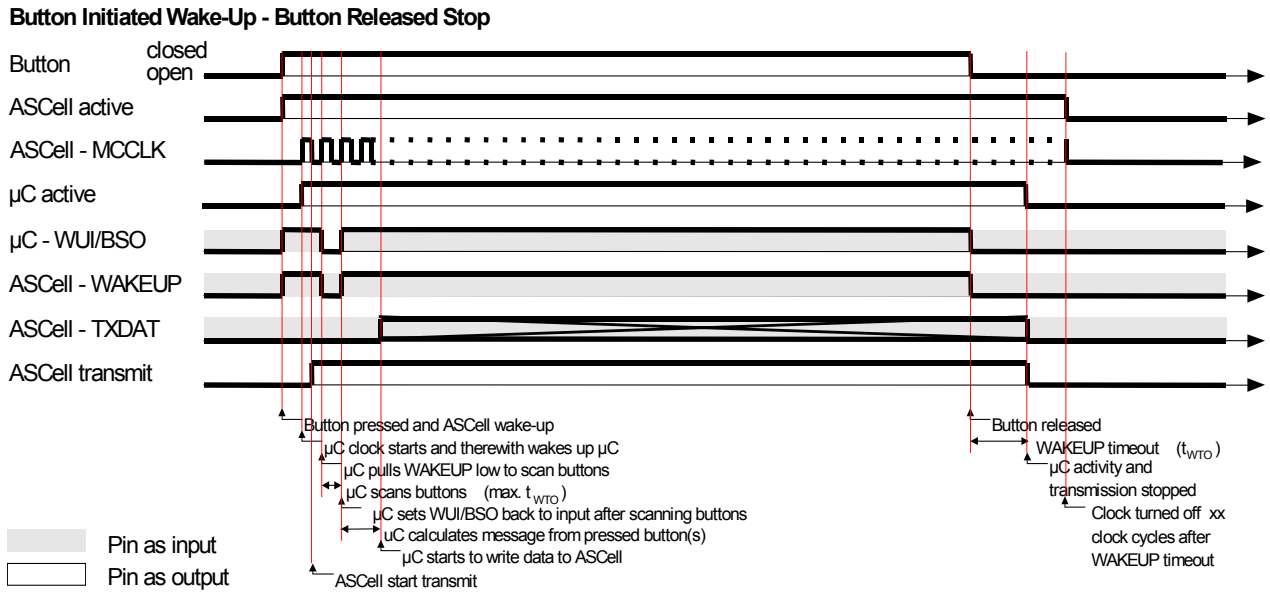

Figure 7: Typical AS3916 µC interface timing for button initiated wake-up and button release power down.

The AS3916 and the µC are in clock-free standby mode, No clock is running. The AS3916 WAKEUP pin as well as the µC Wake Up Input / Button Scan Output (WUI/BSO) pin are configured as inputs.

If one button is pressed the WAKEUP input of the AS3916 and the WUI/BSO pin of µC are forced to 1. The AS3916 wakes up and powers up its XO. After T_{XOON} it starts to support µC clock at the MCCLK pin.

The µC is activated by WUI/BSC = 1 and starts to operate with the µC clock from the AS3916. After initialization the µC changes the WUI/BSC pin for at maximum t_{WTO} to output and sets it to low. During this time the µC is able to scan (identify) the pressed button(s). Then it sets the WUI/BSC pin back to input to wait for a 0 which indicates the release of all buttons.

After the message establishment in the µC, the µC writes the transmit-message to the TXDAT pin of the AS3916.

In this case the duration of pressing a button defines the duration of transmission. During at least one button is pressed, the AS3916 will continuously transmit data delivered by the µC. Therefore the AS3916 will support µC clock from MCCLK until TCLK clock edges after the AS3916 has stopped transmitting.

One wakeup timeout time t_{WTO}, after the last button has been released, the AS3916 stops the RF transmission. After this the µC has to shut down within the TCLK clock cycles the AS3916 provides prior going standby. The whole system is now again in clock-fee standby.

5.1.2 Microcontroller Initiated Wake-Up and Stop Transmit

Figure 8 shows the interconnection of the AS3916 with a typical µC for µC initiated wake-up. Figure 9 presents a related timing for power up and down of the transmitter.

Figure 8: Interconnection example of the AS3916 with a typical µC, where the µC wakes up and shuts down the AS3916.

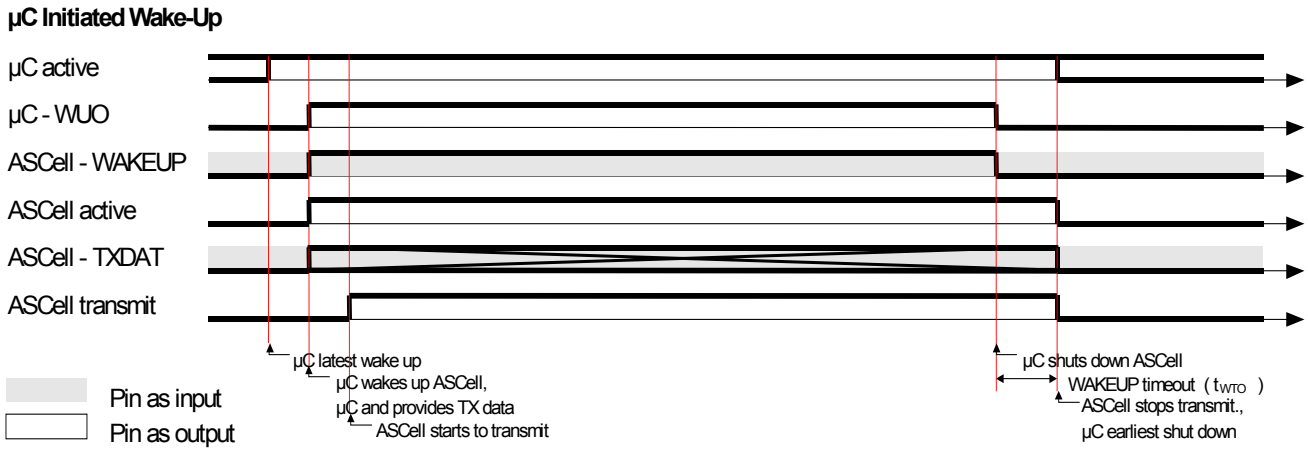

Figure 9: Typical AS3916 µC interface timing for µC initiated wake-up and power down.

The AS3916 is initially shut down. The µC is active or powered up by its own wake-up timer. The µC wakes up the AS3916 by setting the WUO pin to 1. The AS3916 turns on its own XO, which takes T_{XTON} or uses an external clock as reference frequency.

The duration of WAKEUP = 1 is defining the duration of transmission. During WAKEUP = 1, the AS3916 will continuously transmit the data written to TXDAT by the µC. Therefore the µC has to be awake as long as the transmission is required.

One wakeup timeout time t_{WTO}, after WAKEUP has been set to 0 by the µC the AS3916 stops the RF transmission and, if used, turns off its XO. Also the µC may now go asleep. However, if the AS3916 uses an external clock, this has to be available until this time. The whole system is now again in standby.

5.2 Receiver Timing and Operation

The AS3916 acts as receiver (RX) when RXTXN = “1”.

5.2.1 Receiver Timing

The AS3916 with its on board XO can be operated in two modes:

1. As master oscillator, where the XO is permanently on and the AS3916 is supporting the µC with the MCCLK clock.
2. As autonomous device, waked up by a µC which has its own clock. In this case the on board XO it turned on only when used by the AS3916. In this application the XO can also be overwritten by an external reference clock signal.

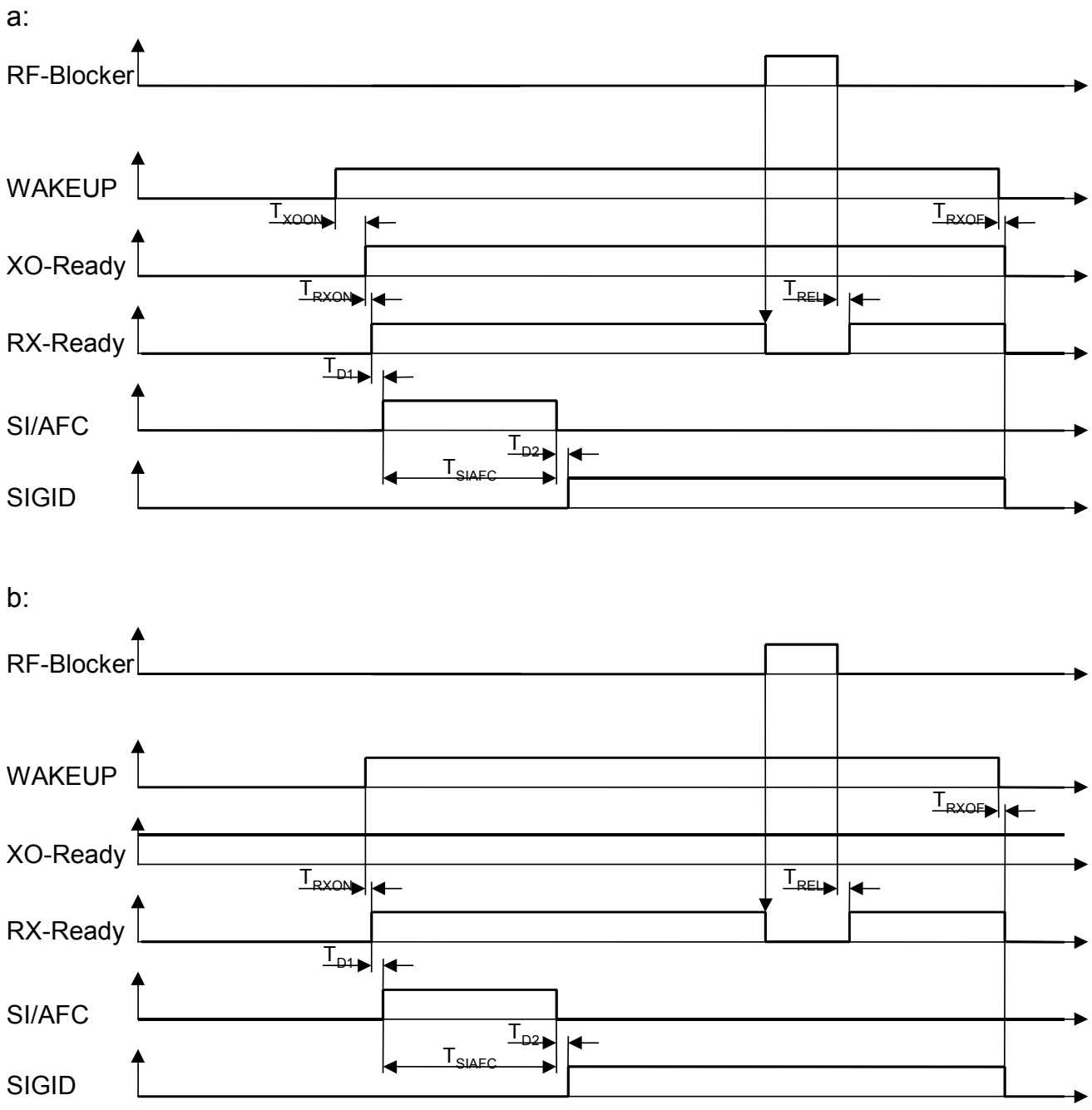

Figure 10: AS3916 basic timing.
***a:** XO only turned on when receiving.*
***b:** operated as master timer with permanently running XO.*

5.2.2 Receiver States

The receiver state can be controlled by the two bit receiver state control word RXST1 as shown in Table 7. If RXST1 = 0 the µC must have its own oscillator due to the AS3916 XO is turned off when WAKEUP is set to 0. For RXST1 = 1 the µC may use the AS3916 µC clock MCCLK which is permanently running when switching between standby and receiving.

MCCLKOFF	WAKEUP	AS3916 status	MCCLK	Comment
0	0	Standby	On	XO running or external reference.
0	1	Receiving	On	XO running or external reference.
1	0	Off	Off	XO off. µC must have its own clock!
1	1	Receiving	Off	XO running or external reference µC must have its own clock!

Table 7: Setting of receiver state by the RXST1 word and WAKEUP input and related MCCLK activity in.

6 Transceiver Status and Configuration Information

The three-wire interface of the AS3916 is used for downloading TX and RX configurations and for reading out status information data.

6.1 Status Registers

The content and format of the one byte long AS3916 RX status register is shown in Table 8. Bit 0 is readout by the µC at first.

Bit #	Name	Meaning	Parameters	Default / Comments
0				Not used
1				Not used
2..3				Not used
4..7	XOS[3..0]	XTO set value	0_H to 7_H	Has been set by download or generated by AFC operation

Table 8: AS3916 RX status information in the status register.

6.2 Configuration Registers

The content and format of the three byte long AS3916 configuration register is shown in Table 9. Bit 0 is written by the µC at first.

Bit #	Name	Meaning	Parameters	Default / Comment
0	CRYSTAL	Quartz crystal frequency	Crystal=0: 13,56MHZ, 13,5672MHz CRYSTAL=1: 19.6875MHz	Default
1	RANGE	Frequency range	0=868,300 MHz 1=433,920 MHz	default
2 3	POLL0 POLL1	Polling interval	0_{DEZ}: disabled 1_{DEZ}: 20ms 2_{DEZ}: 50ms 3_{DEZ}:100ms	Default
4	LNAGAIN	LNA gain	0 = LNA at high gain 1 = LNA at low gain	Default
5 6	RDA0 RDA1	Receiver bit rate	0_{DEZ}: 18.22 kbit/s 1_{DEZ}: 9.11 kbit/s 2_{DEZ}: 4.56 kbit/s 3_{DEZ}: 2.28 kbit/s	Default
7..10	XOP[3..0]	XTO programming value	0_{DEZ} to 15_{DEZ}	7_{DEZ} recommended as default
11..14	TCLK[3..0]	MCCLK turnoff delay	0_{DEZ} to 7_{DEZ}	Default: 0_{DEZ}
15..16	PWR [1..0]	Transmit power level reduction	0_{DEZ}: P_{OUT0} – 6 dB 1_{DEZ}: P_{OUT0} – 0 dB 2_{DEZ}: P_{OUT0} – -6 dB 3_{DEZ}: P_{OUT0} – 12 dB	Default
17	LCROFF	Level control	0 = level control on 1 = No Control level	Default
18	MCCLKOFF	Specifies uC clock	0= enabled 1=disabled	Default
19	AGFOFF	Antiglitch Filter	0= enabled 1=disabled	Default
20..23				Not used

Table 9: AS3916 TX instruction set to be loaded into the configuration register.

6.3 Test analog Register

The content and format of the three byte long AS3916 test analog register is shown in Table 9.1. Bit 0 is written by the µC at first.

Bit #	Name	Meaning	Parameters	Default / Comment
0..2		Not used		
3 4 5	SwC2 SwC1 SwC0	Variable parallel capacitance C_T / fF for Antenna tuning	000 =0fF 001 =200fF 010 =400fF 011 =600fF 100 =800fF 101 =1000fF 110 =1200fF 111 =1400fF	Default
6,,23		Not used		

Table 9.1 Test Analog Register:

7 Electrical Characteristics

7.1 Absolute Maximum Ratings (non operating)

Symbol	Parameter	Min	Max	Units	Note
VDD; AVDD	Positive supply voltage	-0,5	6	V	
GND; AGND	Negative supply voltage	0	0	V	
VIN	Voltage at every input pin	GND-0,5	VCC+0,5	V	
IIN	Input current into any pin except supply pins	-10	10	mA	
ESD	Electrostatic discharge		1k	V	1) 3)
ESDRF	Electrostatic discharge of RF pins		500	V	1) 4)
Tstg	Storage temperature	-55	125	°C	
Tlead	Lead temperature		260	°C	2)
$P_{IN,MAX}$	Maximum input power level at RF+ and RF-.		27	dBm	

1) Test according to MIL STD 883C, Method 3015.7: HBM: R=1,5 kΩ, C=100 pF, 5 positive pulses per pin against supply pins, 5 negative pulses per pin against supply pins [C2].

2) 260 °C for 10 sec (Reflow and Wave Soldering), 360 °C for 3 sec (Manual soldering).

3) All pins except RF-pins.

4) RF pins are: XTAL1,XTAL2, RF+,RF-,LC+ and LC-.

7.2 Operating Conditions

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
VDD	Positive supply voltage		2,2	3,0	3,6	V
GND	Ground		0	0	0	V
TA	Operating temperature		-40		85	°C
IDDTX+6	Current consumption transmitting @ P_{OUT+6}	@ 433,920 MHz and 3,0 V: @ 868,300 MHz and 3,0 V:		18 23		mA mA
IDDTX+0	Current consumption transmitting @ P_{OUT+0}	@ 433,920 MHz and 3,0 V: @ 868,300 MHz and 3,0 V:		15 18		mA mA
IDDRX	Current consumption receiving	VDD = 3,6 V VDD = 3,0 V @ 868 MHz VDD = 2,2 V		12.5 12 12		mA mA mA
IDDXO	Current consumption XO operation	10 pF load at MCCLK pin			500	µA
IDDOFF	Current consumption turned off				0,3	µA
V_{POR}	Power-On-Reset threshold voltage			1.7		V

7.3 Frequency Generation

TA = 23 °C, VDD = 3,0 V, unless specified otherwise. Device functional for TA = -40 to +85 °C.

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
f_{xo}	Crystal oscillator (XOSC) frequency at center tuning value	for 433,920 MHz: for 868,300 MHz:	13,5593[1)] 13,5669[1)]	13,5600 13,5672	13,5607[1)] 13,5675[1)]	MHz MHz
fT_{xo}	Crystal oscillator (XOSC) frequency tolerance at center tuning value.	433,920 MHz: (-40 to +85°C), 868,300 MHz: (-40 to +85°C)			50 25	ppm ppm
f_{CTX}	Carrier frequency at center tuning value	At proper configuration and external crystal.	433,898[1)] 868,279[1]	433,920 868,300	433,942[1)] 868,323[1)]	MHz MHz
f_{CRX}	RX carrier frequency at center tuning value.	At proper configuration and external crystal.	433,898[1)] 868,279[1)]	433,920 868,300	433,942[1)] 868,323[1)]	MHz MHz
Δf_{XO}	XO tuning range	Magnitude of deviation from center tuning value	50 25			ppm ppm
N_{TUNE}	Tuning steps			16		-

1) Minimum and maximum value given by external crystal prior to AFC operation - therefore parameter not production tested.

7.4 Transmit Operation

TA = 23 °C, VDD = 3,0 V, unless specified otherwise. Device functional for TA = -40 to +85 °C.

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
Δf_{TX}	Magnitude of FSK frequency deviation	at 433,920 MHz: at 868,300 MHz:	[1)] [1)]	+60,6 +60,5	[1)] [1)]	kHz kHz
RTX	Transmit data rate	Transparent	0		20	kbps
f_{FSK}	FSK smoothing filter cutoff frequency			180		kHz
R_{LOAD}	Nominal differential load resistance	Resonance resistance R_{LOAD} at f_{CTX} of the load resonance circuit with the impedance Z_{LOAD}		400		Ω
P_{OUT+6}	Available output power, at PWR = 0_{DEZ} into R_{LOAD} (differential)	f_{CTX} = 433,920 MHz: f_{CTX} = 868,300 MHz: at turned on level control	4,5 3,0	6,0 4,5	7,5 6,0	dBm dBm
P_{OUT0}	Available output power, at PWR = 1_{DEZ} into R_{LOAD} (differential)	f_{CTX} = 433,920 MHz: f_{CTX} = 868,300 MHz: at turned on level control	-1,5 -3,0	0,0 -1,5	+1,5 0,0	dBm dBm
P_{OUT-6}	Available output power, at PWR = 2_{DEZ} into R_{LOAD} differential	f_{CTX} = 433,920 MHz: f_{CTX} = 868,300 MHz: at turned on level control	-7,5 -9,0	-6,0 -7,5	-4,5 -6,0	dBm dBm
P_{OUT-12}	Available output power, at PWR = 3_{DEZ} into R_{LOAD} (differential)	f_{CTX} = 433,920 MHz: f_{CTX} = 868,300 MHz: at turned on level control	-13,5 -15,0	-12,0 -13,5	-10,5 -12,0	dBm dBm
$P_{OUT,SPX}$[2)]	Spurious emission power transmitting at $f_{CTX} \pm f_{XO}$ @ P_{OUT+6} into res. circuit with Z_{LOAD} = (differential)	f_{CTX} = 433,920 MHz: f_{CTX} = 868,300 MHz: at turned on level control			-36 -36	dBm dBm

$P_{OUT,SPM}$ [2)]	Spurious emission power transmitting at $f_{CTX} \pm f_{MCLK}$ @ P_{OUT+6} into res. circuit with Z_{LOAD} = (differential)	f_{CTX} = 433,920 MHz: f_{CTX} = 868,300 MHz: at turned on level control			-36 -36	dBm dBm
$P_{OUT,SP4}$ [2) 3)]	Spurious emission power transmitting at 433,920 MHz @ P_{OUT+6} into res. circuit with Z_{LOAD} (differential)	2*433,920 MHz: ≥3*433,920 MHz: at turned on level control			-26 -20	dBm dBm
$P_{OUT,SP8}$ [2) 3)]	Spurious emission power transmitting at 868,300 MHz @ P_{OUT+6} into res. circuit with Z_{LOAD} (differential)	≥2*868,300 MHz: at turned on level control			-20	dBm

1) Minimum and maximum value given by external crystal - therefore parameter NOT production tested.

2) Spurious power measured in reactive load with 400 Ω at the transmit frequency f_{CTX}. The given spurious emission values are backwards calculated by knowing the transfer function of the output resonant circuit. The radiated spurious emissions are dependent on antenna selectivity and efficiency and therefore NOT production tested. Spurious emission suppression at carrier harmonics is part of antenna design.

3) Antenna and matching network attenuation for spurious assumed to be at least 10 dB.

7.4.1 Summary of International Regulations about Radiated RF Power

The following limits of radiated RF-transmit- and spurious emissions by national and international regulations are given as design support.

$P_{TX,E}$	Transmission power Europe (EN 300-220) (2000.09) Table 1	25 to 1000 MHz, Class 7a	-16		7	dBm
$P_{TX,SEE}$	Spurious emission intensity of transmitters in Europe (EN 300-220) (2000.09) Table 13	47 to 74MHz, 87.5 to 118MHz, 174 to 230MHz and 470 to 862MHz: < 1000MHz: > 1000MHz:			-54 -36 -30	dBm dBm dBm
$P_{TX,U}$	Transmission power USA (FCC 47 CFR15)	315 to 322 MHz: not limited				dBm
$P_{TX,SEU}$ [1)]	Spurious emission intensity USA (FCC 47 CFR15) §15.209	<30 MHz (30 µV/m @ 30 m): 30 to 88 MHz (100 µV/m @ 3m): 88 to 216 MHz (150 µV/m @ 3 m): 216 to 960 MHz (200 µV/m @ 3 m): >960 MHz (500 µV/m @ 3 m):			-46 -55 -52 -49 -41	dBm dBm dBm dBm dBm
$P_{TX,SEJ}$	Spurious emission intensity Japan	<322 MHz, (500 µV/m @ 3 m): 322 MHz to 10 GHz, (35 µV/m @ 3 m):			-41 -64	dBm dBm

1) Transmitted spurious power in 100 kHz bandwidth via an isotropic antenna giving in 3 m distance the electrical field-strength as given in the FCC regulations.

7.5 Receiver Operation

TA = 23 °C, VDD = 3,0 V, unless specified otherwise. Device functional for TA = -40 to+85 °C.

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
R_{IN}	Input impedance	Capacitive part t.b.d.		400		Ω
B_{RX}	Receiver bandwidth			200		kHz
Δf_{RX}	Recommended magnitude of frequency deviation	As provided by AS3916		Δf_{TX}		
Δf_{SI}	Tolerated magnitude of frequency deviation for signal identification and AFC	433,920, 868,300 MHz	50		70	kHz
RRX	RX data rate.	Transparent	0		20	kbps
SEN	Receiver sensitivity.	For SRQ[1] at -10 °C<TA<+70 °C		-100		dBm
ΔSEN_{TEMP}	Temperature sensitivity reduction.	-40<TA<-10 °C or +70>TA>+85 °C.			4	dB
ΔSEN_{OFFS}	Receiver sensitivity reduction caused by frequency offset.	@ 44 kHz TX-RX carrier frequency offset.			7	dB
ΔSEN_{LNA}	Sensitivity reduction caused by LNA gain switching.			10		dB
BI_{200kHz}[2]	Blocking immunity 200 kHz..<1 MHz from f_{CRX}.	Without external filter.	0			dB_C
BI_{1MHz}[2]	Blocking immunity 1..<2 MHz from f_{CRX}.	Without external filter	30			dB_C
BI_{2MHz}[2]	Blocking immunity 2..<5 MHz from f_{CRX}.	Without external filter	35			dB_C
BI_{5MHz}[2]	Blocking immunity 5..<10 MHz from f_{CRX}.	Without external filter	50			dB_C
BI_{10MHz}[2]	Blocking immunity @ ≥10 MHz from f_{CRX}.	Without external filter	60			dB_C
P_{LOL}	Leakage LO power @ f_{CRX} available between the RF+ and RF- pins.	LO power in a differentially matching source resistor as load with LNA in high or low gain mode			-60	dBm

Standard Receive Quality (SRQ): Bit Error Rate (BER) ≤10-3 at a RX data rate of 10 kbit/s.

SRQ fulfilled with: Useful signal applied 3 dB above the measured sensitivity limit, however not below -97 dBm. Blocking signal un-modulated CW. This measurement method is slightly more restrictive than the EN 300 220-1 v1.3.1 section 9.3.2 for class 2 receivers due to they are related to the nominal received carrier position instead of the band edges.

7.6 Timing Parameters

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
R_{DATA}	3 wire interface data rate				3	Mbit/s
f_{CLOCK}	3 wire interface clock frequency				6	MHz
T_{XTON}	XO turn on time	WAKEUP → 1 to XO defined running			1	ms
Transmit/receive switching time						
T_{RXTX}	Receive to transmit data switching time	Falling edge on RXTXN pin to accepting input of first transmit data bit at TRXDAT (as input)			500	µs
T_{TXRX}	Transmit to receive data switching time	Rising edge on RXTXN pin to TRXDAT = output			500	µs
Transmitter						
T_{TXON}	Transmitter startup time	XO running			1000	µs
T_{WTO}	Wakeup timeout after WAKEUP → 0	Time for button scanning and turn off delay for CMT	1			ms
T_{POR}	Power-On-Reset duration		2		10	ms
Receiver						
T_{RXON}	Receiver startup time	XO running			1000	µs
T_{D1}	Delay for Signal identification / AFC operation start				4	µs
T_{SIAFC}	Signal identification / AFC duration	Given by µC	0,2	4 to 8 T_{BIT}	10	ms
T_{D2}	SI/AFC reaction delay	internal calculation and reaction times			50	µs
$T_{REL,0}$	Receiver relaxation time	From end of strong interference to receiver full sensitivity at low AC coupling cutoff frequency.			450	µs
$T_{REL,1}$	Receiver relaxation time	From end of strong interference to receiver full sensitivity at high AC coupling cutoff frequency.			150	µs
T_{RXOF}	Receiver turn off time	From WAKEUP → 0 no reception possible			0	µs

7.7 Digital Pin Characteristics

TA = 23 °C, VDD = 3,0 V, unless specified otherwise. GND is the 0 V reference.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENABLE (input), CLOCK (input) RXTXN (input), SI/AFC (input)						
VIH	High level input voltage		0,7 VDD	-		V
VIL	Low level input voltage			-	0,3 VDD	V
IIH	High level input current	VIH = VDD			1	µA
IIL	Low level input current	VIL = 0 V	-1			µA
SIGID (output)						
VOH	High level output voltage	IOH = -1 mA	VDD-0,5			V
VOL	Low level output voltage	IOL = 1 mA			0,5	V
tr	Rise time	CLoad = 10 pF		20		ns
tf	Fall time	CLoad = 10 pF		20		ns
MCCLK (output)						
VOH	High level output voltage	IOH = -1 mA	VDD-0,5	-		V
VOL	Low level output voltage	IOL = 1 mA		-	0,5	V
tr	Rise time	CLoad = 10 pF		20		ns
tf	Fall time	CLoad = 10 pF		20		ns
jcc	Cycle to cycle jitter				+/-5	%
TRXDAT (input / output), DATA (input / output) WAKEUP (input / output)						
VIH	High level input voltage		0,7 VDD	-		V
VIL	Low level input voltage			-	0,3 VDD	V
IIH	High level input current	VIH= VDD			1	µA
IIL	Low level input current	VIL = 0 V	-1			µA
VOH	High level output voltage	IOH = -1 mA	VDD-0,5	-		V
VOL	Low level output voltage	IOL = 1 mA		-	0,5	V
tr	Rise time	CLoad = 10 pF		20		ns
tf	Fall time	CLoad = 10 pF		20		ns
XTAL (if used as reference frequency input)						
VIH	High level input voltage		VDD-0,5	-		V
VIL	Low level input voltage			-	0,5	V
IIH	High level input current	VIH = VDD			1	µA
IIL	Low level input current	VIL =0 V	-1			µA

8 Pin Description

Pin	Name	Type	Dir.	Description
1	AVDD	Sup	Sup	Analog VDD
2	RFVDD	Sup	Sup	RF VDD.
3	RFGND	Sup	Sup	RF GND
4	RF	RF	I/O	LNA input/PA output
5	RFX	RF	I/O	LNA input/PA output
6	RFGND	Sup	Sup	RF GND
7	RESET	A	I/O	Power On Reset
8	RXTXN	D	I	RX / TX selection (RXTXN = 1 is RX).
9	SIAFC	D	I	Signal Identification / Automatic Frequency Control
10	SIGID	D	O	RX SIGnal IDentified.
11	TRXDAT	D	I/O	Tx DAT input Rx DATa output
12	WAKEUP	D	I	power down=0
13	DVDD	Sup	Sup	Digital VDD.
14	XTALOUT	A	O	XO output.
15	XTALIN	A	I	XO input.
16	DGND	Sup	Sup	Digital GND.
17	MCCLK	D	O	Microcontroller CLocK output.
18	CLOCK	D	I	CLOCK for serial interface.
19	DATA	D	I/O	Configuration DATA input and status DATA output.
20	ENABLE	D	I	ENABLE serial interface.
21	AGND	Sup	Sup	Analog GND.
22	AVDD	Sup	Sup	Analog VDD
23	ASKNFSK	D	I	ASK/FSK selection (ASKNFSK=1 is ASK)
24	SL_CAP	A	I/O	Analog Signal
25	V_CTRL	A	I/O	Analog Test (PLL TEST)
26	RSSI	A	I/O	Analog OUTPUT
27	Q_OUT	A	I/O	Analog Test
28	I_OUT	A	I/O	Analog Test

9 Package Information

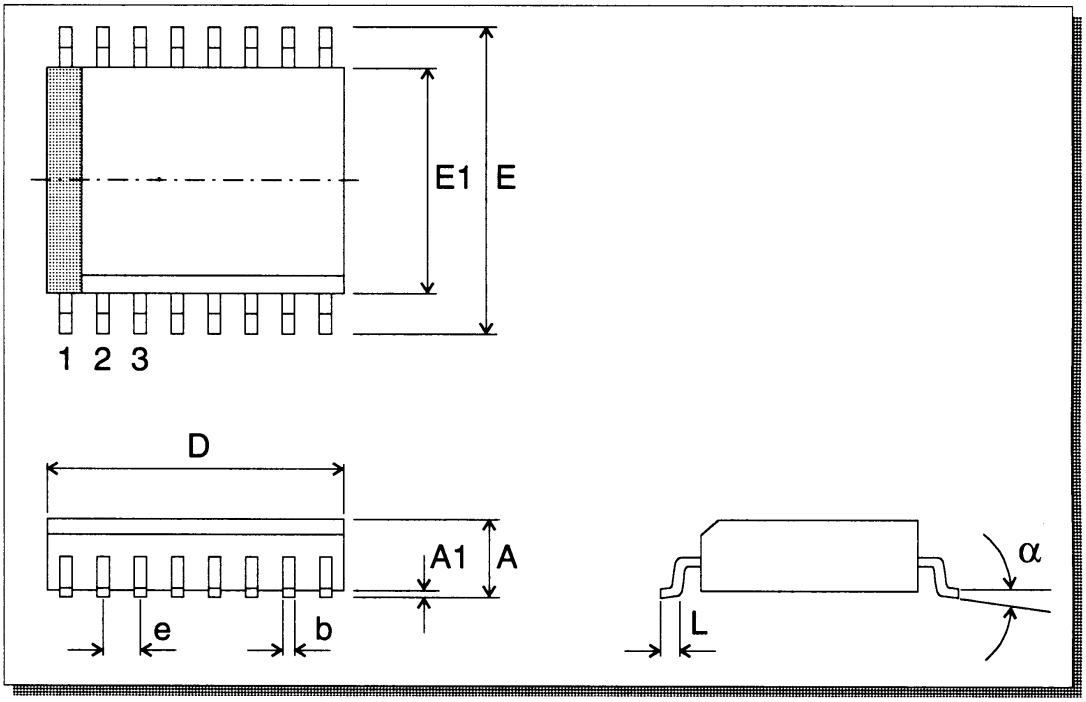

Figure 11: Physical dimensions of TSSOP-28.

Symbol	Common Dimensions		
	Minimal (mm/mil)	**Nominal (mm/mil)**	**Maximal (mm/mil)**
A	-	-	1,10/0,0433
A1	0,05/0,002	0,10/0,004	0,15/0,006
b	0,19/0,0075	-	0,30/0,0118
D		7,80/0,307	
e		0,65 BSC	
E	6,25/0,246	6,40/0,252	6,50/0,256
E1	4,30/0,169	4,40/0,173	4,50/0,177
0	0,50/0,020	0,60/0,024	0,70/0,028
α	0°	4°	8°

Table 10: Package dimensions.

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