PRELIMINARY

FastEdge™ Series
CY2DP3120

1:20 Differential Clock Buffer/Driver

Features

- **Twenty ECL/PECL differential outputs**
- **Two ECL-/PECL-/HSTL-compatible differential clock inputs**
- **Hot-swappable/-insertable**
- **50-ps output-to-output skew**
- **500-ps device-to-device skew**
- **Less than 10-ps intrinsic jitter**
- **< 500-ps propagation delay (typical)**
- **Operation from DC to 1.5 GHz**
- **PECL mode supply range: V_{CC} = 2.375V to 3.465V with V_{EE} = 0V**
- **ECL mode supply range: V_{EE} = –2.375V to –3.465V with V_{CC} = 0V**
- **Industrial temperature range: –40°C to 85°C**
- **52-pin 1.4-mm TQFP package**
- **Temperature compensation like 100K ECL**

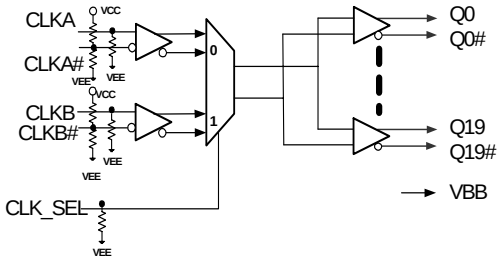
Description

The CY2DP3120 is a low-skew, low propagation delay 1-to-20 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 1.5 GHz.

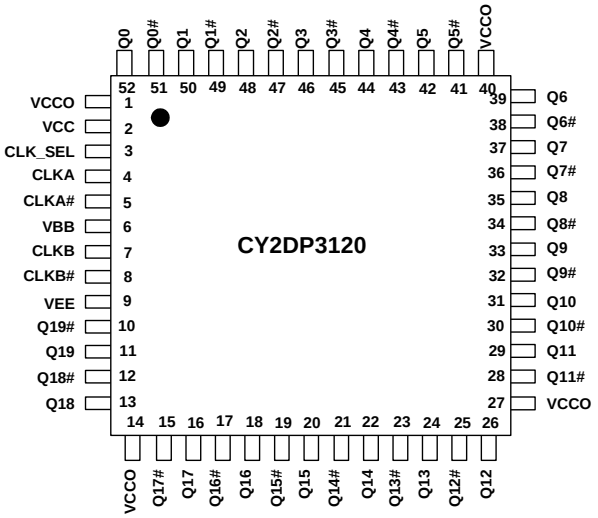
The device is fully differential and features two reference input buffers. The CY2DP3120 may function not only as a differential clock buffer but also as a signal level translator and fanout distributing a single-ended signal to twenty ECL/PECL differential loads. An external bias pin, VBB, is provided for an ECL/PECL/HSTL single-ended or differential. In such an application, the VBB pin should be connected to either one of the CLKA# or CLKB# inputs and bypassed to VCC via a 0.01-µF capacitor. Traditionally, in ECL, it is used to provide the reference level to a receiving single ended input that might have a different self bias point.

Since the CY2DP3120 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2DP3120 delivers consistent, guaranteed performance over differing platforms.

Block Diagram



Pin Configuration



Pin Description

Pin	Name	I/O	Type	Description
4,5	CLKA, CLKA#	I,PD[1] I,PC	ECL/PECL	**Default differential clock input pair**
7,8	CLKB, CLKB#	I,PD I,PC	HSTL	**Alternate differential clock input pair**
3	CLK_SEL	I,PD	ECL/PECL	**CLK – Mux select**
52,50,48,46,44,42,39,37,35,33,31,29,26,24,22,20,18,16,13,11	Q[0-19]	O,OS	ECL/PECL	**True output**
51,49,47,45,43,41,38,36,34,32,30,28,25,23,21,19,17,15,12,10	Q#[0-19]	O,OS	ECL/PECL	**Complement output**
6	VBB[3]	O	Bias	**Reference voltage output for single-ended ECL or PECL operation**
9	VEE[2]	-PWR	Power	**Power supply, negative connection**
2	VCC	+PWR	Power	**Power supply, positive connection**
1,14,27,40	VCCO	+PWR	Power	**Power supply, positive connection**

Governing Agencies

The following agencies provide specifications that apply to the CY2DP3120. The agency name and relevant specification is listed below.

Agency Name	Specification
JEDEC	JESD 51 (Theta JA) JESD 8–2 (ECL) JESD 65–A (Skew,Jitter) JESD 8-6 (HSTL)
IEEE	1596.3 (Jitter Specs)
UL	94 (Moisture Grading)
Mil–Spec	883E Method 1012.1 (Thermal Theta JC)

Notes:

1. In the I/O column, the following notation is used: I = Input, O = Output, PD = Pull-down, PU = Pull-up, PC = Pull Center, O = Output, OS = Open Source, PWR = Power.
2. in ECL mode (negative power supply mode), VEE is either –3.3V or –2.5V and VCC is connected to GND(0V). In PECL mode (positive power supply mode), VEE is connected to GND(0V) and VCC is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (VCC) and are between VCC and VEE.
3. VBB is available for use for single ended bias mode when VCC is +3.3V.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{cc}	Supply Voltage	Non-functional	–0.3	3.6	VDC
V_{cc}	Operating Voltage	Functional	2.5 – 5%	3.3 + 5%	VDC
V_{BB}	Output Reference Voltage	Relative to V_{CC}	V_{CC}–1.525	Vcc–1.325	VDC
I_{BB}	Output Reference Current	Relative to V_{BB}		200	uA
V_{TT}	Output Termination Voltage	V_{TT} = 0V for V_{CC} = 2.5V		VCC–2	VDC
V_{IN}	Input Voltage	Relative to V_{CC}	–0.3	V_{CC}+0.3	VDC
V_{OUT}	Output Voltage	Relative to V_{CC}	–0.3	V_{CC}+0.3	VDC
LU_I	Latch-up Immunity	Functional	300		mA
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
T_J	Temperature, Junction	Functional	10	+110	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Functional	TBD		°C/W
$Ø_{Ja}$	Dissipation, Junction to Ambient	Functional	TBD		°C/W
ESD_h	ESD Protection (Human Body Model)		2000		V
M_{SL}	Moisture Sensitivity Level		TBD		N.A.
G_{ATES}	Total Functional Gate Count	Assembled Die	50		Ea.
UL–94	Flammability Rating	@1/8 in	V–0		N.A.
FIT	Failure in Time	Manufacturing Test	TBD		PPM

PECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{IL}	Input Voltage, Low		V_{CC}–1.945	V_{CC}–1.625	V
V_{IH}	Input Voltage, High	Define VCC and Load Current	V_{CC}–1.165	V_{CC}–0.880	V
I_{IN}	Input Current[4]	V_{IN} = V_{IL} or V_{IN} = V_{IH}		200	uA
Clock input pair CLKA, CLKA#,CLKB, CLKB# (PECL Differential Signals)					
V_{PP}	Differential Input Voltage[5]	Differential Operation	0.1	1.3	V
V_{CMR}	Differential Cross Point Voltage[6]	Differential Operation	1.2	V_{CC}	V
I_{IN}	Input Current[4]	V_{IN} = V_{IL} or V_{IN} = V_{IH}		200	uA
PECL Outputs Q0-Q19, (Q0-Q19)#(PECL Differential Signals)					
V_{OH}	Output High Voltage	I_{OH} = –30 mA[9], 50Ω Load	V_{CC}–1.145	V_{CC}–0.895	V
V_{OL}	Output Low Voltage V_{CC} = 3.3V ±5%V_{CC} = 2.5V ±5%	I_{OL} = –5 ma[9],50Ω Load	V_{CC}–1.945 V_{CC} –1.945	V_{CC}–1.695 V_{CC}–1.695	V
Clock Input Pair CLKA, CLKA#,CLKB, CLKB# (HSTL Differential Signals)					
V_{DIF}	Differential Input Voltage[7]		0.4	1.9	V
V_X	Differential Cross Point Voltage[8]		0.68	0.9	V
I_{IN}	Input Current	Vin = Vx ± 0.2V		200	uA

Notes:

4. Input have internal pullup / pulldown or biasing resistors which affect the input current.
5. VPP (DC) is the minimum differential input voltage swing required to maintain device functionality.
6. VCMR (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the VCMR (DC) range and the input swing lies within the VPP (DC) specification.
7. VDIF (DC) is the amplitude of the differential HSTL input voltage swing required for device functionality.
8. VX (DC) is the crosspoint of the differential HSTL input signal. Functional operations is obtained when the crosspoint is within the VX (DC) range and the input swing lies within the VPP (DC) specification.
9. Equivalent to a termination of 50 Ω to VTT.

PECL DC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
Supply Current and VBB					
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current[10]	VEE Pin		130	mA
V_{BB}	Output Reference Voltage	I_{BB} = 200 uA	V_{CC}–1.525	V_{CC}–1.325	V
I_{pup}	Internal Pull-up Current		TBD	TBD	mA.
I_{pdwn}	Internal Pull-down Current		TBD	TBD	mA.
C_{IN}	Input Pin Capacitance		TBD	TBD	pF
C_{OUT}	Output Pin Capacitance	Q0–Q19, (Q0–Q19)#	TBD	TBD	pF
L_{IN}	Pin Inductance		TBD	TBD	nH
Z_{OUT}	Output Impedance	Q0–Q19, (Q0–Q19)#	TBD	TBD	Ω

ECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{IL}	Input Voltage, Low		–1.945	–1.625	V
V_{IH}	Input Voltage, High		–1.165	–0.880	V
I_{IN}	Input Current[11]	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$		200	uA
Clock input pair CLKA, CLKA#,CLKB, CLKB# (ECL Differential Signals)					
V_{PP}	Differential Input Voltage[12]	Differential Operation	0.1	1.3	V
V_{CMR}	Differential Cross Point Voltage[13]	Differential Operation	V_{EE}+1.2	0	V
I_{IN}	Input Current[11]	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$		200	uA
ECL Outputs Q0-Q19, (Q0-Q19)# (ECL Dfferential Signals)					
V_{OH}	Output High Voltage	I_{OH} = –30 mA[14]	–1.145	–0.895	V
V_{OL}	Output Low Voltage V_{EE} = –3.3V ±5% V_{EE} = –2.5V ±5%	I_{OL} = –5 ma[14]	–1.945 –1.945	–1.695 –1.695	V
Supply Current and VBB					
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current[15]	V_{EE} Pin		130	mA
V_{BB}	Output Reference Voltage	I_{BB} = 200 uA	–1.525	–1.325	V

Notes:

10. ICC calculation: ICC = (number of differential output pairs used) x (IOH + IOL) + IEE or ICC = (number of differential output pairs used) x (VOH – VTT)/Rload + (VOL – VTT)/Rload +IEE.
11. Input have internal pull-up/pull-down or biasing resistors which affect the input current.
12. VPP (DC) is the minimum differential input voltage swing required to maintain device functionality.
13. VCMR (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the VCMR (DC) range and the input swing lies within the VPP (DC) specification.
14. Equivalent to a termination of 50Ω to VTT.
15. ICC Calculation: ICC = (number of differential output pairs used) x (IOH + IOL) + IEE or ICC = (number of differential output pairs used) x (VOH – VTT)/Rload + (VOL – VTT)/Rload +IEE.

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Clock Input Pair CLKA, CLKA (PECL or ECL Differential Signals)					
V_{PP}	Differential Input Voltage[17]	Differential Operation	0.1	1.3	V
V_{CMR}	Differential Cross Point Voltage[18]	Differential Operation	V_{EE}+1.2	0	V
F_{CLK}	Input Frequency[19]	50% Duty Cycle Standard Load		1,500	MHz
T_{PD}	Propagation Delay CLKA or CLKB to Q0–Q9 Pair	660 MHz 50% Duty Cycle Standard Load Differential Operation	400	750	ps
Clock Input Pair CLKB, CLKB (HSTL Differential Signals)					
V_{PP}	Differential Input Voltage[17]	Differential Operation	0.1	1.3	V
V_{CMR}	Differential Cross Point Voltage[18]	Differential Operation	V_{EE}+1.2	0	V
F_{CLK}	Input Frequency[19]	50% Duty Cycle Standard Load		1,500	MHz
T_{PD}	Propagation Delay CLKA or CLKB to Q0–Q9 Pair	660 MHz 50% Duty Cycle Standard Load Differential Operation	400	750	ps
ECL/PECL Clock Outputs (Q0–19, Q#0–19) (Differential)					
$Vo_{(P-P)}$	Differential Output Voltage (Peak-to-Peak)	Differential PRBS fo < 50 MHz fo < 0.8 GHz fo < 1.0 GHz	0.45 0.4 0.375		V
$tsk_{(O)}$	Output-to-Output skew	660-MHz 50% Duty Cycle Standard Load Differential Operation		50	ps
$tsk_{(PP)}$	Output-to-output skew (part-to-part)	660-MHz 50% Duty Cycle Standard Load Differential Operation		500	ps
$T_{jitt(cc)}$	Output cycle-to-cycle jitter (Intrinsic)	660-MHz 50% Duty Cycle Standard Load Differential Operation		10	ps r.m.s
tsk(P)	Output pulse skew[21]	660-MHz 50% Duty Cycle Standard Load Differential Operation			ps
T_F, T_F	Output Rise/Fall time	660-MHz 50% Duty Cycle Differential 20% to 80%		0.3	ns
TTB	Total Timing Budget	660-MHz 50% Duty Cycle Standard Load			ps

Notes:

16. AC characteristics apply for parallel output termination of 50Ω to VTT.
17. VPP (AC) is the minimum differential ECL/PECL input swing required to maintain AC characteristics including tpd and device-to-device skew.
18. VCMR (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the VCMR(AC) range and the input swing lies within the VPP(AC) specification. Violation of VCMR(AC) or VPP(AC) impacts the device propagation delay, device and part-to-part skew.
19. The CY2DP3120 is fully operation up to 1.5 GHz.
20. VX(AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the VX(AC) range and the input swing lies within the VDIF(AC) specification. Violation of VX(AC) or VDIF(AC) impacts the device propagation delay, device and part-to-part skew.
21. Output pulse skew is the absolute difference of the propagation delay times: | tPLH – tPHL |.

Test Configurations

Standard test load using a differential pulse generator and differential measurement instrument.

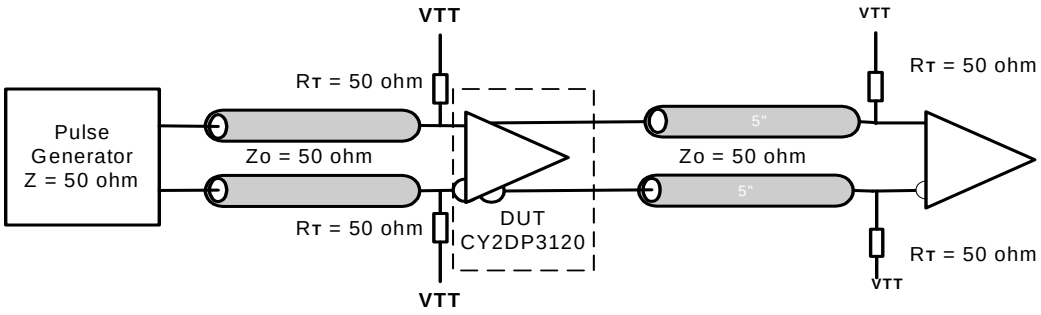


Figure 1. CY2DP3120 AC Test Reference

Timing Definitions

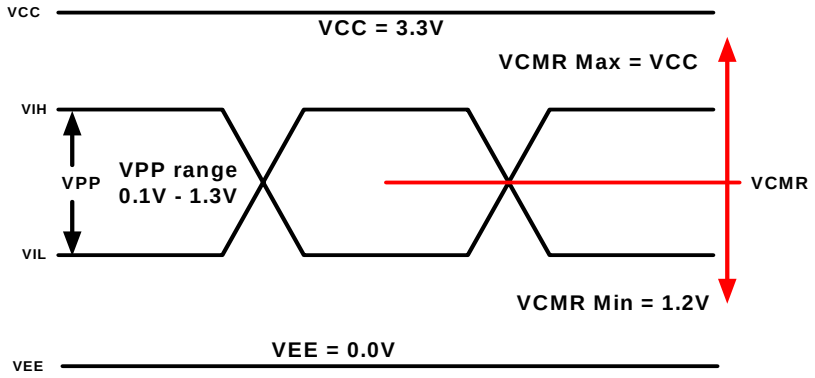


Figure 2. PECL Waveform Definitions

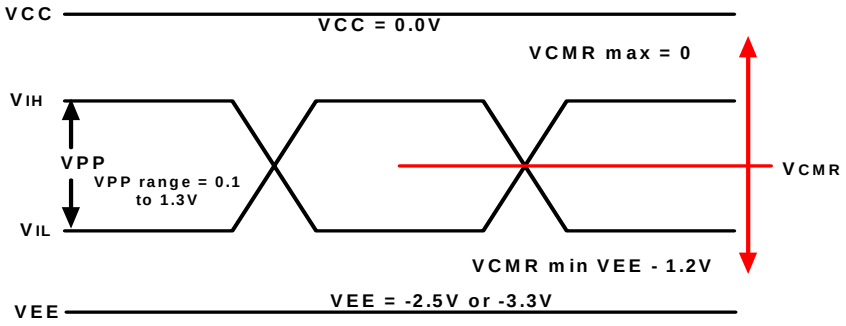


Figure 3. PECL Waveform Definitions

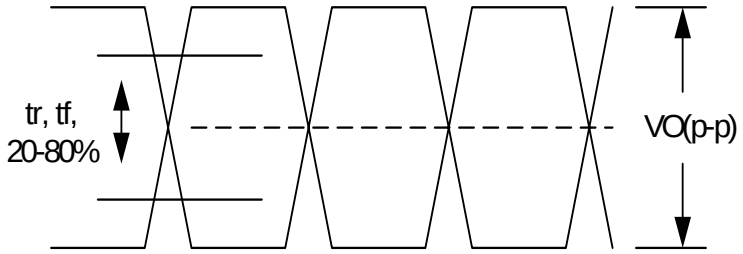


Figure 4. ECL/LVPECL Output

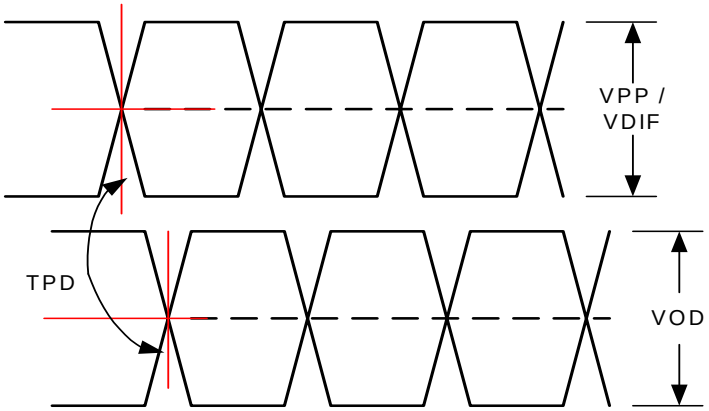
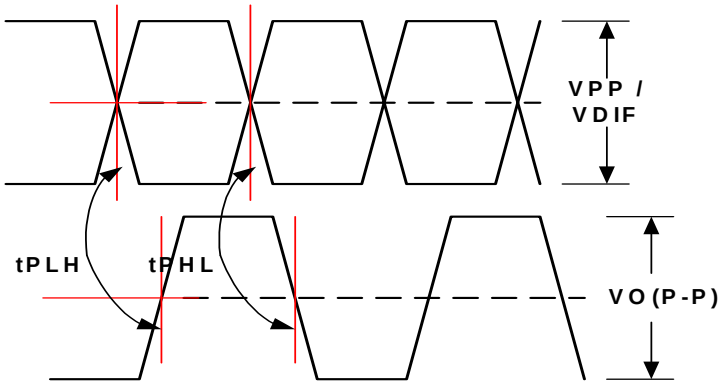


Figure 5. TPD Propagation Delay of Both CLKA or CLKB to (Q0–Q19),Q0#–Q0#19 Pair PECL/ECL/HSTL to PECL/ECL



tsk(P) Output pulse skew
= | tPLH - tPHL |

Figure 6. Output Pulse Skew

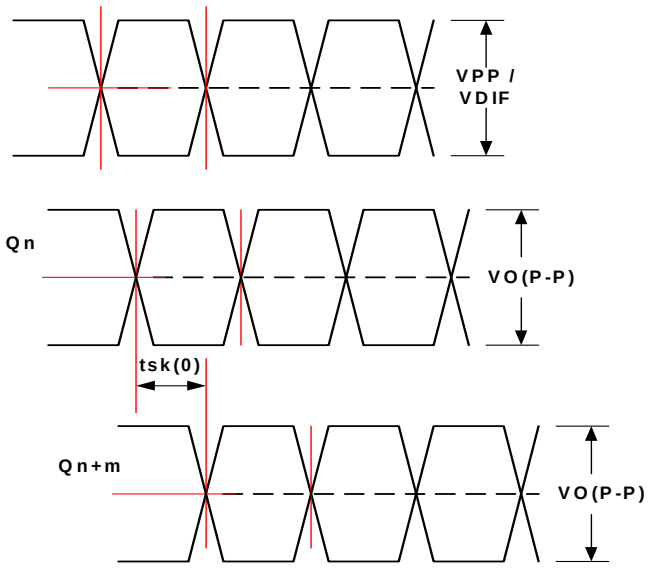


Figure 7. Output to Output Skew

Applications Information

Termination Examples

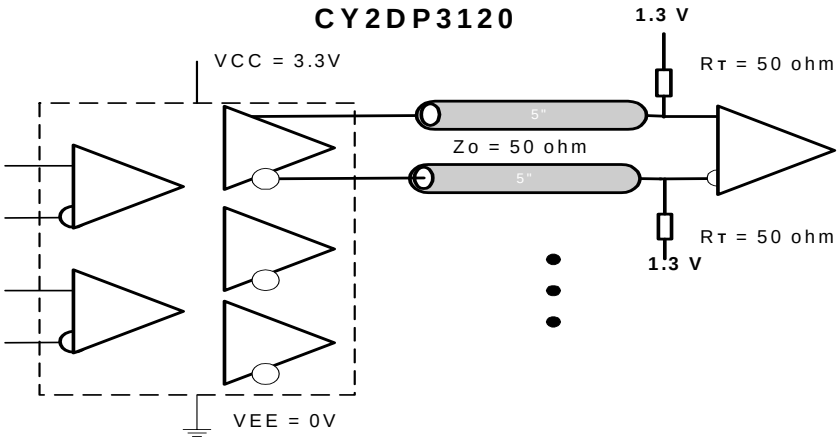


Figure 8. Standard LVPECL – PECL Output Termination

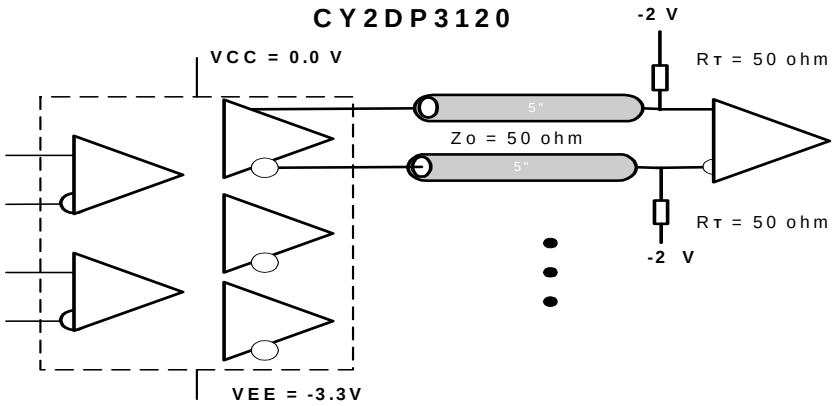


Figure 9. Standard ECL Output Termination

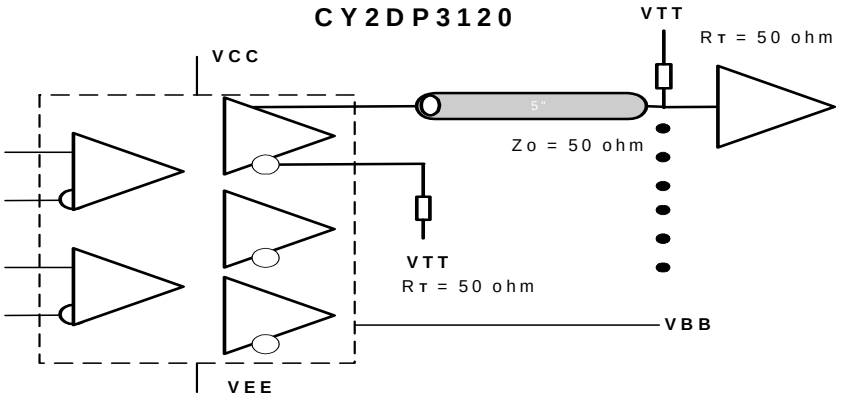


Figure 10. Driving a PECL/ECL Single-Ended Input

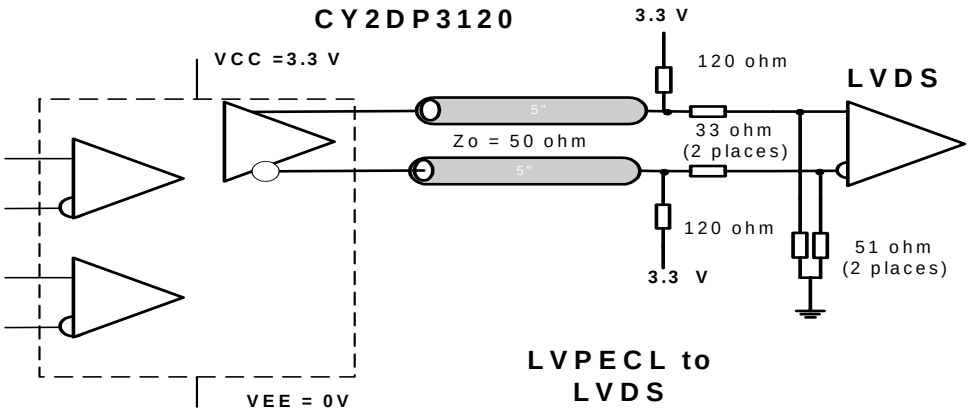


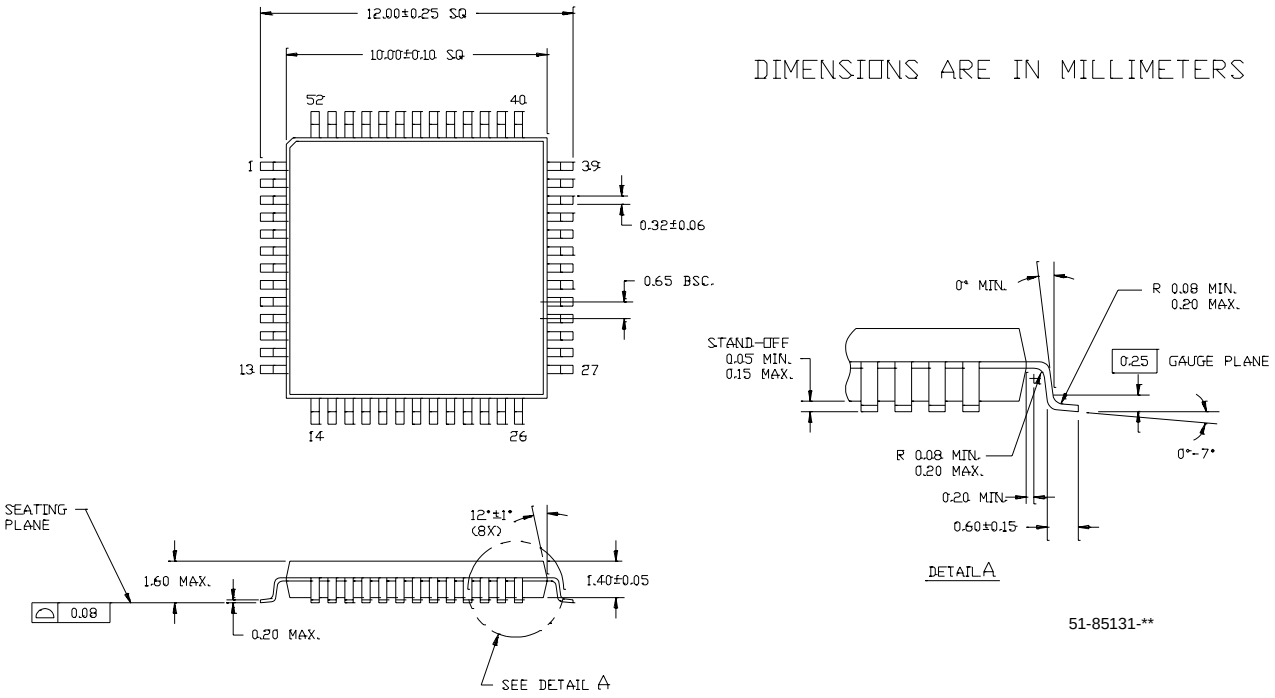
Figure 11. Low-Voltage Positive Emitter-Coupled Logic (LVPECL) to a Low-Voltage Differential Signaling (LVDS) Interface

Ordering Information

Part Number	Package Type	Product Flow
CY2DP3120AI	52-pin TQFP	Industrial, –40° to 85°C
CY2DP3120AIT	52-pin TQFP – Tape and Reel	Industrial, –40° to 85°C

Package Diagram

52-lead Thin Plastic Quad Flat Pack (10 × 10 × 1.4 mm) A52



Document History Page

Document Title: CY2DP3120 FastEdge™ Series 1:20 Differential Clock Buffer/Driver Document Number: 38-07514				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	122438	12/05/02	RGL	New data sheet
*A	125457	04/17/03	RGL	Corrected typo Q14 to Q4 in pin 44 in the pin configuration diagram Changed pin #s 1,14,27 and 40 from VCC to VCCO Changed title to FastEdge™ Series 1:20 Differential Clock Buffer/Driver