



DT2042-01CSP

LOW CAPACITANCE UNIDIRECTIONAL TVS DIODE

Product Summary

V _{BR} Min	I _{PP} Max	C _{IN} Typ
6V	6.5A	0.8pF

Description

This new generation TVS is designed to protect sensitive electronics from the damage due to ESD. The combination of small size and high ESD surge capability makes it ideal for use in portable applications such as cellular phones, digital cameras and MP3 players.

Applications

- Cellular Handsets
- Portable Electronics
- · Computers and Peripheral

Features

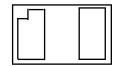
- Provides ESD Protection per IEC 61000-4-2 Standard: Air ±20kV, Contact ±20kV
- Provides ESD Protection per IEC 61000-4-4 Standard: 40A (tp = 5/50ns)
- 1 Channel of ESD Protection
- Low Channel Input Capacitance
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

Mechanical Data

- Case: X3-DSN1006-2 (Type B)
- Case Material: Chip Scale Package
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: NiAu Bump. Solderable per MIL-STD-202, Method 208
 (4)
- Weight: 0.001 grams (Approximate)

X3-DSN1006-2 (Type B)







Top View

Bottom View

Device Schematic

Ordering Information (Note 4)

Part Number	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DT2042-01CSP-7B	Standard	MQ	7	8	10,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/

Marking Information

MQ

MQ = Product Type Marking Code Line Denotes Pin 1



Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Power Dissipation	P_PP	50	W	8/20µs (See Figure 1)
Peak Pulse Current	I _{PP}	6.5	Α	8/20µs (See Figure 1)
ESD Protection – Air Discharge	V _{ESD_AIR}	20	kV	IEC 61000-4-2 Standard
ESD Protection – Contact Discharge	V _{ESD_CONTACT}	20	kV	IEC 61000-4-2 Standard

Thermal Characteristics

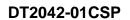
Characteristic	Symbol	Value	Unit
Package Power Dissipation (Note 5)	P_{D}	250	mW
Thermal Resistance, Junction to Ambient (Note 5)	$R_{ heta JA}$	500	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-65 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

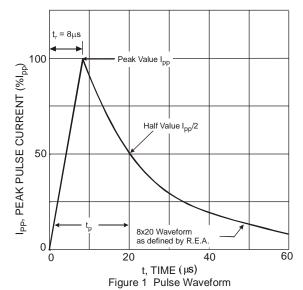
Characteristic	Symbol	Min	Тур	Max	Unit	Test Conditions
Reverse Standoff Voltage	V_{RWM}	_	_	5	V	_
Channel Leakage Current (Note 6)	I _{RM}	_	_	0.5	μΑ	V _{RWM} = 5V
Breakdown Voltage	V_{BR}	6	_	10	V	I _R = 10mA
Clamping Voltage Desitive Transients	V _{CL}	_	7.0	_	V	$I_{PP} = 1A$, $t_P = 8/20 \mu s$
Clamping Voltage, Positive Transients		VCL	_	7.4	_	V
Differential Resistance	R _{DYN}	_	0.2	_	Ω	ITLP = 1A to 10A, t _P = 100ns, I/O to GND
Channel Input Capacitance	C _{IN}	_	0.8	_	pF	V _R = 0V, f = 1MHz

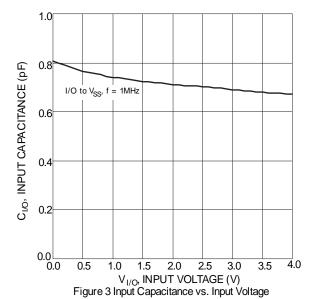
Notes: 5. Device mounted on FR-4 PCB pad layout (2oz copper) per Diodes Incorporated's recommended pad layout, refer to http://www.diodes.com/package-outlines.html.

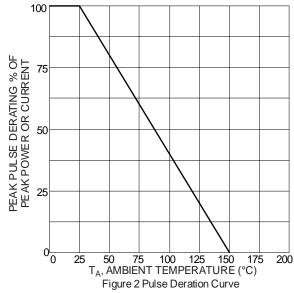
^{6.} Short duration pulse test used to minimize self-heating effect.

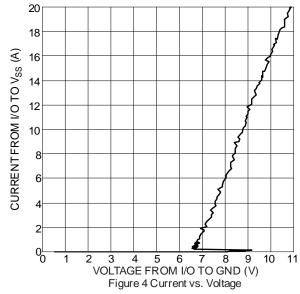










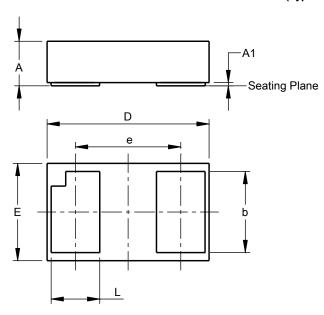




Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X3-DSN1006-2 (Type B)

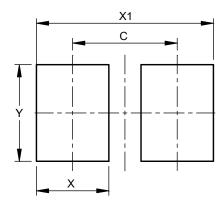


X3-DSN1006-2 (Type B)				
Dim	Min	Max	Тур	
Α	0.250	0.300	0.275	
A1	0.00	0.02	0.01	
b	0.490	0.510	0.500	
D	0.975	1.025	1.00	
Е	0.575	0.625	0.600	
е			0.650	
L	0.290	0.310	0.300	
All Dimensions in mm				

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X3-DSN1006-2 (Type B)



Dimensions	Value (in mm)		
С	0.65		
Х	0.45		
X1	1.10		
Υ	0.60		

Note 7: Device side walls are electrically active bare silicon. Avoid contact of solder or flux on the side walls during the PCB assembly process.



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