Clock Recovery and Data Retiming Phase-Locked Loop

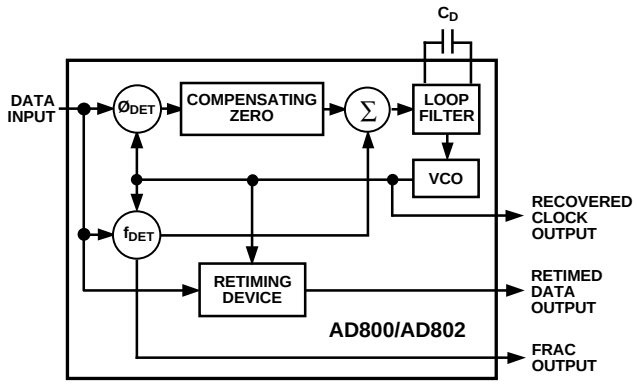
AD800/AD802

FEATURES

Standard Products
- **44.736 Mbps—DS-3**
- **51.84 Mbps—STS-1**
- **155.52 Mbps—STS-3 or STM-1**

Accepts NRZ Data, No Preamble Required
Recovered Clock and Retimed Data Outputs
Phase-Locked Loop Type Clock Recovery—No Crystal Required
Random Jitter: 20° Peak-to-Peak
Pattern Jitter: Virtually Eliminated
10KH ECL Compatible
Single Supply Operation: –5.2 V or +5 V
Wide Operating Temperature Range: –40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD800 and AD802 employ a second order phase-locked loop architecture to perform clock recovery and data retiming on Non-Return to Zero, NRZ, data. This architecture is capable of supporting data rates between 20 Mbps and 160 Mbps. The products described here have been defined to work with standard telecommunications bit rates. 45 Mbps DS-3 and 52 Mbps STS-1 are supported by the AD800-45 and AD800-52 respectively. 155 Mbps STS-3 or STM-1 are supported by the AD802-155.

Unlike other PLL-based clock recovery circuits, these devices do not require a preamble or an external VCXO to lock onto input data. The circuit acquires frequency and phase lock using two control loops. The frequency acquisition control loop initially acquires the clock frequency of the input data. The phase-lock loop then acquires the phase of the input data, and ensures that the phase of the output signals track changes in the phase of the input data. The loop damping of the circuit is dependent on the value of a user selected capacitor; this defines jitter peaking performance and impacts acquisition time. The devices exhibit 0.08 dB jitter peaking, and acquire lock on random or scrambled data within 4×10^5 bit periods when using a damping factor of 5.

During the process of acquisition the frequency detector provides a Frequency Acquisition (FRAC) signal which indicates that the device has not yet locked onto the input data. This signal is a series of pulses which occur at the points of cycle slip between the input data and the synthesized clock signal. Once the circuit has acquired frequency lock no pulses occur at the FRAC output.

The inclusion of a precisely trimmed VCO in the device eliminates the need for external components for setting center frequency, and the need for trimming of those components. The VCO provides a clock output within ±20% of the device center frequency in the absence of input data.

The AD800 and AD802 exhibit virtually no pattern jitter, due to the performance of the patented phase detector. Total loop jitter is 20° peak-to-peak. Jitter bandwidth is dictated by mask programmable fractional loop bandwidth. The AD800, used for data rates < 90 Mbps, has been designed with a nominal loop bandwidth of 0.1% of the center frequency. The AD802, used for data rates in excess of 90 Mbps, has a loop bandwidth of 0.08% of center frequency.

All of the devices operate with a single +5 V or –5.2 V supply.

REV. B

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AD800/AD802–SPECIFICATIONS

(V_{EE} = V_{MIN} to V_{MAX}, V_{CC} = GND, T_A = T_{MIN} to T_{MAX}, Loop Damping Factor = 5, unless otherwise noted)

Parameter[1]	Condition	AD800-45BQ Min	AD800-45BQ Typ	AD800-45BQ Max	AD800-52BR Min	AD800-52BR Typ	AD800-52BR Max	AD802-155KR/BR Min	AD802-155KR/BR Typ	AD802-155KR/BR Max	Units
NOMINAL CENTER FREQUENCY			44.736			51.84			155.52		MHz
OPERATING TEMPERATURE	K Grade							0		70	°C
RANGE (T_{MIN} to T_{MAX})	B Grade	–40		85	–40		85	–40		85	°C
TRACKING RANGE		43		45.5	49		53	155		156	Mbps
CAPTURE RANGE		43		45.5	49		53	155		156	Mbps
STATIC PHASE ERROR	ρ = 1, T_A = +25°C, V_{EE} = –5.2 V		2	10		2	10		14	30	Degrees
	ρ = 1		3	11.5		3	11.5		18	37	Degrees
RECOVERED CLOCK SKEW	t_{RCS} (Figure 1)	0.2	0.6	1	0.2	0.6	1	0.2	0.8	1	ns
SETUP TIME	t_{SU} (Figure 1)							2.06	2.37		ns
TRANSITIONLESS DATA RUN				240			240			240	Bit Periods
OUTPUT JITTER	ρ = 1		2			2			3.5		Degrees rms
	2^7–1 PRN Sequence		2.5	4.7		2.5	4.7		5.4	9.7	Degrees rms
	2^{23}–1 PRN Sequence		2.5	4.7		2.5	4.7		5.4	9.7	Degrees rms
JITTER TOLERANCE	f = 10 Hz		2,500			2,500			3,000		Unit Intervals
	f = 2.3 kHz	6.5									Unit Intervals
	f = 30 kHz	0.47									Unit Intervals
	f = 1 MHz	0.47									Unit Intervals
	f = 30 Hz				830						Unit Intervals
	f = 300 Hz				83						Unit Intervals
	f = 2 kHz				7.4						Unit Intervals
	f = 20 kHz				0.47						Unit Intervals
	f = 6.5 kHz							2.0	7.6		Unit Intervals
	f = 65 kHz							0.26	0.9		Unit Intervals
JITTER TRANSFER											
Damping Factor											
Capacitor, C_D											
ζ = 1, Nominal			8.2			6.8			2.2		nF
ζ = 5, Nominal			0.22			0.15			0.047		µF
ζ = 10, Nominal			0.82			0.68			0.22		µF
Peaking											
ζ = 1, Nominal	T_A = +25°C, V_{EE} = –5.2 V		2			2			2		dB
ζ = 5, Nominal	T_A = +25°C, V_{EE} = –5.2 V		0.08			0.08			0.08		dB
ζ = 10, Nominal	T_A = +25°C, V_{EE} = –5.2 V		0.02			0.02			0.02		dB
Bandwidth			45			52			130		kHz
ACQUISITION TIME											
ρ = 1/2	ζ = 1		1×10^4			1×10^4			1.5×10^4		Bit Periods
T_A = +25°C	ζ = 5		3×10^5	8×10^5		3×10^5	8×10^5		4×10^5	8×10^5	Bit Periods
V_{EE} = –5.2 V	ζ = 10		8×10^5			8×10^5			1.4×10^6		Bit Periods
POWER SUPPLY											
Voltage (V_{MIN} to V_{MAX})	T_A = +25°C	–4.5	–5.2	–5.5	–4.5	–5.2	–5.5	–4.5	–5.2	–5.5	Volts
Current	T_A = +25°C, V_{EE} = –5.2 V		125	170		125	170		140	180	mA
				180			180			205	mA
INPUT VOLTAGE LEVELS	T_A = +25°C										
Input Logic High, V_{IH}		–1.084		–0.72	–1.084		–0.72	–1.084		–0.72	Volts
Input Logic Low, V_{IH}		–1.95		–1.594	–1.95		–1.594	–1.95		–1.594	Volts
OUTPUT VOLTAGE LEVELS	T_A = +25°C										
Output Logic High, V_{OH}		–1.084		–0.72	–1.084		–0.72	–1.084		–0.72	Volts
Output Logic Low, V_{OL}		–1.95		–1.60	–1.95		–1.60	–1.95		–1.60	Volts
INPUT CURRENT LEVELS	T_A = +25°C										
Input Logic High, I_{IH}				125			125			125	µA
Input Logic Low, I_{IL}				80			80			80	µA
OUTPUT SLEW TIMES	T_A = +25°C										
Rise Time (t_R)	20%–80%		0.75	1.5		0.75	1.5		0.75	1.5	ns
Fall Time (t_F)	80%–20%		0.75	1.5		0.75	1.5		0.75	1.5	ns
SYMMETRY	ρ = 1/2, T_A = +25°C										
Recovered Clock Output	V_{EE} = –5.2 V	45		55	45		55	45		55	%

NOTES

[1]Refer to Glossary for parameter definition.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –6 V
Input Voltage (Pin 16 or Pin 17 to V_{CC}) . . . . V_{EE} to +300 mV
Maximum Junction Temperature
SOIC Package . . . . . +150°C
Ceramic DIP Package . . . . . +175°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C
ESD Rating
AD800 . . . . . 1500 V
AD802 . . . . . 1000 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to an absolute maximum rating condition for an extended period may adversely affect device reliability.

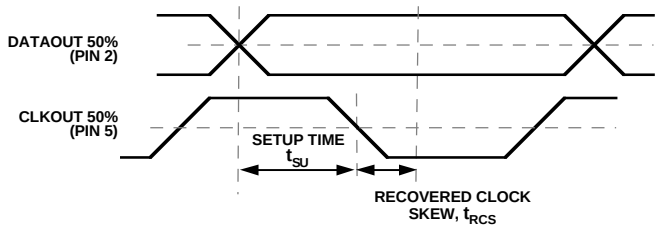


Figure 1. Recovered Clock Skew and Setup (See Previous Page)

PIN DESCRIPTIONS

Number	Mnemonic	Description
1	$\overline{\text{DATAOUT}}$	Differential Retimed Data Output
2	DATAOUT	Differential Retimed Data Output
3	V_{CC2}	Digital Ground
4	$\overline{\text{CLKOUT}}$	Differential Recovered Clock Output
5	CLKOUT	Differential Recovered Clock Output
6	V_{EE}	Digital V_{EE}
7	V_{EE}	Digital V_{EE}
8	V_{CC1}	Digital Ground
9	AV_{EE}	Analog V_{EE}
10	ASUBST	Analog Substrate
11	CF_2	Loop Damping Capacitor Input
12	CF_1	Loop Damping Capacitor Input
13	AV_{CC}	Analog Ground
14	V_{CC1}	Digital Ground
15	V_{EE}	Digital V_{EE}
16	DATAIN	Differential Data Input
17	$\overline{\text{DATAIN}}$	Differential Data Input
18	SUBST	Digital Substrate
19	$\overline{\text{FRAC}}$	Differential Frequency Acquisition Indicator Output
20	FRAC	Differential Frequency Acquisition Indicator Output

THERMAL CHARACTERISTICS

	θ_{JC}	θ_{JA}
SOIC Package	22°C/W	75°C/W
Cerdip Package	25°C/W	90°C/W

Use of a heatsink may be required depending on operating environment.

GLOSSARY

Maximum and Minimum Specifications
Maximum and minimum specifications result from statistical analyses of measurements on multiple devices and multiple test systems. Typical specifications indicate mean measurements. Maximum and minimum specifications are calculated by adding or subtracting an appropriate guardband from the typical specification. Device-to-device performance variation and test system-to-test system variation contribute to each guardband.

Nominal Center Frequency
This is the frequency that the VCO will operate at with no input signal present and the loop damping capacitor, C_D, shorted.

Tracking Range
This is the range of input data rates over which the PLL will remain in lock.

Capture Range
This is the range of input data rates over which the PLL can acquire lock.

Static Phase Error
This is the steady-state phase difference, in degrees, between the recovered clock sampling edge and the optimum sampling instant, which is assumed to be halfway between the rising and falling edges of a data bit. Gate delays between the signals that define static phase error, and IC input and output signals prohibit direct measurement of static phase error.

Data Transition Density, ρ
This is a measure of the number of data transitions, from "0" to "1" and from "1" to "0," over many clock periods. ρ is the ratio ($0 \le \rho \le 1$) of data transitions to clock periods.

Jitter
This is the dynamic displacement of digital signal edges from their long term average positions, measured in degrees rms, or Unit Intervals (UI). Jitter on the input data can cause dynamic phase errors on the recovered clock sampling edge. Jitter on the recovered clock causes jitter on the retimed data.

Output Jitter
This is the jitter on the retimed data, in degrees rms, due to a specific pattern or some psuedo-random input data sequence (PRN Sequence).

Jitter Tolerance
Jitter tolerance is a measure of the PLL's ability to track a jittery input data signal. Jitter on the input data is best thought of as phase modulation, and is usually specified in unit intervals.

ORDERING GUIDE

Device	Center Frequency	Fractional Loop Bandwidth	Description	Operating Temperature	Package Option
AD800-45BQ	44.736 MHz	0.1%	20-Pin Cerdip	–40°C to +85°C	Q-20
AD800-52BR	51.84 MHz	0.1%	20-Pin Plastic SOIC	–40°C to +85°C	R-20
AD802-155BR	155.52 MHz	0.08%	20-Pin Plastic SOIC	–40°C to +85°C	R-20
AD802-155KR	155.52 MHz	0.08%	20-Pin Plastic SOIC	0°C to +70°C	R-20

The PLL must provide a clock signal which tracks this phase modulation in order to accurately retime jittered data. In order for the VCO output to have a phase modulation which tracks the input jitter, some modulation signal must be generated at the output of the phase detector (see Figure 21). The modulation output from the phase detector can only be produced by a phase error between the data input and the clock input. Hence, the PLL can never perfectly track jittered data. However, the magnitude of the phase error depends on the gain around the loop. At low frequencies the integrator provides very high gain, and thus very large jitter can be tracked with small phase errors between input data and recovered clock. At frequencies closer to the loop bandwidth, the gain of the integrator is much smaller, and thus less input jitter can be tolerated. The PLL data output will have a bit error rate less than 1×10^{-10} when in lock and retiming input data that has the specified jitter applied to it.

Jitter Transfer
The PLL exhibits a low-pass filter response to jitter applied to its input data.

Bandwidth
This describes the frequency at which the PLL attenuates sinusoidal input jitter by 3 dB.

Peaking
This describes the maximum jitter gain of the PLL in dB.

Damping Factor, ζ
ζ describes how the PLL will track an input signal with a phase step. A greater value of ζ corresponds to less overshoot in the PLL response to a phase step. ζ is a standard constant in second order feedback systems.

Acquisition Time
This is the transient time, measured in bit periods, required for the PLL to lock on input data from its free-running state.

Symmetry
Symmetry is calculated as (100 × on time)/period, where on time equals the time that the clock signal is greater than the midpoint between its "0" level and its "1" level.

Bit Error Rate vs. Signal-to-Noise Ratio
The AD800 and AD802 were designed to operate with standard ECL signal levels at the data input. Although not recommended, smaller input signals are tolerable. Figure 8, 14, and 20 show the bit error rate performance versus input signal-to-noise ratio for input signal amplitudes of full 900 mV ECL, and decreased amplitudes of 80 mV and 20 mV. Wideband amplitude noise is summed with the data signals as shown in Figure 2. The full ECL and 80 mV signals give virtually indistinguishable results. The 20 mV signals also provide adequate performance when in lock, but signal acquisition may be impaired.

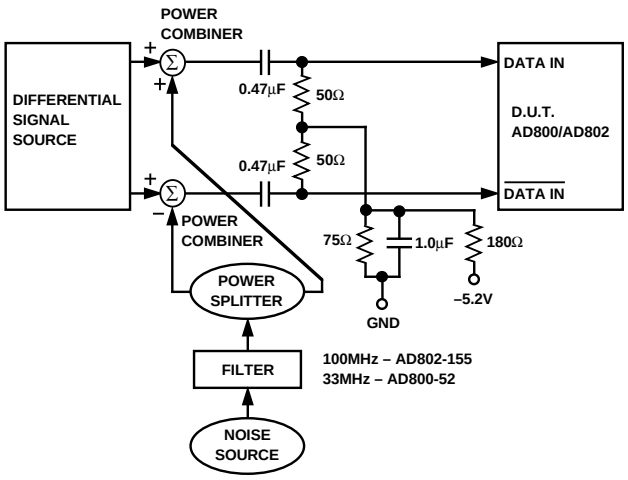


Figure 2. Bit Error Rate vs. Signal-to-Noise Ratio Test: Block Diagram

USING THE AD800 AND THE AD802 SERIES

Ground Planes
Use of one ground plane for connections to both analog and digital grounds is recommended. Output signal sensitivity to power supply noise (PECL configuration, Figure 22) is less using one ground plane than when using separate analog and digital ground planes.

Power Supply Connections
Use of a 10 μF tantalum capacitor between V_{EE} and ground is recommended.

Use of 0.1 μF ceramic capacitors between IC power supply or substrate pins and ground is recommended. Power supply decoupling should take place as close to the IC as possible. Refer to schematics, Figure 22 and Figure 26, for advised connections.

Sensitivity of IC output signals (PECL configuration, Figure 22) to high frequency power supply noise (at 2 × the nominal data rate) can be reduced through the connection of signals AV_{CC} and V_{CC1}, and the addition of a bypass network. The type of bypass network to consider depends on the noise tolerance required. The more complex bypass network schemes tolerate greater power supply noise levels. Refer to Figures 23 and 24 for bypassing schemes and power supply sensitivity curves.

Transmission Lines
Use of 50 Ω transmission lines are recommended for DATAIN, CLKOUT, DATAOUT, and FRAC signals.

Terminations
Termination resistors should be used for DATAIN, CLKOUT, DATAOUT, and FRAC signals. Metal, thick film, 1% tolerance resistors are recommended. Termination resistors for the DATAIN signals should be placed as close as possible to the DATAIN pins.

Connections from V_{EE} to lead resistors for DATAIN, DATAOUT, FRAC, and CLKOUT signals should be individual, not daisy chained. This will avoid crosstalk on these signals.

Loop Damping Capacitor, C_D
A ceramic capacitor may be used for the loop damping capacitor.

Input Buffer
Use of an input buffer, such as a 10H116 Line Receiver IC, is suggested for an application where the DATAIN signals do not come directly from an ECL gate, or where noise immunity on the DATAIN signals is an issue.

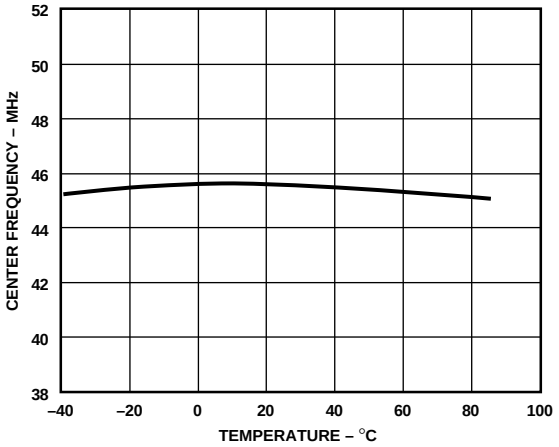


Figure 3. AD800-45 Center Frequency vs. Temperature

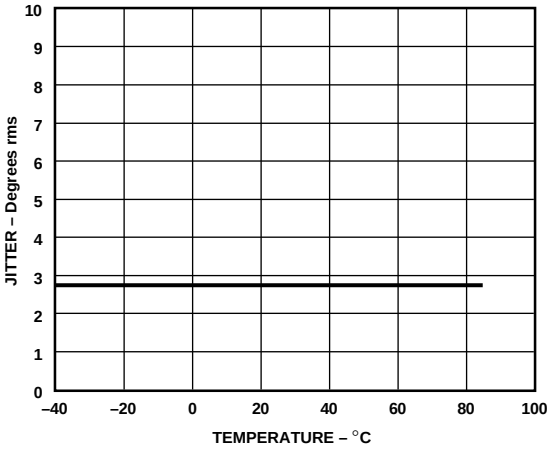


Figure 4. AD800-45 Jitter vs. Temperature

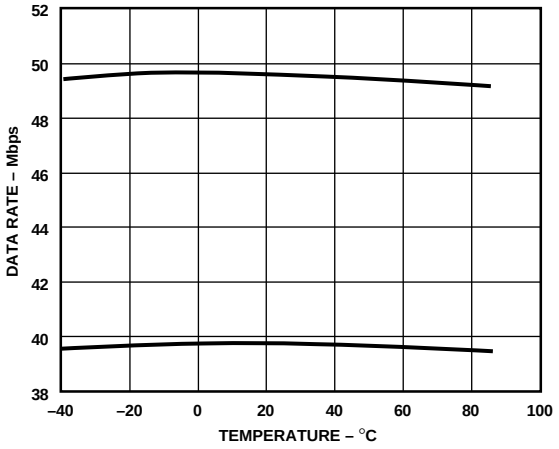


Figure 5. AD800-45 Capture and Tracking Range vs. Temperature

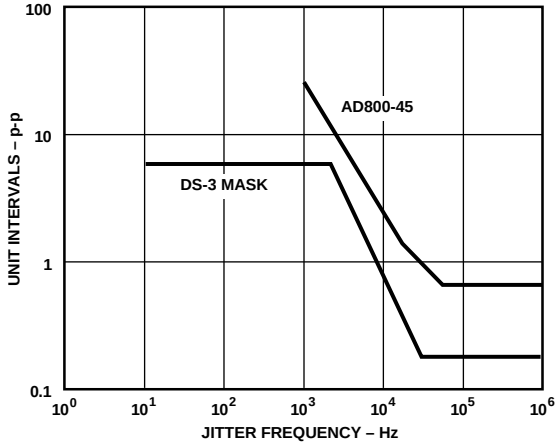


Figure 6. AD800-45 Jitter Tolerance

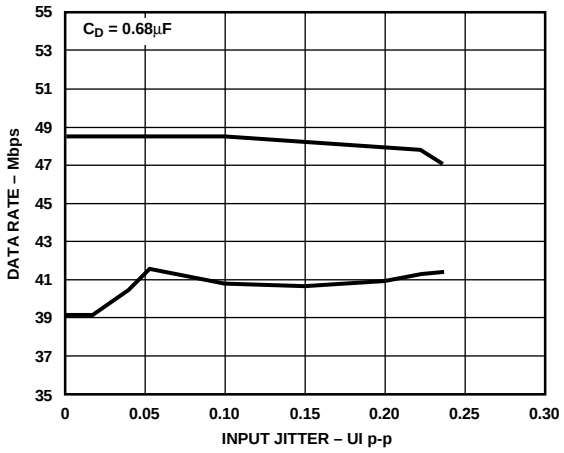


Figure 7. AD800-45 Acquisition Range vs. Input Jitter

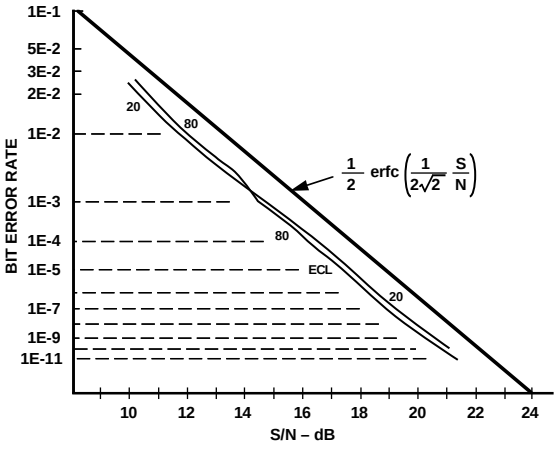


Figure 8. AD800-45 Bit Error Rate vs. Input Jitter

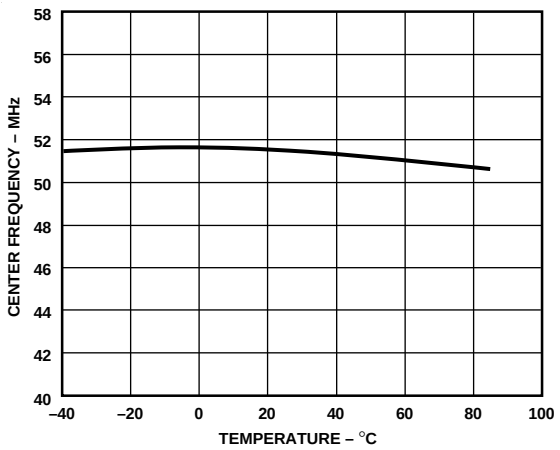


Figure 9. AD800-52 Center Frequency vs. Temperature

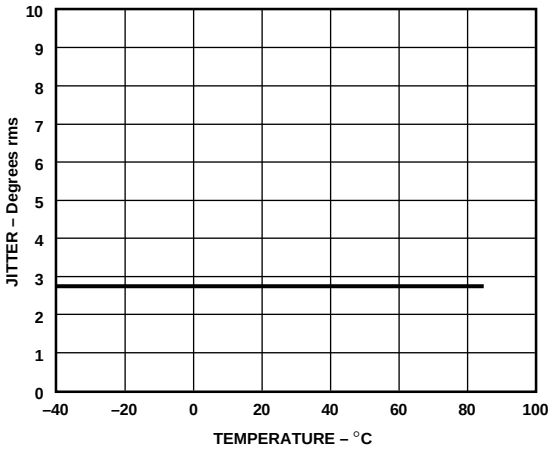


Figure 10. AD800-52 Jitter vs. Temperature

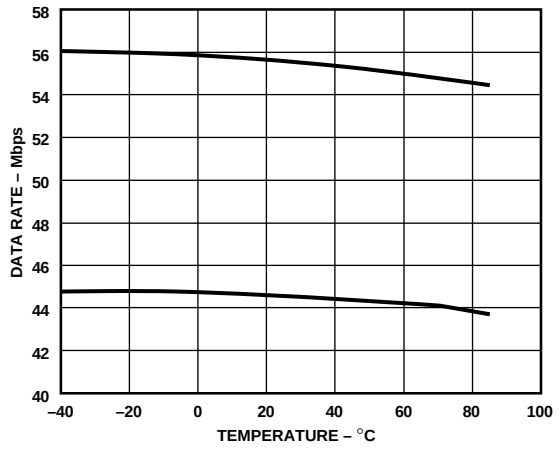


Figure 11. AD800-52 Capture and Tracking Range vs. Temperature

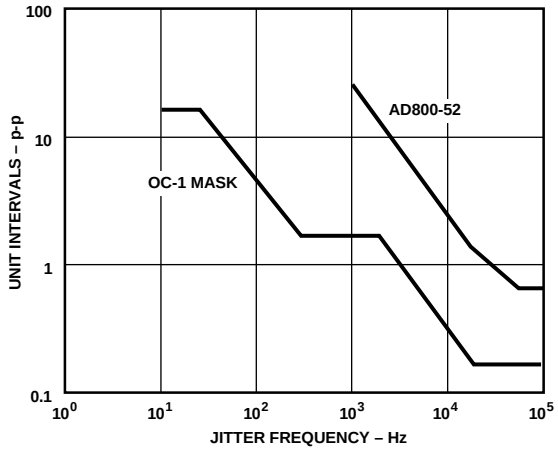


Figure 12. AD800-52 Jitter Tolerance

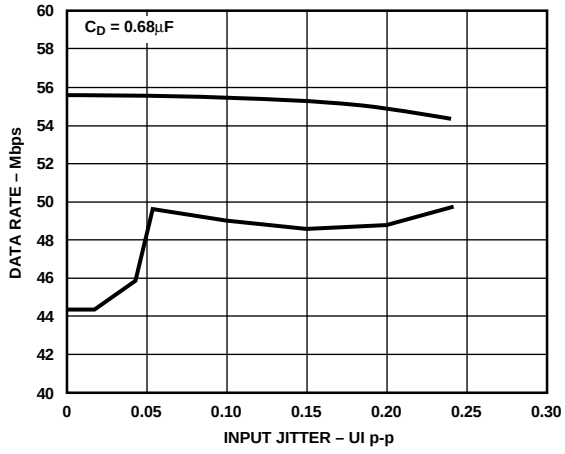


Figure 13. AD800-52 Acquisition Range vs. Input Jitter

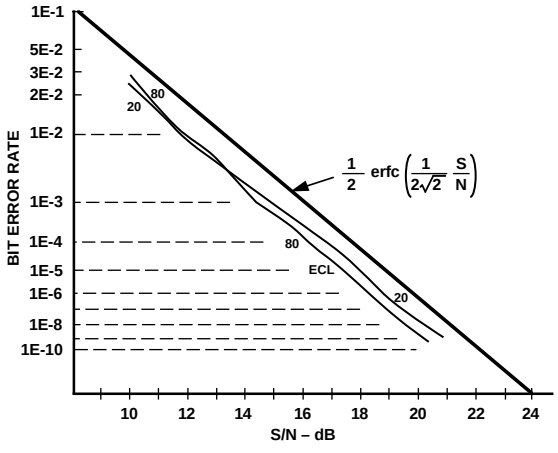


Figure 14. AD800-52 Bit Error Rate vs. Input Jitter

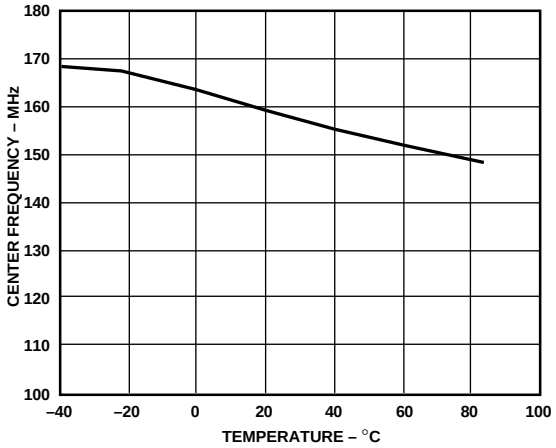


Figure 15. AD802-155 Center Frequency vs. Temperature

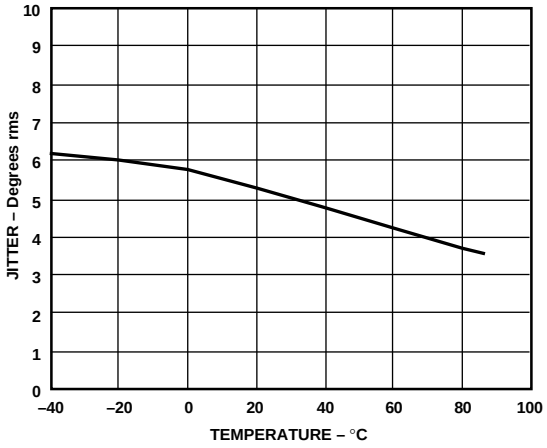


Figure 16. AD802-155 Output Jitter vs. Temperature

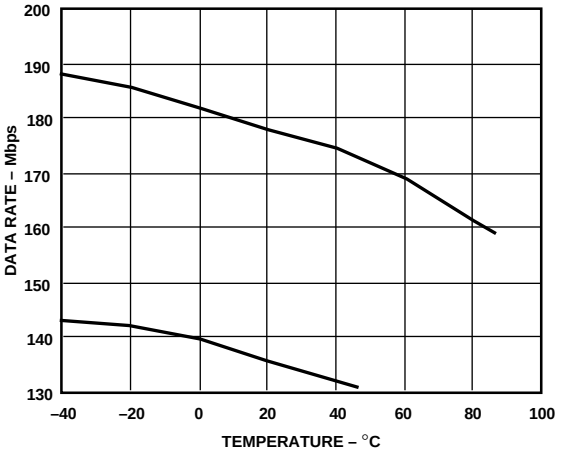


Figure 17. AD802-155 Capture Range, Tracking Range vs. Temperature

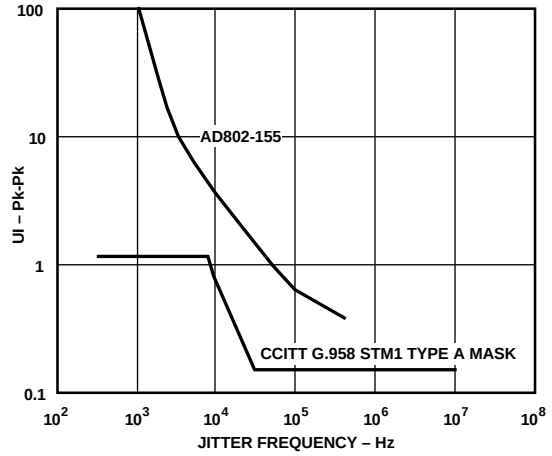


Figure 18. AD802-155 Jitter Tolerance

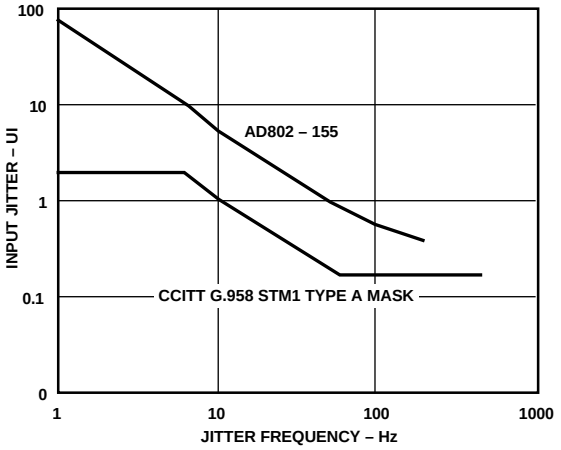


Figure 19. AD802-155 Minimum Acquisition Range vs. Jitter Frequency, T_{MIN} to T_{MAX} V_{MIN} to V_{MAX}

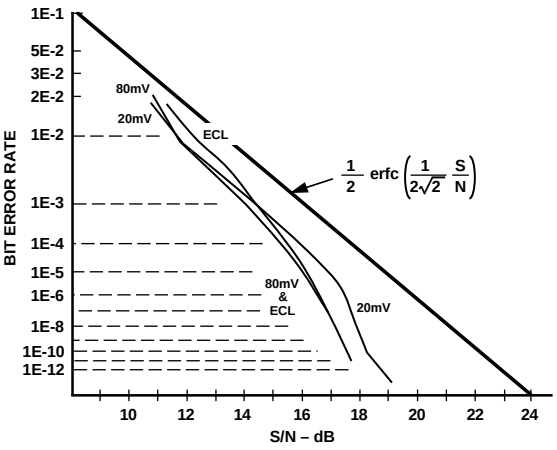


Figure 20. AD802-155 Bit Error Rate vs. Input Jitter

THEORY OF OPERATION

The AD800 and AD802 are phase-locked loop circuits for recovery of clock from NRZ data. The architecture uses a frequency detector to aid initial frequency acquisition, refer to Figure 21 for a block diagram. Note the frequency detector is always in the circuit. When the PLL is locked, the frequency error is zero and the frequency detector has no further effect. Since the frequency detector is always in circuit, no control functions are needed to initiate acquisition or change mode after acquisition. The frequency detector also supplies a frequency acquisition (FRAC) output to indicate when the loop is acquiring lock. During the frequency acquisition process the FRAC output is a series of pulses of width equal to the period of the VCO. These pulses occur on the cycle slips between the data frequency and the VCO frequency. With a maximum density (1010 . . .) data pattern, every cycle slip will produce a pulse at FRAC. However, with random data, not every cycle slip produces a pulse. The density of pulses at FRAC increases with the density of data transitions. The probability that a cycle slip will produce a pulse increases as the frequency error approaches zero. After the frequency error has been reduced to zero, the FRAC output will have no further pulses. At this point the PLL begins the process of phase acquisition, with a settling time of roughly 2000 bit periods. Valid retimed data can be guaranteed by waiting 2000 bit periods after the last FRAC pulse has occurred.

Jitter caused by variations of density of data transitions (pattern jitter) is virtually eliminated by use of a new phase detector (patented). Briefly, the measurement of zero phase error does not cause the VCO phase to increase to above the average run rate set by the data frequency. The jitter created by a 2^7–1 pseudo-random code is 1/2 degree, and this is small compared to random jitter.

The jitter bandwidth for the AD802-155 is 0.08% of the center frequency. This figure is chosen so that sinusoidal input jitter at 130 kHz will be attenuated by 3 dB. The jitter bandwidths of the AD800-45 and AD800-52 are 0.1% of the respective center frequencies. The jitter bandwidth of the AD800 or the AD802 is mask programmable from 0.01% to 1% of the center frequency. A device with a very low loop bandwidth (0.01% of the center frequency) could effectively filter (clean up) a jittery timing reference. Consult the factory if your application requires a special loop bandwidth.

The damping ratio of the phase-locked loop is user programmable with a single external capacitor. At 155 MHz a damping ratio of 10 is obtained with a 0.22 µF capacitor. More generally, the damping ratio scales as $1.7 \times \sqrt{f_{DATA} \times C_D}$. At 155 MHz a damping ratio of 1 is obtained with a 2.2 nF capacitor. A lower damping ratio allows a faster frequency acquisition; generally the acquisition time scales directly with the capacitor value. However, at damping ratios approaching one, the acquisition time no longer scales directly with the capacitor value. The acquisition time has two components: frequency acquisition and phase acquisition. The frequency acquisition always scales with capacitance, but the phase acquisition is set by the loop bandwidth of the PLL and is independent of the damping ratio. Thus, the 0.08% fractional loop bandwidth sets a minimum acquisition time of 15,000 bit periods. Note the acquisition time for a damping factor of 1 is specified as 15,000 bit periods. This comprises 13,000 bit periods for frequency acquisition and 2,000 periods for phase acquisition. Compare this to the 400,000 bit periods acquisition time specified for a damping ratio of 5; this consists entirely of frequency acquisition, and the 2,000 bit periods of phase acquisition is negligible.

While lower damping ratio affords faster acquisition, it also allows more peaking in the jitter transfer response (jitter peaking). For example, with a damping ratio of 10 the jitter peaking is 0.02 dB, but with a damping factor of 1, the peaking is 2 dB.

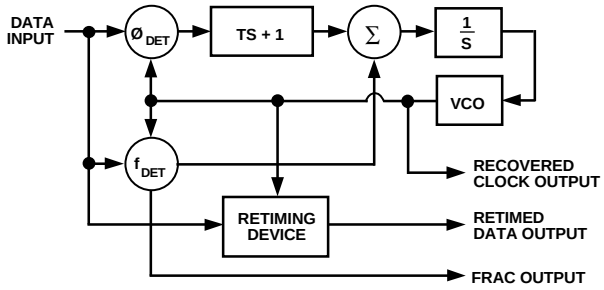


Figure 21. AD800 and AD802 Block Diagram

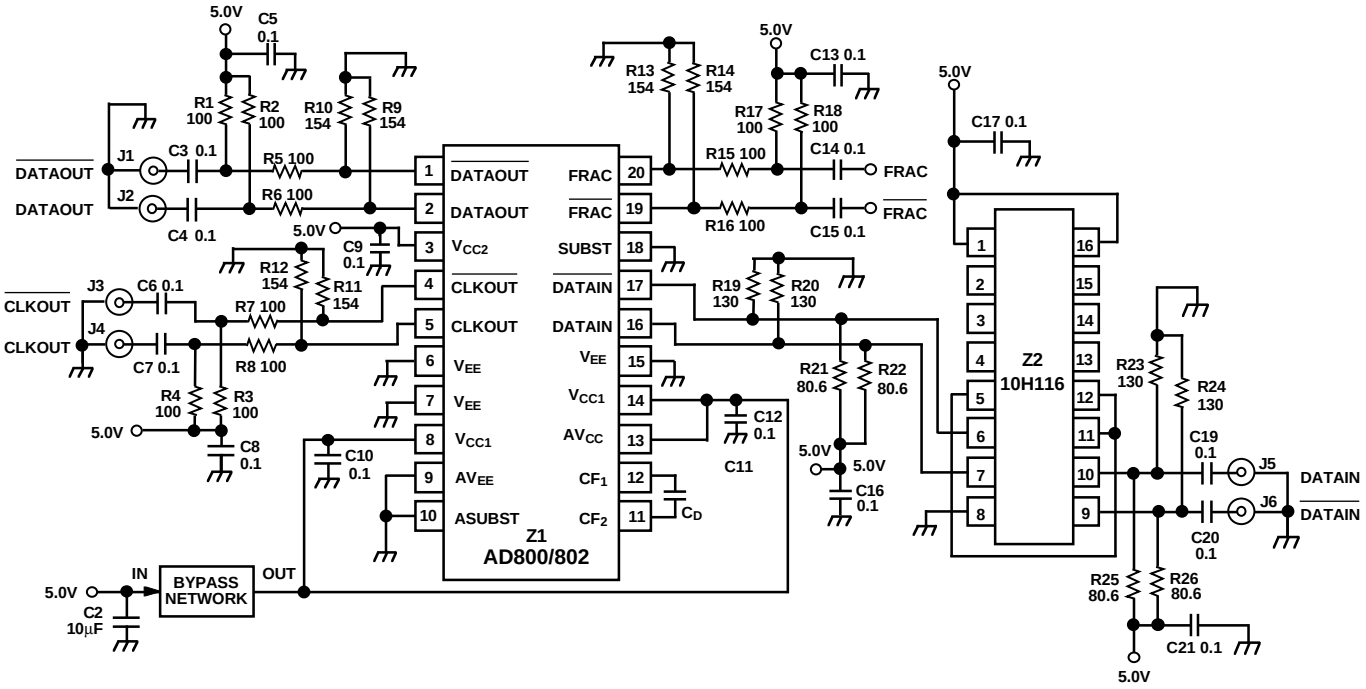


Figure 22. Evaluation Board Schematic, Positive Supply

Table I. Evaluation Board, Positive Supply: Components List

Reference Designator	Description	Quantity
R1–8, R15–18	Resistor, 100 Ω, 1%	12
R9–14	Resistor, 154 Ω, 1%	6
R19, 20, 23, 24	Resistor, 130 Ω, 1%	4
R21, 22, 25, 26	Resistor, 80.6 Ω, 1%	4
C_D	Capacitor, Loop Damping (See Specifications Page)	1
C2	Capacitor, 10 μF, Tantalum	1
C3–C21	Capacitor, 0.1 μF, Ceramic Chip	17
Z1	AD800/AD802	1
Z2	10H116, ECL Line Receiver	1

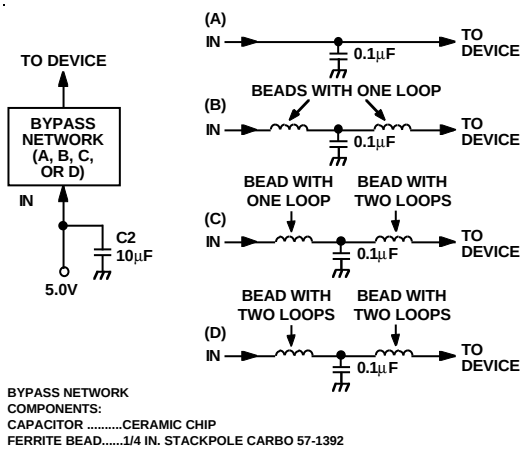


Figure 23. Bypass Network Schemes

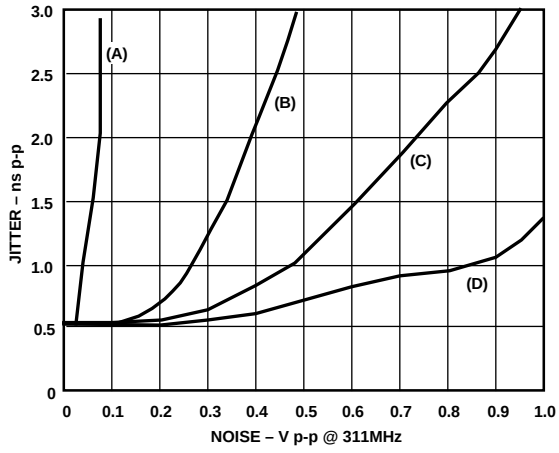


Figure 24. AD802-155 Output Jitter vs. Supply Noise (PECL Configuration)

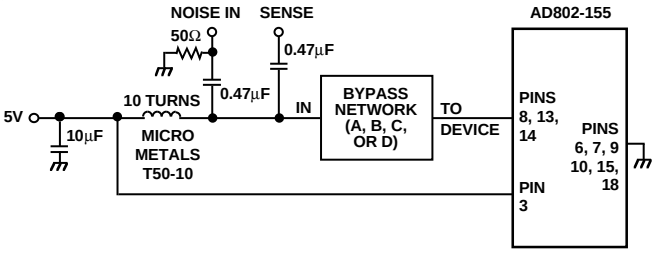


Figure 25. Power Supply Noise Sensitivity Test Circuit, PECL Configuration

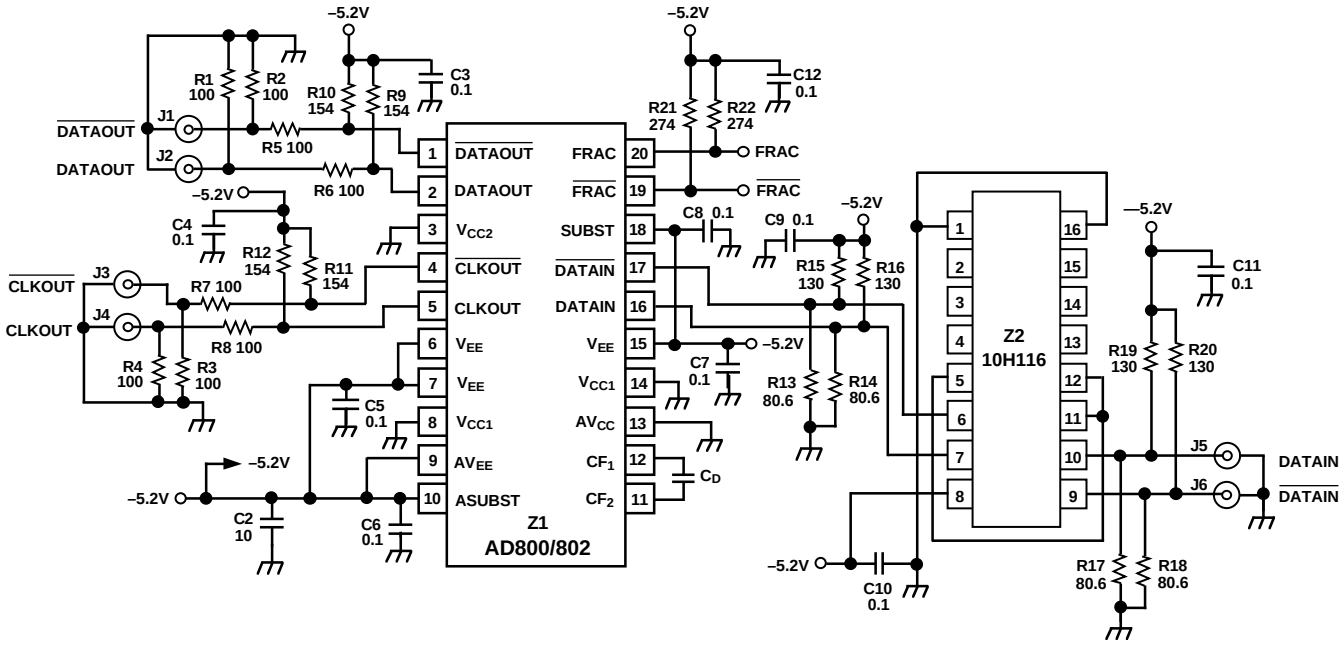


Figure 26. Evaluation Board Schematic, Negative Supply

Table II. Evaluation Board, Negative Supply: Components List

Reference Designator	Description	Quantity
R1–8	Resistor, 100 Ω, 1%	8
R9–12	Resistor, 154 Ω, 1%	4
R13, 14, 17, 18	Resistor, 80.6 Ω, 1%	4
R15, 16, 19, 20	Resistor, 130 Ω, 1%	4
R21, 22	Resistor, 274 Ω, 1%	2
C_D	Capacitor, Loop Damping (See Specifications Page)	1
C2	Capacitor, 10 μF, Tantalum	1
C3–C12	Capacitor, 0.1 μF, Ceramic Chip	10
Z1	AD800/AD802	1
Z2	10H116, ECL Line Receiver	1

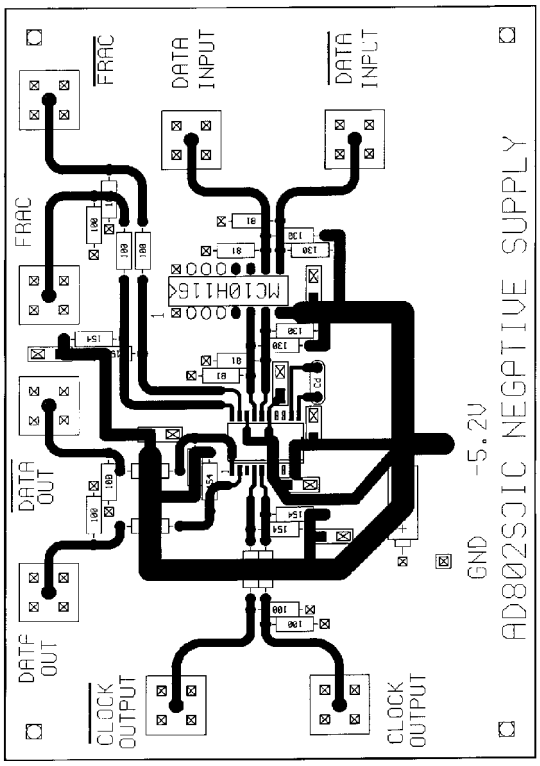


Figure 27. Negative Supply Configuration: Component Side (Top Layer)

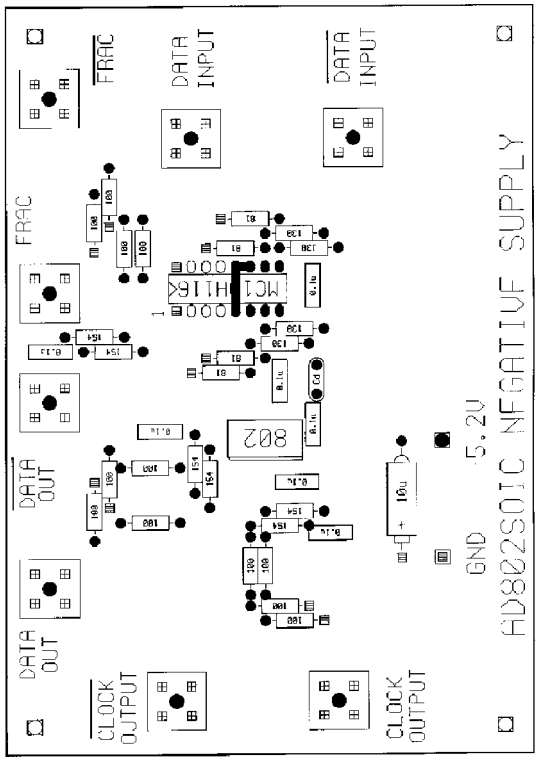


Figure 28. Negative Supply Configuration: Solder Side

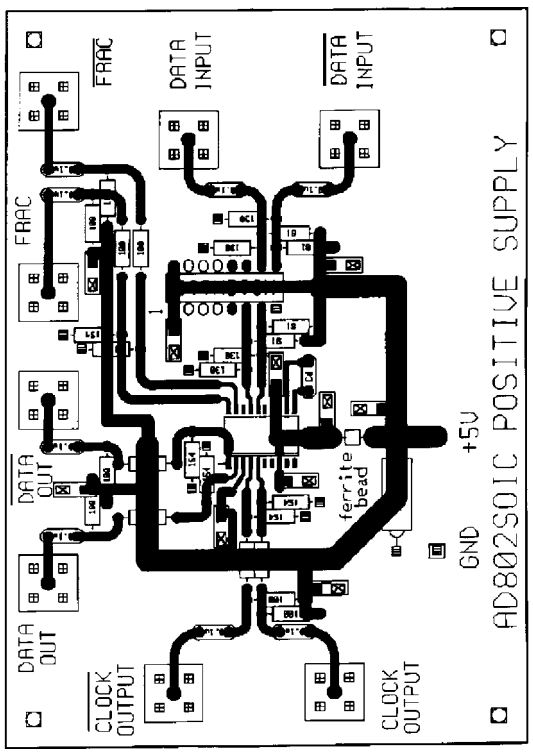


Figure 29. Positive Supply Configuration: Component Side (Top Layer)

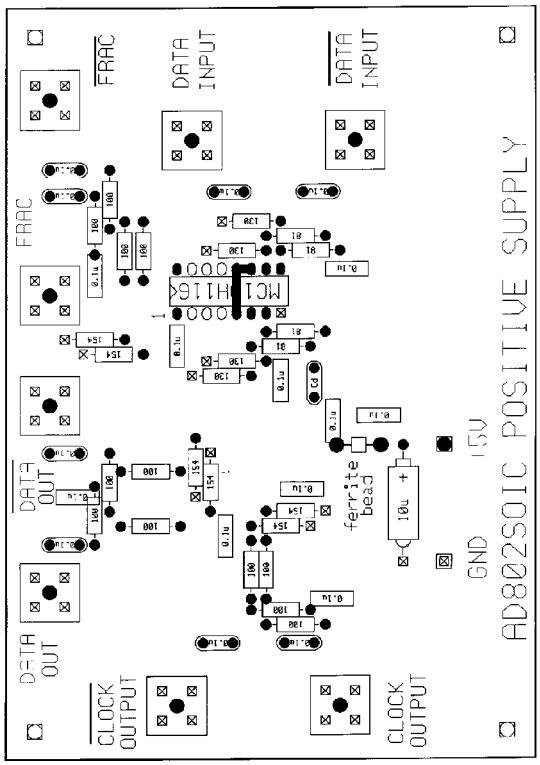
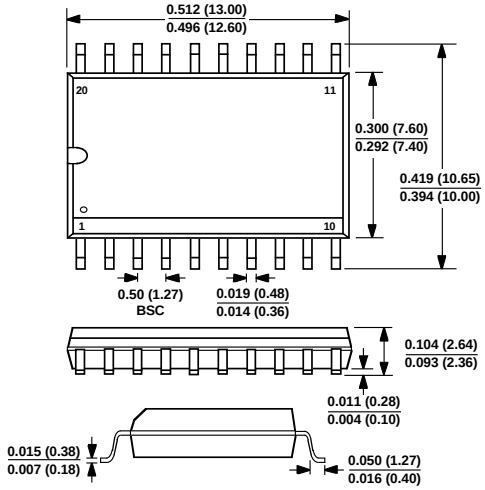


Figure 30. Positive Supply Configuration: Solder Side

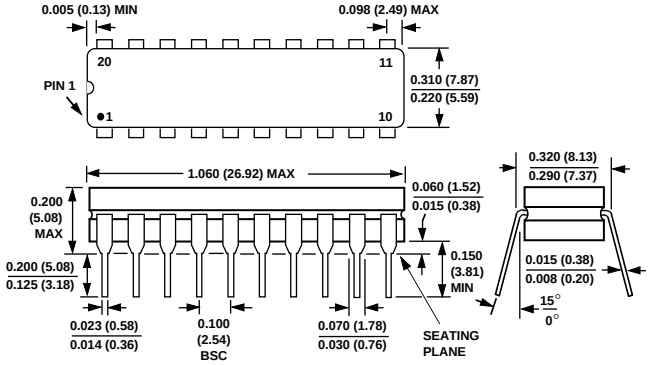
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Pin Small Outline IC Package (R-20)



20-Pin Cerdip Package (Q-20)



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