CAT1320, CAT1321

Supervisory Circuits with I²C Serial 32K CMOS EEPROM

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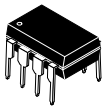
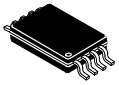
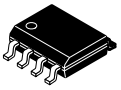


PDIP−8
CASE 646AA



TSSOP−8
CASE 948S



SOIC−8
CASE 751BD

TDFN−8
CASE 511AM

ORDERING INFORMATION

For Ordering Information details, see page 13.

Description

The CAT1320 and CAT1321 are complete memory and supervisory solutions for microcontroller−based systems. A 32 kbit serial EEPROM memory and a system power supervisor with brown−out protection are integrated together in low power CMOS technology. Memory interface is via a 400 kHz I²C bus.

The CAT1320 provides a precision V_{CC} sense circuit and drives an open drain output, $\overline{\text{RESET}}$ low whenever V_{CC} falls below the reset threshold voltage.

The CAT1321 provides a precision VCC sense circuit that drives an open drain output, RESET high whenever V_{CC} falls below the reset threshold voltage.

The power supply monitor and reset circuit protect memory and system controllers during power up/down and against brownout conditions. Five reset threshold voltages support 5 V, 3.3 V and 3 V systems. If power supply voltages are out of tolerance reset signals become active, preventing the system microcontroller, ASIC or peripherals from operating. Reset signals become inactive typically 200 ms after the supply voltage exceeds the reset threshold level. With both active high and low reset options, interface to microcontrollers and other ICs is simple. In addition, the $\overline{\text{RESET}}$ (CAT1320) pin can be used as an input for push−button manual reset capability.

The CAT1320/21 memory features a 64−byte page. In addition, hardware data protection is provided by a V_{CC} sense circuit that prevents writes to memory whenever V_{CC} falls below the reset threshold or until V_{CC} reaches the reset threshold during power up.

Available packages include an 8−pin DIP, SOIC, TSSOP and 4.9 x 3 mm TDFN.

Features

- Precision Power Supply Voltage Monitor
  - 5 V, 3.3 V and 3 V Systems
    - +5.0 V (±5%, ±10%)
    - +3.3 V (±5%, ±10%)
    - +3.0 V (±10%)
- Active Low Reset, CAT1320
- Active High Reset, CAT1321
- Valid Reset Guaranteed at V_{CC} = 1 V
- 400 kHz I²C Bus
- 3.0 V to 5.5 V Operation
- Low Power CMOS Technology
- 64−Byte Page Write Buffer
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- 8−pin DIP, SOIC, TSSOP and TDFN Packages
- Industrial Temperature Range
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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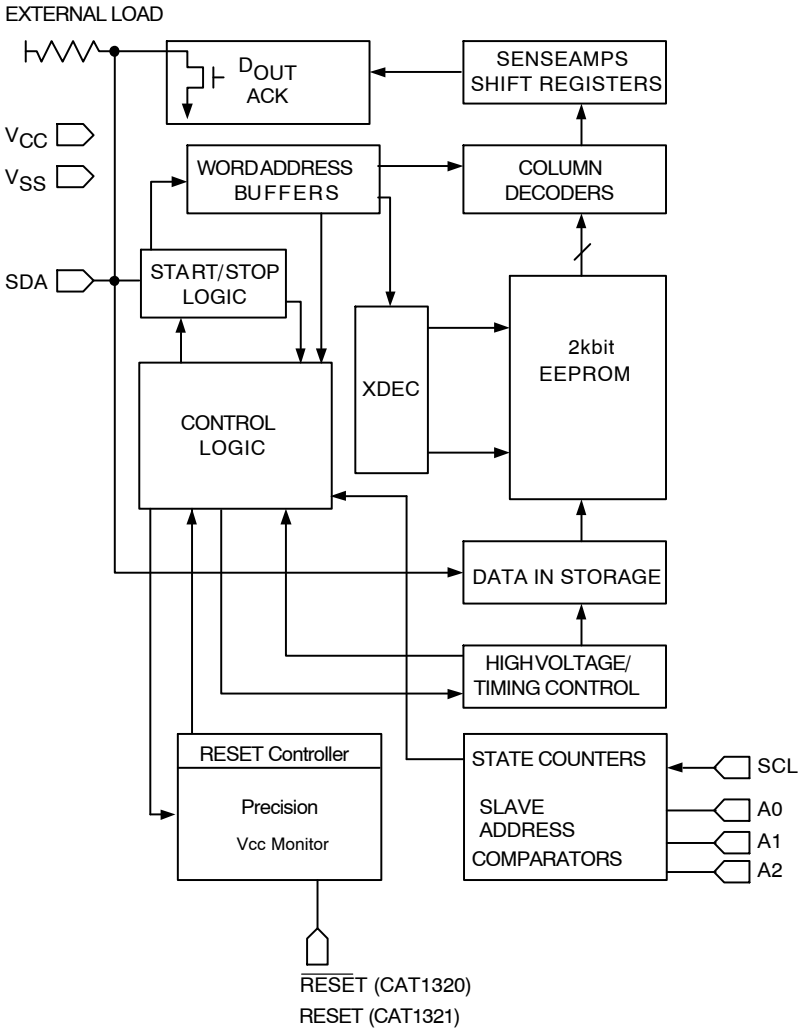
Table 1. THRESHOLD VOLTAGE OPTION

Part Dash Number	Minimum Threshold	Maximum Threshold
−45	4.50	4.75
−42	4.25	4.50
−30	3.00	3.15
−28	2.85	3.00
−25	2.55	2.70

BLOCK DIAGRAM



PIN CONFIGURATION

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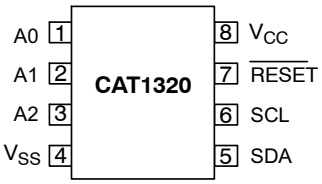
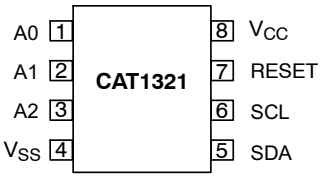
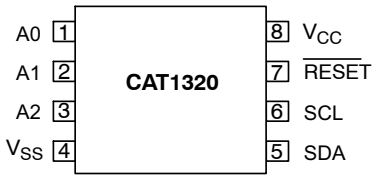
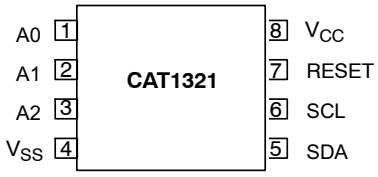
SOIC (W)



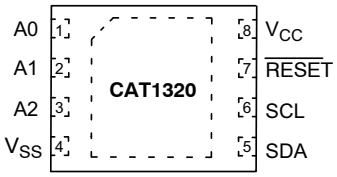


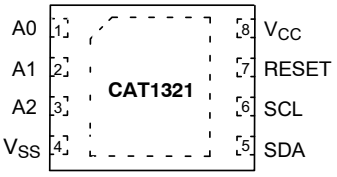
TSSOP (Y)





TDFN Package 4.9 mm x 3 mm
(ZD2)





PIN DESCRIPTION

RESET/$\overline{\text{RESET}}$: RESET OUTPUTS

These are open drain pins and $\overline{\text{RESET}}$ can be used as a manual reset trigger input. By forcing a reset condition on the pin the device will initiate and maintain a reset condition. The RESET pin must be connected through a pull−down resistor, and the $\overline{\text{RESET}}$ pin must be connected through a pull−up resistor.

SDA: SERIAL DATA ADDRESS

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire−ORed with other open drain or open collector outputs.

SCL: SERIAL CLOCK

Serial clock input.

A0, A1, A2: DEVICE ADDRESS INPUTs

When hardwired, up to eight CAT1320/21 devices may be addressed on a single bus system (refer to Device Addressing). When the pins are left unconnected, the default values are zeros.

Table 2. PIN FUNCTION

Pin Name	Function
$\overline{\text{RESET}}$	Active Low Reset Input/Output (CAT1320)
V_{SS}	Ground
SDA	Serial Data/Address
SCL	Clock Input
RESET	Active High Reset Output (CAT1321)
V_{CC}	Power Supply

Table 3. OPERATING TEMPERATURE RANGE

Industrial	−40°C to 85°C

SPECIFICATIONS

Table 4. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Temperature Under Bias	−40 to +85	°C
Storage Temperature	−65 to +105	°C
Voltage on any Pin with Respect to Ground (Note 1)	−0.5 to V_{CC} + 2.0	V
V_{CC} with Respect to Ground	−0.5 to +7.0	V
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Lead Soldering Temperature (10 seconds)	300	°C
Output Short Circuit Current (Note 1)	100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Output shorted for no more than one second. No more than one output shorted at a time.

Table 5. D.C. OPERATING CHARACTERISTICS

V_{CC} = +3.0 V to +5.5 V and over the recommended temperature conditions unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}	−2		10	μA
I_{LO}	Output Leakage Current	V_{IN} = GND to V_{CC}	−10		10	μA
I_{CC1}	Power Supply Current (Write)	f_{SCL} = 400 kHz V_{CC} = 5.5 V			3	mA
I_{CC2}	Power Supply Current (Read)	f_{SCL} = 400 kHz V_{CC} = 5.5 V			1	mA
I_{SB}	Standby Current	V_{CC} = 5.5 V V_{IN} = GND or V_{CC}			40	μA
V_{IL} (Note 3)	Input Low Voltage		−0.5		0.3 x V_{CC}	V
V_{IH} (Note 3)	Input High Voltage		0.7 x V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage (SDA, $\overline{\text{RESET}}$)	I_{OL} = 3 mA V_{CC} = 3.0 V			0.4	V
V_{OH}	Output High Voltage (RESET)	I_{OH} = −0.4 mA V_{CC} = 3.0 V	V_{CC} − 0.75			V
V_{TH}	Reset Threshold	CAT132x−45 (V_{CC} = 5.0 V)	4.50		4.75	V
		CAT132x−42 (V_{CC} = 5.0 V)	4.25		4.50	
		CAT132x−30 (V_{CC} = 3.3 V)	3.00		3.15	
		CAT132x−28 (V_{CC} = 3.3 V)	2.85		3.00	
		CAT132x−25 (V_{CC} = 3.0 V)	2.55		2.70	
V_{RVALID} (Note 2)	Reset Output Valid V_{CC} Voltage		1.00			V
V_{RT} (Note 2)	Reset Threshold Hysteresis		15			mV

2. This parameter is tested initially and after a design or process change that affects the parameter. Not 100% tested.
3. V_{IL} min and V_{IH} max are reference values only and are not tested.

Table 6. CAPACITANCE

T_A = 25°C, f = 1.0 MHz, V_{CC} = 5 V

Symbol	Test	Test Conditions	Max	Units
C_{OUT} (Note 1)	Output Capacitance	V_{OUT} = 0 V	8	pF
C_{IN} (Note 1)	Input Capacitance	V_{IN} = 0 V	6	pF

Table 7. AC CHARACTERISTICS

V_{CC} = 3.0 V to 5.5 V and over the recommended temperature conditions, unless otherwise specified.

Memory Read & Write Cycle (Note 2)

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency		400	kHz
t_{SP}	Input Filter Spike Suppression (SDA, SCL)		100	ns
t_{LOW}	Clock Low Period	1.3		μs
t_{HIGH}	Clock High Period	0.6		μs
t_R (Note 1)	SDA and SCL Rise Time		300	ns
t_F (Note 1)	SDA and SCL Fall Time		300	ns
$t_{HD; STA}$	Start Condition Hold Time	0.6		μs
$t_{SU; STA}$	Start Condition Setup Time (for a Repeated Start)	0.6		μs
$t_{HD; DAT}$	Data Input Hold Time	0		ns
$t_{SU; DAT}$	Data Input Setup Time	100		ns
$t_{SU; STO}$	Stop Condition Setup Time	0.6		μs
t_{AA}	SCL Low to Data Out Valid		900	ns
t_{DH}	Data Out Hold Time	50		ns
t_{BUF} (Note 1)	Time the Bus must be Free Before a New Transmission Can Start	1.3		μs
t_{WC} (Note 3)	Write Cycle Time (Byte or Page)		5	ms

1. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
2. Test Conditions according to “AC Test Conditions” table.
3. The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high and the device does not respond to its slave address.

Table 8. RESET CIRCUIT AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PURST}	Reset Timeout	Note 2	130	200	270	ms
t_{RDP}	V_{TH} to RESET output Delay	Note 3			5	μs
t_{GLITCH}	V_{CC} Glitch Reject Pulse Width	Notes 4 and 5			30	ns
MR Glitch	Manual Reset Glitch Immunity	Note 5			100	ns
t_{MRW}	MR Pulse Width	Note 5	5			μs

Table 9. POWER−UP TIMING (Notes 5 and 6)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PUR}	Power−Up to Read Operation				270	ms
t_{PUW}	Power−Up to Write Operation				270	ms

Table 10. AC TEST CONDITIONS

Parameter	Test Conditions
Input Pulse Voltages	0.2 V_{CC} to 0.8 V_{CC}
Input Rise and Fall Times	10 ns
Input Reference Voltages	0.3 V_{CC} , 0.7 V_{CC}
Output Reference Voltages	0.5 V_{CC}
Output Load	Current Source: I_{OL} = 3 mA; C_L = 100 pF

Table 11. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Max	Units
N_{END} (Note 5)	Endurance	MIL−STD−883, Test Method 1033	1,000,000		Cycles/Byte
T_{DR} (Note 5)	Data Retention	MIL−STD−883, Test Method 1008	100		Years
V_{ZAP} (Note 5)	ESD Susceptibility	MIL−STD−883, Test Method 3015	2000		Volts
I_{LTH} (Notes 5 & 7)	Latch−Up	JEDEC Standard 17	100		mA

1. Test Conditions according to “AC Test Conditions” table.
2. Power−up, Input Reference Voltage $V_{CC} = V_{TH}$, Reset Output Reference Voltage and Load according to “AC Test Conditions” Table
3. Power−Down, Input Reference Voltage $V_{CC} = V_{TH}$, Reset Output Reference Voltage and Load according to “AC Test Conditions” Table
4. V_{CC} Glitch Reference Voltage = V_{THmin}; Based on characterization data
5. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
6. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified memory operation can be initiated.
7. Latch−up protection is provided for stresses up to 100 mA on input and output pins from −1 V to V_{CC} + 1 V.

DEVICE OPERATON

Reset Controller Description

The CAT1320/21 precision Reset controllers ensure correct system operation during brownout and power up/down conditions. They are configured with opendrain $\overline{\text{RESET}}$/RESET outputs.

During power−up, the $\overline{\text{RESET}}$/RESET output remains active until V_{CC} reaches the V_{TH} threshold and will continue driving the outputs for approximately 200 ms (t_{PURST}) after reaching V_{TH}. After the t_{PURST} timeout interval, the device will cease to drive the reset output. At this point the reset output will be pulled up or down by their respective pull up/down resistors.

During power−down, the $\overline{\text{RESET}}$/RESET outputs will be active when V_{CC} falls below V_{TH}. The $\overline{\text{RESET}}$/RESET output will be valid so long as V_{CC} is > 1.0 V (V_{RVALID}). The device is designed to ignore the fast negative going V_{CC} transient pulses (glitches).

Reset output timing is shown in Figure 1.

Manual Reset Operation

The $\overline{\text{RESET}}$ pin can operate as reset output and manual reset input. The input is edge triggered; that is, the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a high to low transition.

When $\overline{\text{RESET}}$ I/O is driven to the active state, the 200 ms timer will begin to time the reset interval. If external reset is shorter than 200 ms, Reset outputs will remain active at least 200 ms.

Glitches shorter than 100 ns on $\overline{\text{RESET}}$ input will not generate a reset pulse.

Hardware Data Protection

The CAT1320/21 family has been designed to solve many of the data corruption issues that have long been associated with serial EEPROMs. Data corruption occurs when incorrect data is stored in a memory location which is assumed to hold correct data.

Whenever the device is in a Reset condition, the embedded EEPROM is disabled for all operations, including write operations. If the Reset output is active, in progress communications to the EEPROM are aborted and no new communications are allowed. In this condition an internal write cycle to the memory can not be started, but an in progress internal non−volatile memory write cycle can not be aborted. An internal write cycle initiated before the Reset condition can be successfully finished if there is enough time (5 ms) before VCC reaches the minimum value of 2 V.

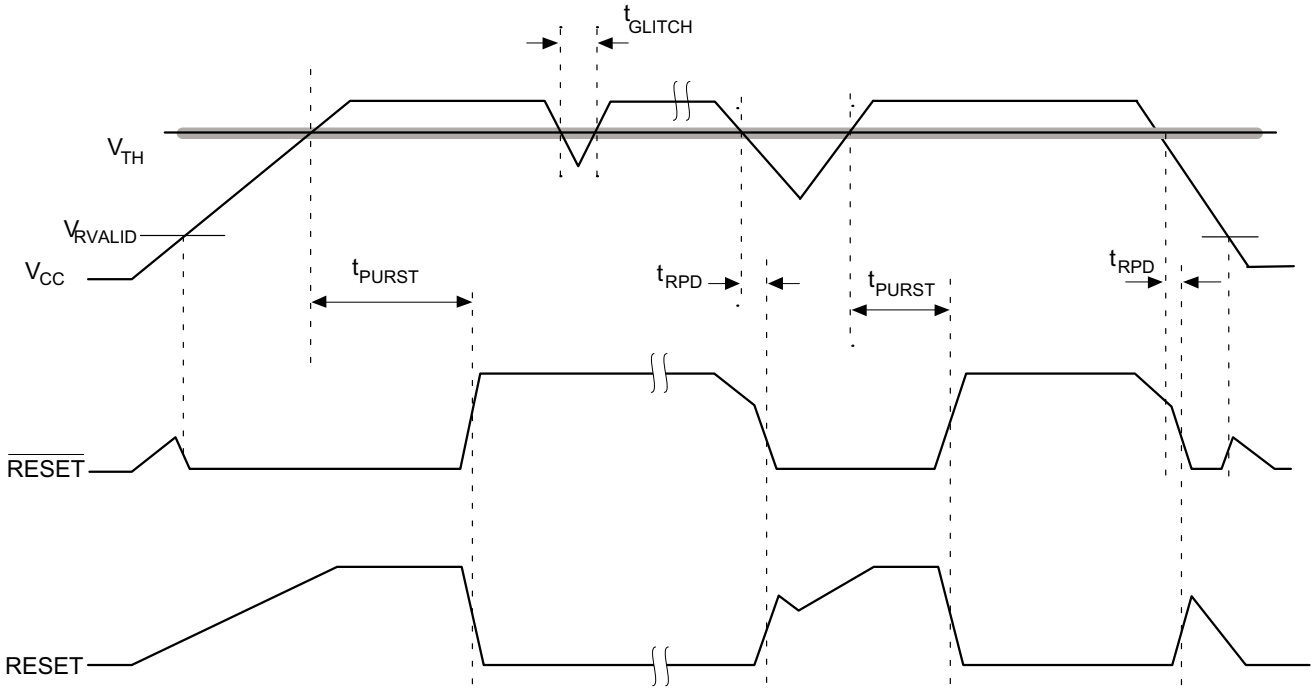


Figure 1. RESET/$\overline{\text{RESET}}$ Output Timing

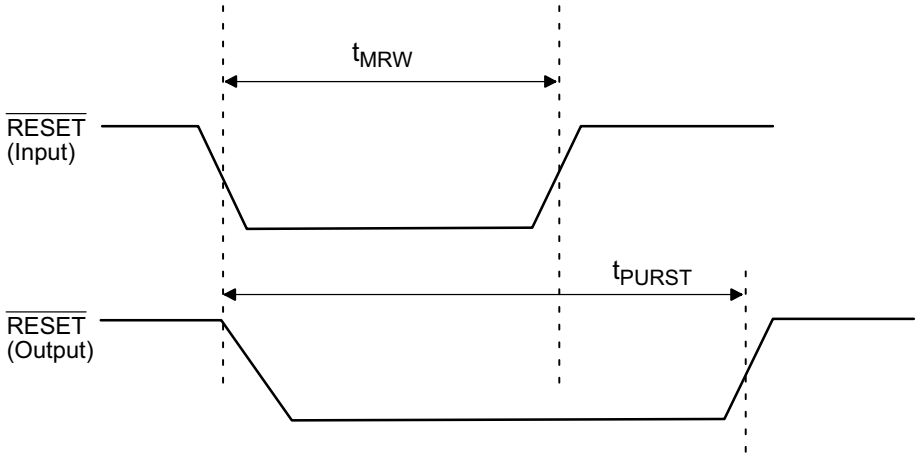


Figure 2. $\overline{\text{RESET}}$ as Manual Reset Input Operation and Timing

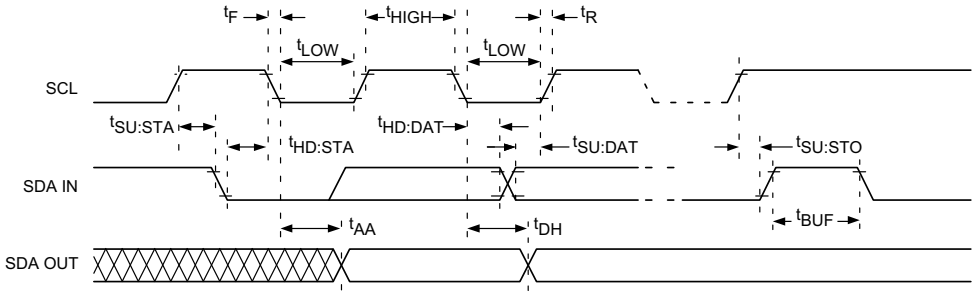


Figure 3. Bus Timing

EMBEDDED EEPROM OPERATON

The CAT1320 and CAT1321 feature a 32 kbit embedded serial EEPROM that supports the I^2C Bus data transmission protocol. This Inter−Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C Bus Protocol

The features of the I^2C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

Start Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT1320/21 monitors the SDA and SCL lines and will not respond until this condition is met.

Stop Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The four most significant bits of the 8−bit slave address are programmable in metal and the default is 1010.

The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT1320/21 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT1320/21 then perform a Read or Write operation depending on the R/$\overline{W}$ bit.

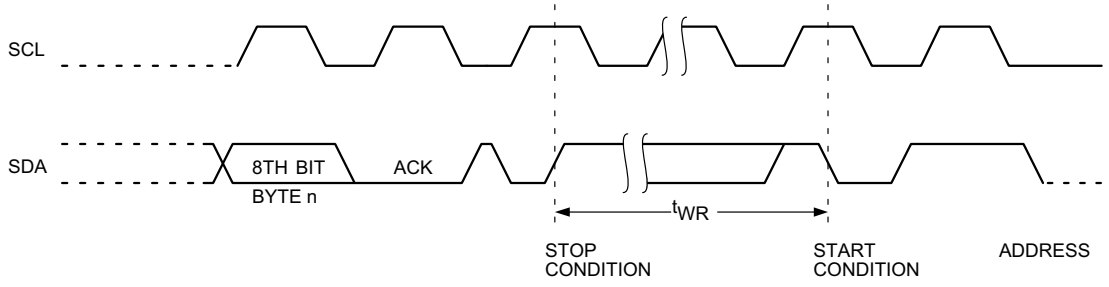


Figure 4. Write Cycle Timing

ACKNOWLEDGE

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT1320/21 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8−bit byte.

When the CAT1320/21 begins a READ mode it transmits 8 bits of data, releases the SDA line and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT1320/21 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends two 8−bit address bytes that are to be written into the address pointers of the device. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT1320/21 acknowledges once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to non−volatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

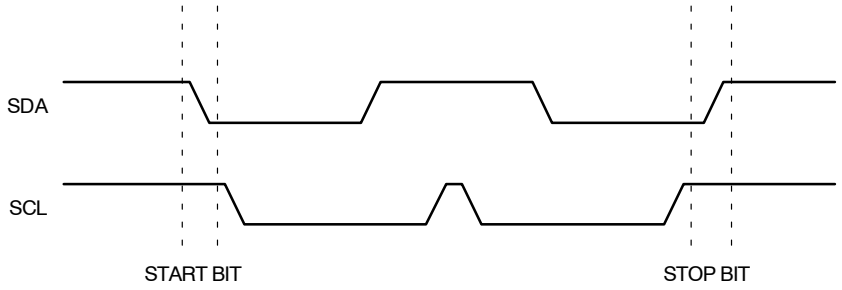


Figure 5. Start/Stop Timing

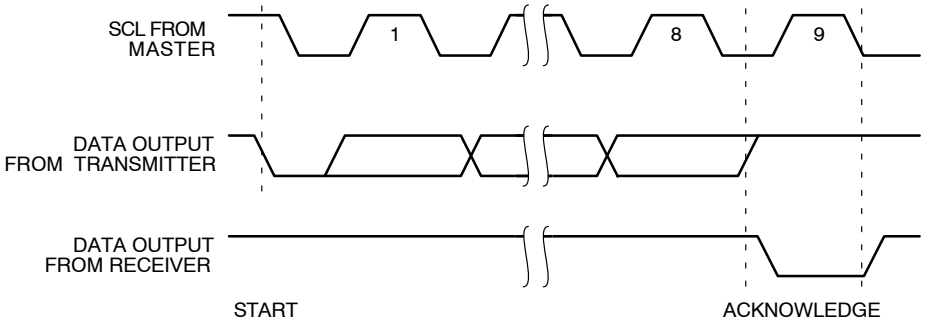


Figure 6. Acknowledge Timing

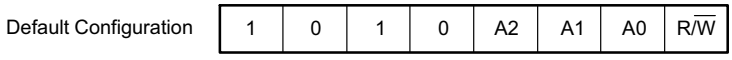


Figure 7. Slave Address Bits

Page Write

The CAT1320/21 writes up to 64 bytes of data in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to additional 63 bytes. After each byte has been transmitted, the CAT1320/21 will respond with an acknowledge and internally increment the lower order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 64 bytes before sending the STOP condition, the address counter ‘wraps around’, and previously transmitted data will be overwritten.

When all 64 bytes are received, and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the CAT1320/21 in a single write cycle.

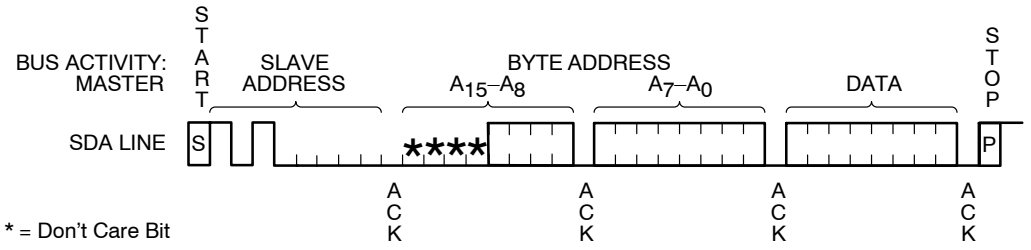


Figure 8. Byte Write Timing

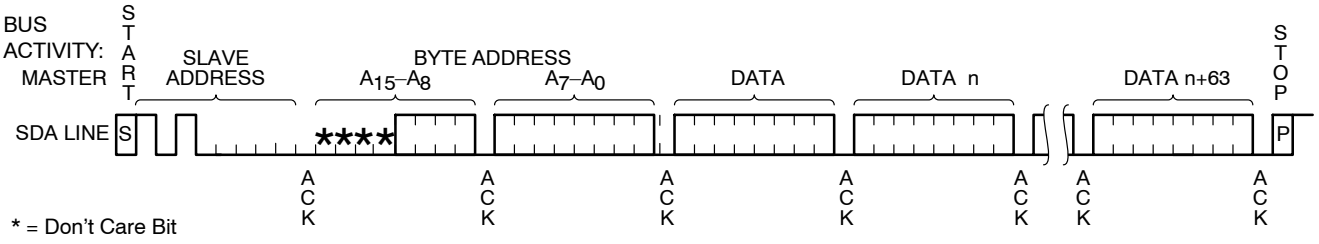


Figure 9. Page Write Timing

Acknowledge Polling

Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT1320/21 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the device is still busy with the write operation, no ACK will be returned. If a write operation has completed, an ACK will be returned and the host can then proceed with the next read or write operation.

Read Operations

The READ operation for the CAT1320/21 is initiated in the same manner as the write operation with one exception, that R/$\overline{W}$ bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/Random READ and Sequential READ.

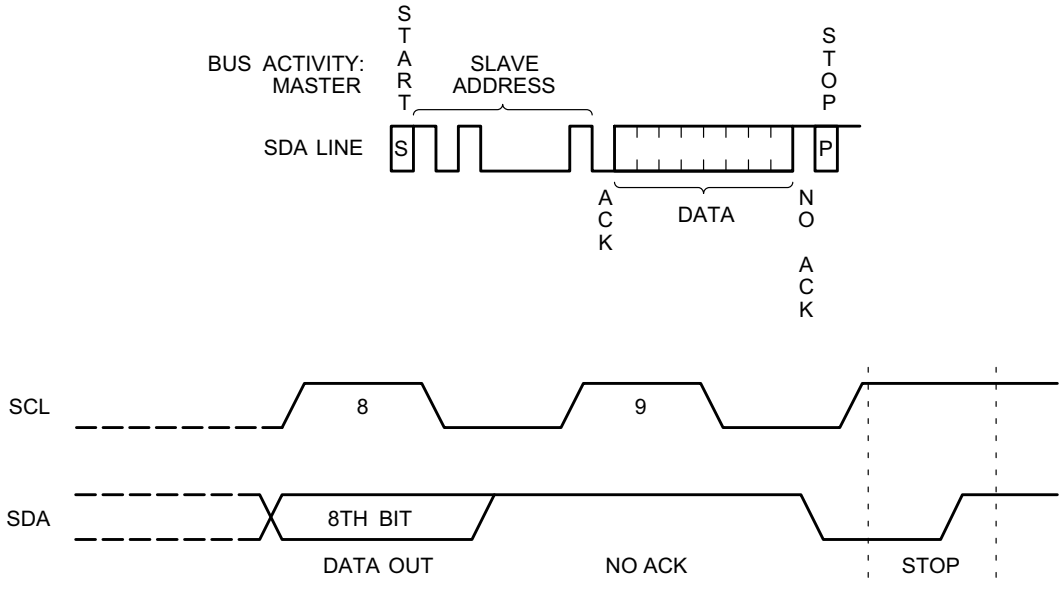


Figure 10. Immediate Address Read Timing

Immediate/Current Address Read

The CAT1320 and CAT1321 address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. For all devices, N = E = 4,095. The counter will wrap around to Zero and continue to clock out valid data. After the CAT1320 and CAT1321 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8−bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

Selective/Random Read

Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a ‘dummy’ write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After the CAT1320 and CAT1321 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT1320 and CAT1321 then responds with its acknowledge and sends the 8−bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT1320 and CAT1321 sends the initial 8−bit byte requested, the Master will responds with an acknowledge which tells the device it requires more data. The CAT1320 and CAT1321 will continue to output an 8−bit byte for each acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT1320 and CAT1321 is sent sequentially with the data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT1320 and CAT1321 address bits so that the entire memory array can be read during one operation.

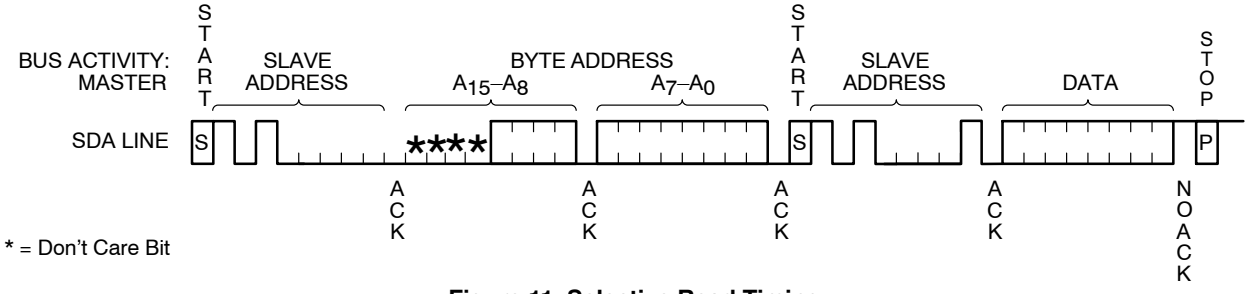


Figure 11. Selective Read Timing

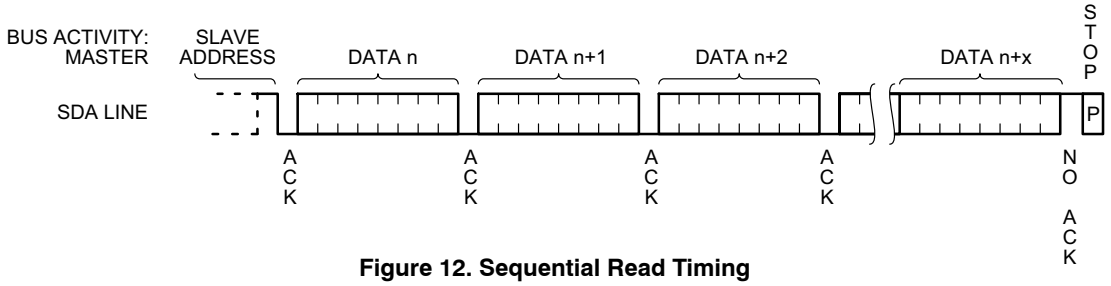


Figure 12. Sequential Read Timing

ORDERING INFORMATION

Orderable Part Numbers – CAT1320 Series (See Notes 1 – 5)			
Device	Reset Threshold	Package	Shipping
CAT1320LI−45−G	4.50 V – 4.75 V	PDIP	3000 Tape & Reel
CAT1320LI−42−G	4.25 V – 4.50 V		
CAT1320LI−30−G	3.00 V – 3.15 V		
CAT1320LI−28−G	2.85 V – 3.00 V		
CAT1320LI−25−G	2.55 V – 2.70 V		
CAT1320WI−45−GT3	4.50 V – 4.75 V	SOIC	
CAT1320WI−42−GT3	4.25 V – 4.50 V		
CAT1320WI−30−GT3	3.00 V – 3.15 V		
CAT1320WI−28−GT3	2.85 V – 3.00 V		
CAT1320WI−25−GT3	2.55 V – 2.70 V		
CAT1320YI−45−GT3	4.50 V – 4.75 V	TSSOP	
CAT1320YI−42−GT3	4.25 V – 4.50 V		
CAT1320YI−30−GT3	3.00 V – 3.15 V		
CAT1320YI−28−GT3	2.85 V – 3.00 V		
CAT1320YI−25−GT3	2.55 V – 2.70 V		
CAT1320ZD2I45GT3	4.50 V – 4.75 V	TDFN	
CAT1320ZD2I42GT3	4.25 V – 4.50 V		
CAT1320ZD2I30GT3	3.00 V – 3.15 V		
CAT1320ZD2I28GT3	2.85 V – 3.00 V		
CAT1320ZD2I25GT3	2.55 V – 2.70 V		

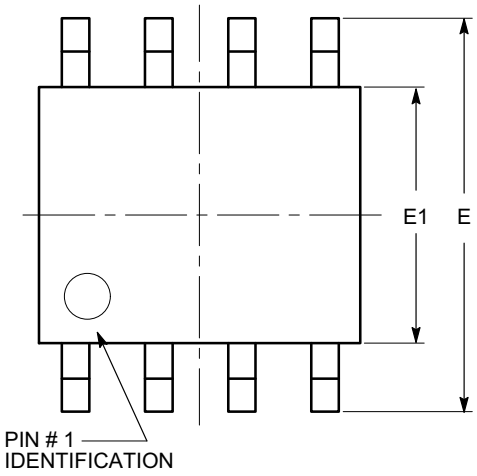
1. All packages are RoHS−compliant (Lead−free, Halogen−free).
2. The standard lead finish is NiPdAu.
3. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
4. TDFN not available in NiPdAu (−G) version.
5. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

Orderable Part Numbers – CAT1321 Series (See Notes 1 – 5)			
Device	Reset Threshold	Package	Shipping
CAT1321LI–45–G	4.50 V – 4.75 V	PDIP	3000 Tape & Reel
CAT1321LI–42–G	4.25 V – 4.50 V		
CAT1321LI–30–G	3.00 V – 3.15 V		
CAT1321LI–28–G	2.85 V – 3.00 V		
CAT1321LI–25–G	2.55 V – 2.70 V		
CAT1321WI–45–GT3	4.50 V – 4.75 V	SOIC	
CAT1321WI–42–GT3	4.25 V – 4.50 V		
CAT1321WI–30–GT3	3.00 V – 3.15 V		
CAT1321WI–28–GT3	2.85 V – 3.00 V		
CAT1321WI–25–GT3	2.55 V – 2.70 V		
CAT1321YI–45–GT3	4.50 V – 4.75 V	TSSOP	
CAT1321YI–42–GT3	4.25 V – 4.50 V		
CAT1321YI–30–GT3	3.00 V – 3.15 V		
CAT1321YI–28–GT3	2.85 V – 3.00 V		
CAT1321YI–25–GT3	2.55 V – 2.70 V		
CAT1321ZD2I45GT3	4.50 V – 4.75 V	TDFN	
CAT1321ZD2I42GT3	4.25 V – 4.50 V		
CAT1321ZD2I30GT3	3.00 V – 3.15 V		
CAT1321ZD2I28GT3	2.85 V – 3.00 V		
CAT1321ZD2I25GT3	2.55 V – 2.70 V		

1. All packages are RoHS–compliant (Lead–free, Halogen–free).
2. The standard lead finish is NiPdAu.
3. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
4. TDFN not available in NiPdAu (–G) version.
5. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

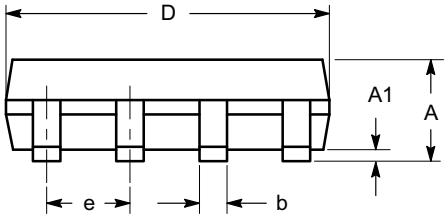
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

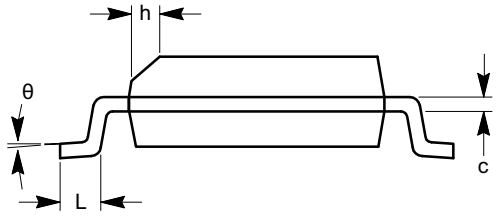


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



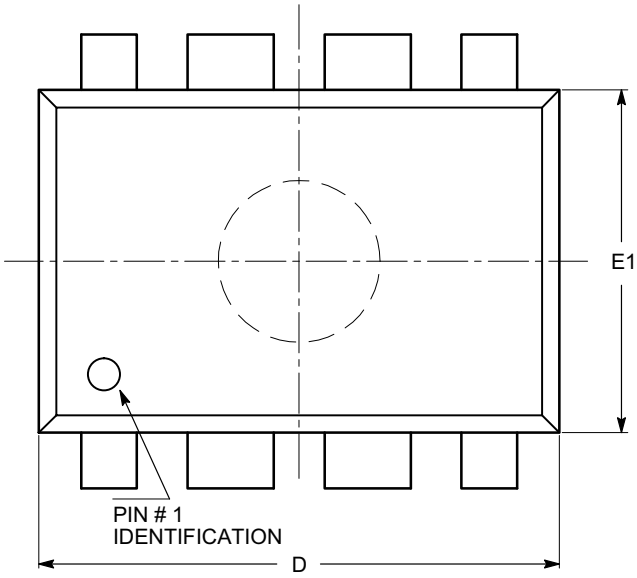
SIDE VIEW



END VIEW

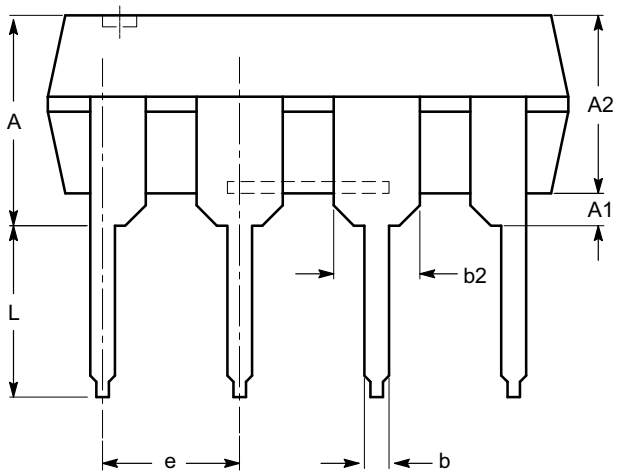
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

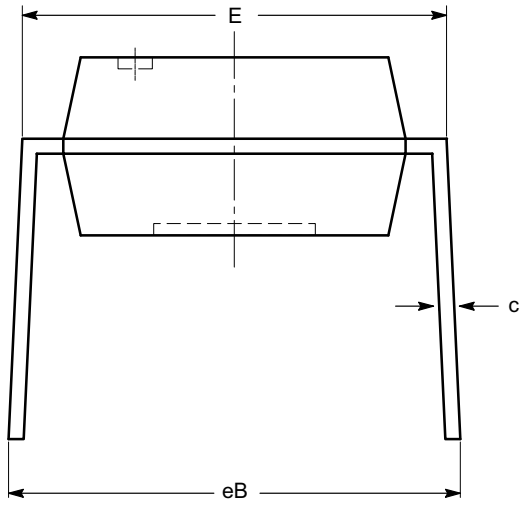


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



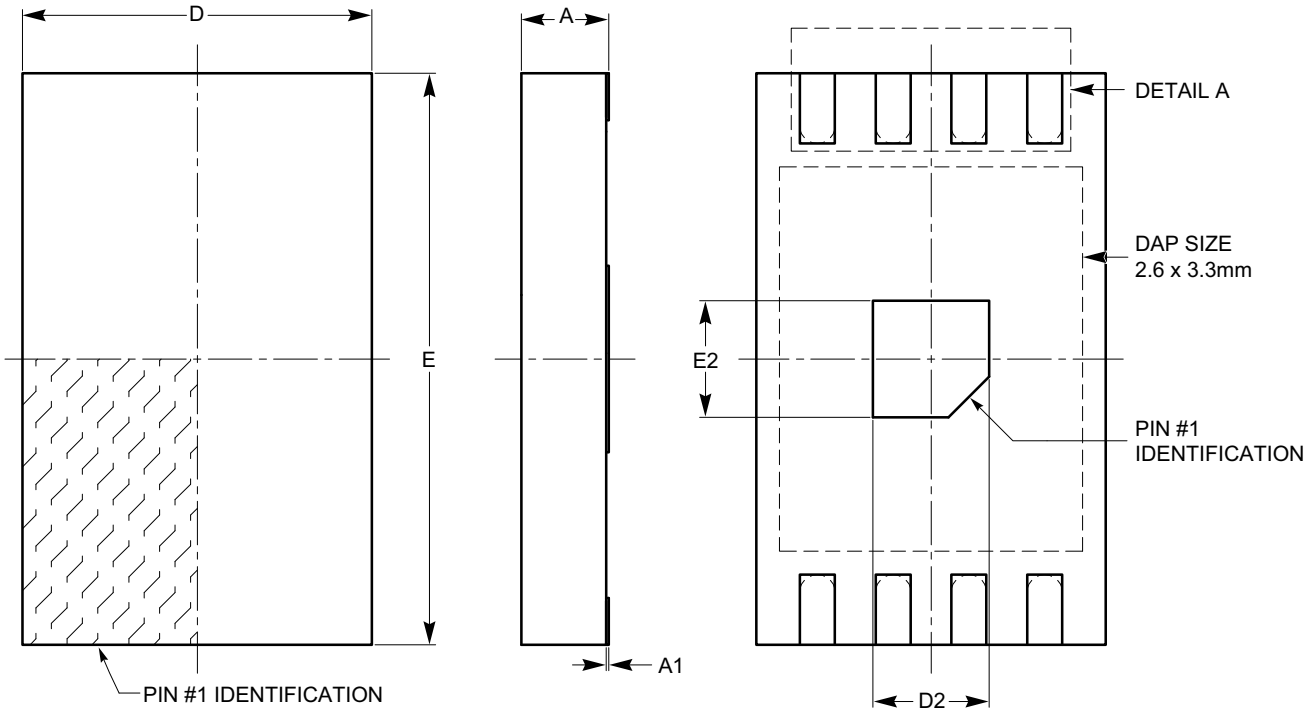
SIDE VIEW



END VIEW

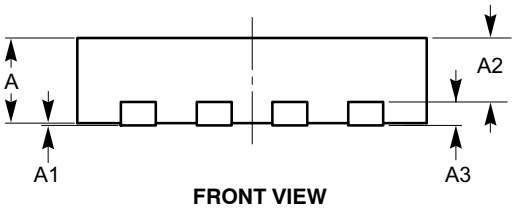
Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

TDFN8, 3x4.9
CASE 511AM−01
ISSUE A

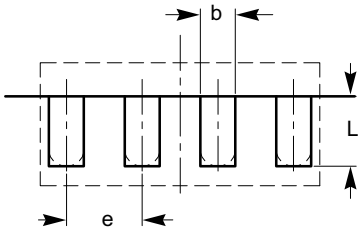


TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3		0.20 REF	
b	0.25	0.30	0.35
D	2.90	3.00	3.10
D2	0.90	1.00	1.10
E	4.80	4.90	5.00
E2	0.90	1.00	1.10
e		0.65 TYP	
L	0.50	0.60	0.70



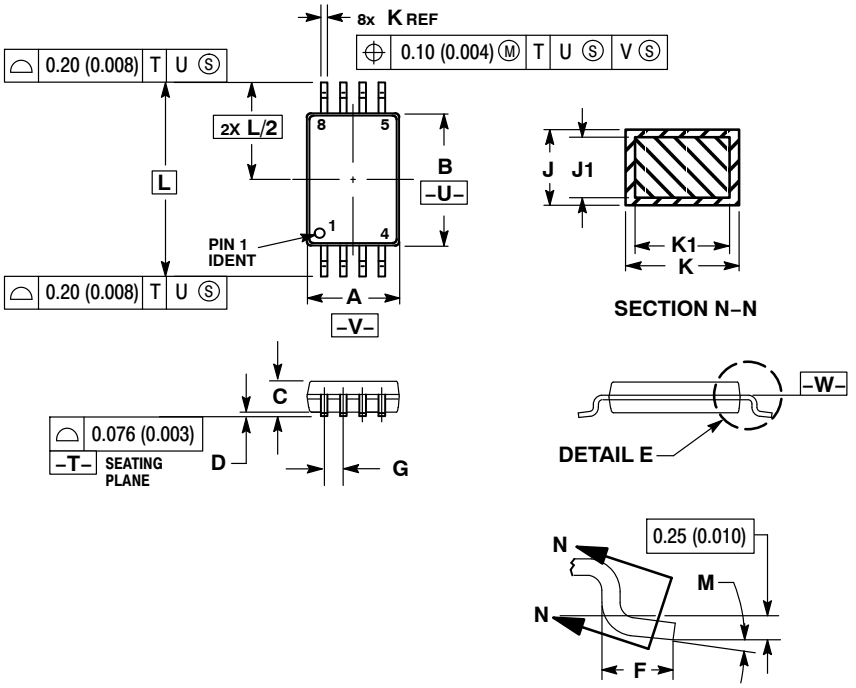
FRONT VIEW



DETAIL A

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

TSSOP−8
CASE 948S−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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