



ALPHA & OMEGA
SEMICONDUCTOR



AO4624

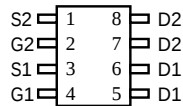
Complementary Enhancement Mode Field Effect Transistor

General Description

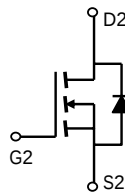
The AO4624 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications. *Standard product AO4624 is Pb-free (meets ROHS & Sony 259 specifications). AO4624L is a Green Product ordering option. AO4624 and AO4624L are electrically identical.*

Features

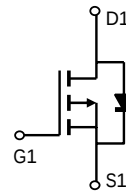
n-channel	p-channel
V_{DS} (V) = 30V	-30V
I_D = 6.9A (V_{GS} =10V)	-6A (V_{GS} =-10V)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 28m Ω (V_{GS} =10V)	< 35m Ω (V_{GS} = -10V)
< 42m Ω (V_{GS} =4.5V)	< 58m Ω (V_{GS} = -4.5V)



SOIC-8



n-channel



p-channel

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^A	$T_A=25^\circ\text{C}$	6.9	-6	A
	$T_A=70^\circ\text{C}$	5.8	-5	
Pulsed Drain Current ^B	I_{DM}	30	-30	A
Power Dissipation	$T_A=25^\circ\text{C}$	2	2	W
	$T_A=70^\circ\text{C}$	1.44	1.44	
Avalanche Current ^B	I_{AR}	15	20	A
Repetitive avalanche energy 0.1mH ^B	E_{AR}	11	20	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ\text{C}$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	48	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		n-ch	74	110	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	n-ch	35	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	48	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		p-ch	74	110	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	p-ch	35	40	$^\circ\text{C/W}$

N-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V T _J =55°C		0.002	1	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	1.9	3	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	20			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =6.9A		23	28	mΩ
		T _J =125°C		31	38	
		V _{GS} =4.5V, I _D =5.0A		34	42	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =6.9A	10	15.4		S
V _{SD}	Diode Forward Voltage	I _S =1A		0.76	1	V
I _S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		737	885	pF
C _{oss}	Output Capacitance			115		pF
C _{rss}	Reverse Transfer Capacitance			73		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		3	4.5	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =6.9A		13.84	17	nC
Q _g (4.5V)	Total Gate Charge			6.74	8.1	nC
Q _{gs}	Gate Source Charge			1.82		nC
Q _{gd}	Gate Drain Charge			3.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =2.2Ω, R _{GEN} =3Ω		4.6	7	ns
t _r	Turn-On Rise Time			4.1	6	ns
t _{D(off)}	Turn-Off DelayTime			20.6	30	ns
t _f	Turn-Off Fall Time			5.2	8	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =6.9A, dI/dt=100A/μs		17.9	21.5	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =6.9A, dI/dt=100A/μs		9.8	11.8	nC

A: The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t_{ON} ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient. R_{θJL} and R_{θJC} are equivalent terms referring to thermal resistance from junction to drain lead.

D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL

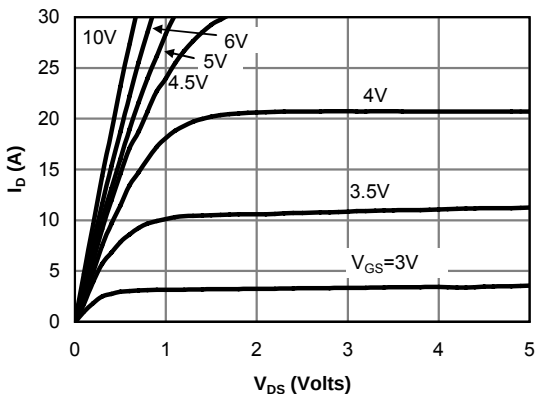


Fig 1: On-Region Characteristics

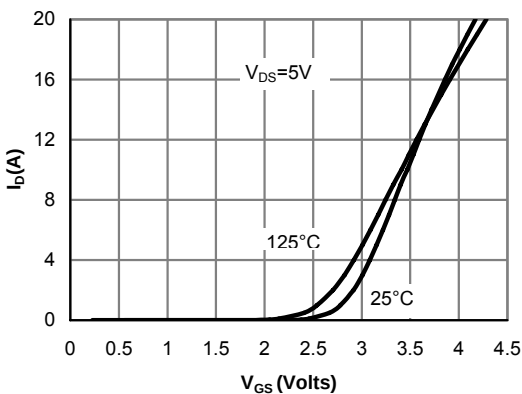


Figure 2: Transfer Characteristics

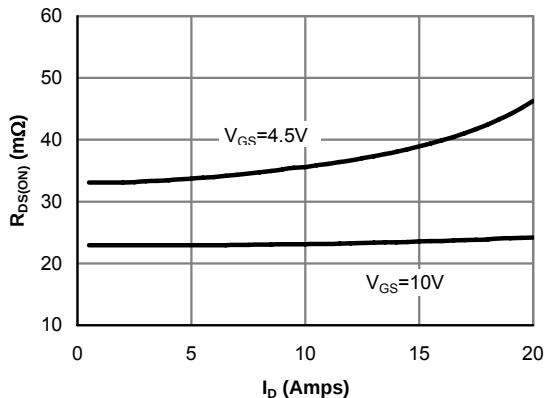


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

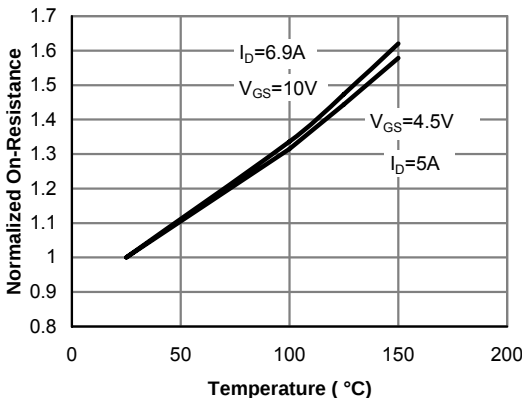


Figure 4: On-Resistance vs. Junction Temperature

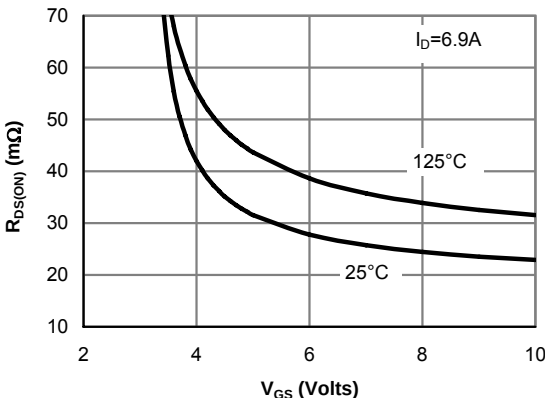


Figure 5: On-Resistance vs. Gate-Source Voltage

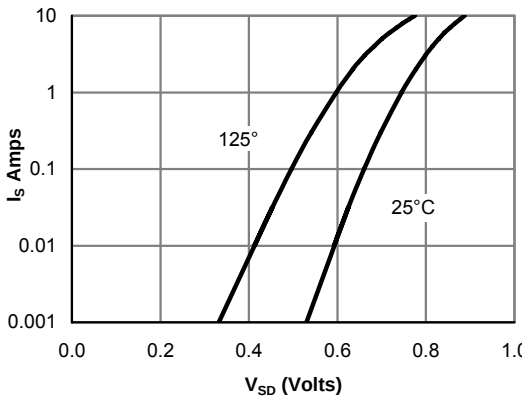


Figure 6: Body diode characteristics

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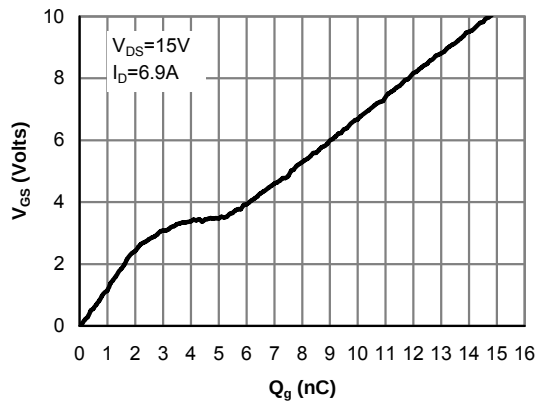


Figure 7: Gate-Charge characteristics

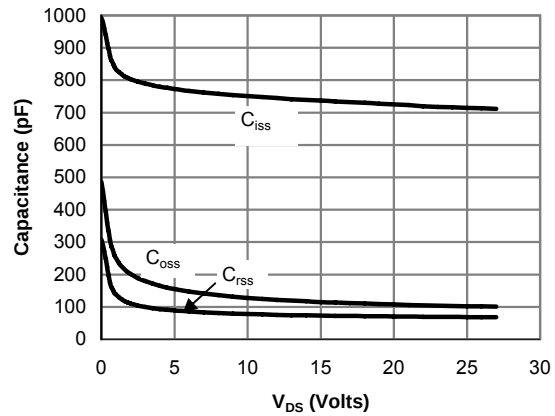


Figure 8: Capacitance Characteristics

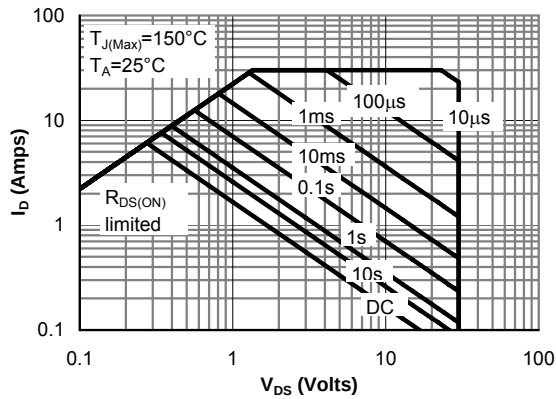


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

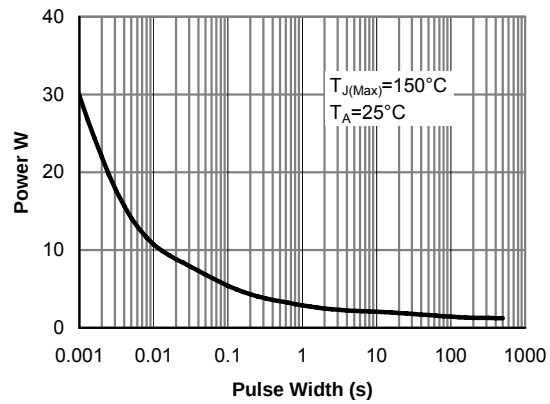


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

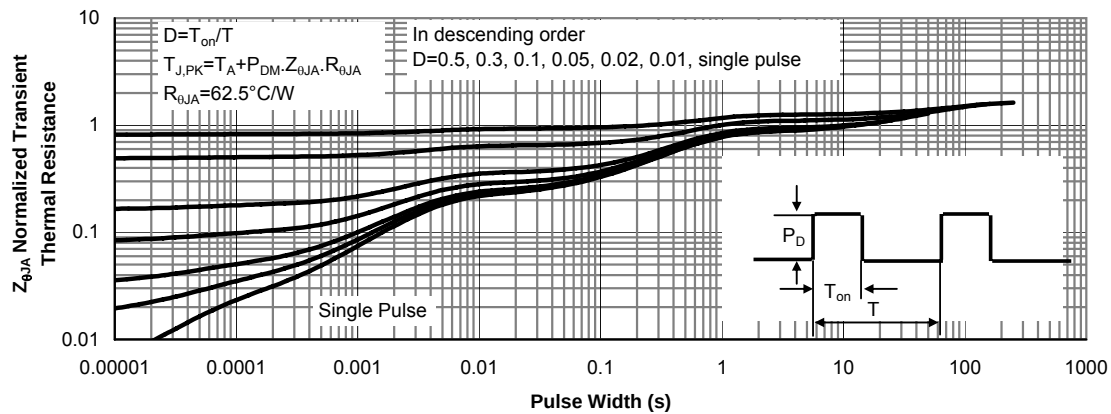


Figure 11: Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V T _J =55°C		-0.003	-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-1.2	-2	-2.4	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-6A T _J =125°C		27 37	35 45	mΩ
		V _{GS} =-4.5V, I _D =-5A		45	58	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-6A		13		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.76	-1	V
I _S	Maximum Body-Diode Continuous Current				-4.2	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		920	1100	pF
C _{oss}	Output Capacitance			190		pF
C _{rss}	Reverse Transfer Capacitance			122		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		3.6	5.4	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge (10V)	V _{GS} =-10V, V _{DS} =-15V, I _D =-6A		18.5	22.2	nC
Q _g (4.5V)	Total Gate Charge (4.5V)			9.6	11.6	nC
Q _{gs}	Gate Source Charge			2.7		nC
Q _{gd}	Gate Drain Charge			4.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =2.7Ω, R _{GEN} =3Ω		7.7	11.5	ns
t _r	Turn-On Rise Time			5.7	8.5	ns
t _{D(off)}	Turn-Off DelayTime			20.2	30	ns
t _f	Turn-Off Fall Time			9.5	14	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-6A, dI/dt=100A/μs		20	24	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-6A, dI/dt=100A/μs		12.3	15	nC

A: The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient. R_{θJL} and R_{θJC} are equivalent terms referring to thermal resistance from junction to drain lead.

D: The static characteristics in Figures 1 to 6, 12, 14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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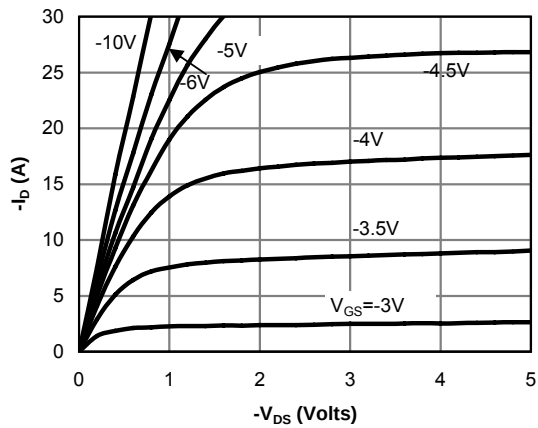


Fig 1: On-Region Characteristics

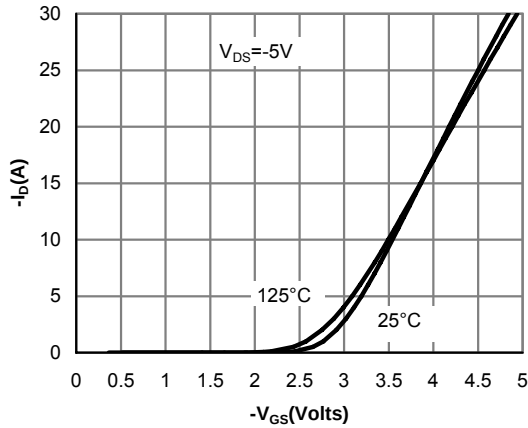


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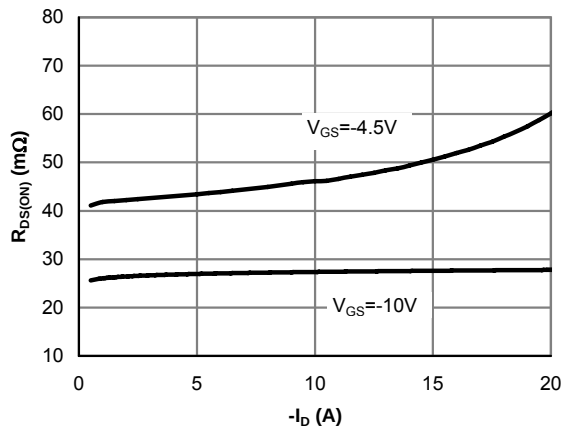


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

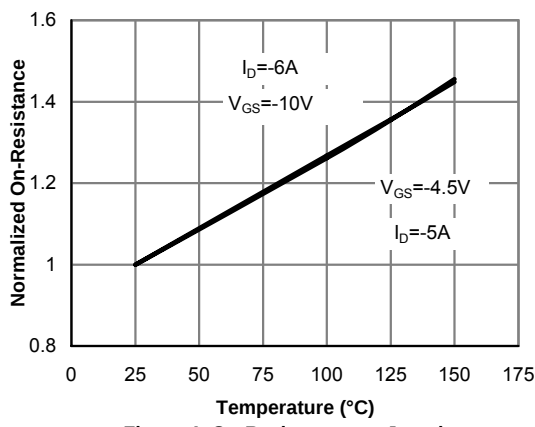


Figure 4: On-Resistance vs. Junction Temperature

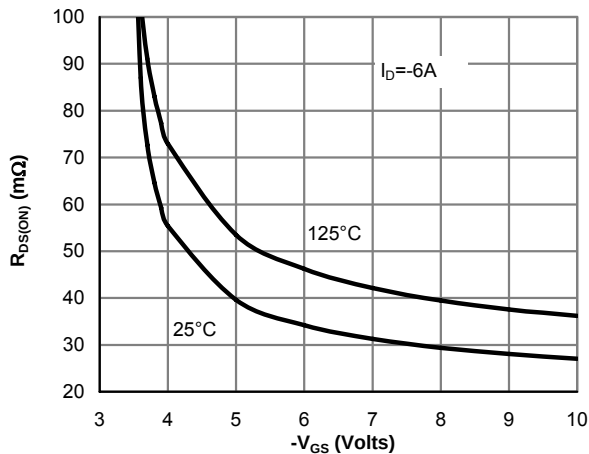


Figure 5: On-Resistance vs. Gate-Source Voltage

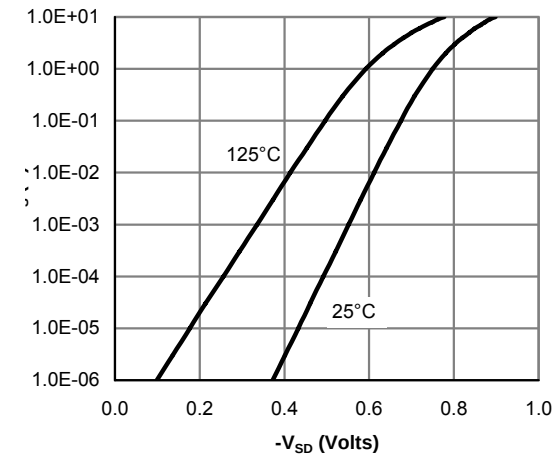


Figure 6: Body-Diode Characteristics

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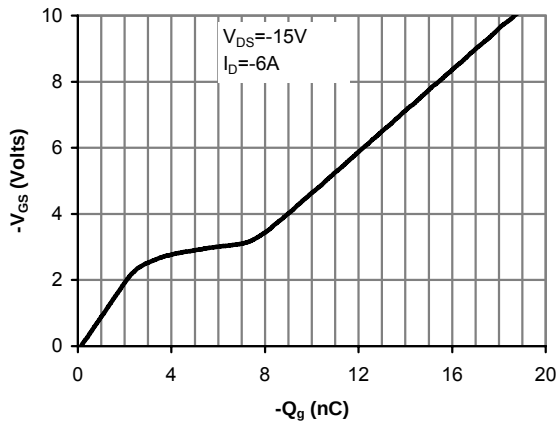


Figure 7: Gate-Charge Characteristics

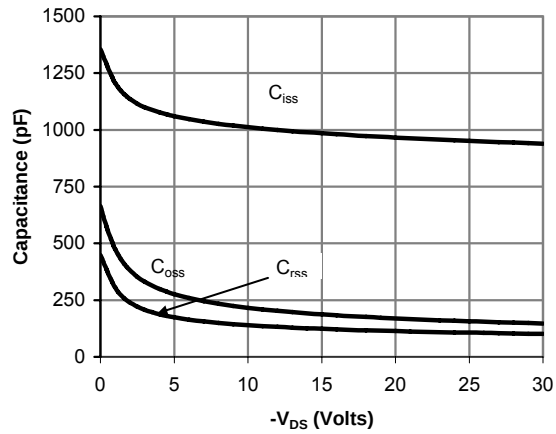


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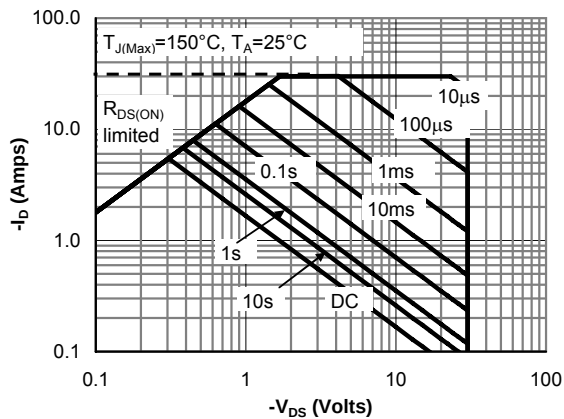


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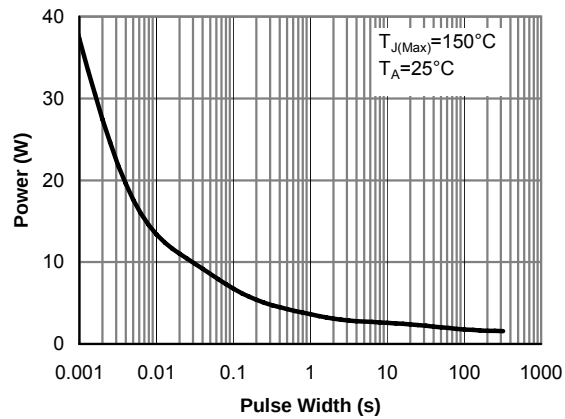


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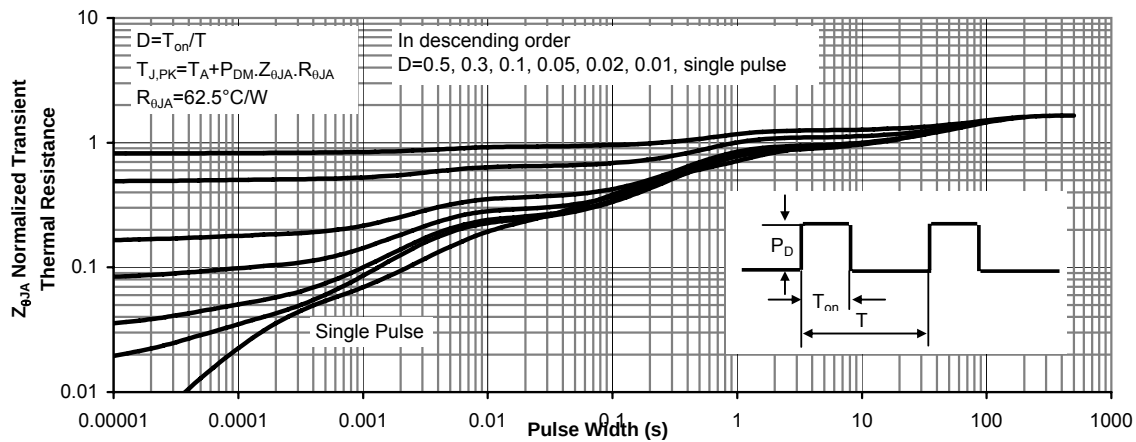


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