



CYPRESS

CY62137CV18 MoBL2™

## 128K x 16 Static RAM

### Features

- **High Speed**
  - 55 ns and 70 ns availability
- **Low voltage range:**
  - CY62137CV18: 1.65V–1.95V
- **Pin Compatible w/ CY62137V18/BV18**
- **Ultra-low active power**
  - Typical Active Current: 0.5 mA @  $f = 1$  MHz
  - Typical Active Current: 1.5 mA @  $f = f_{max}$  (70 ns speed)
- **Low standby power**
- **Easy memory expansion with CE and OE features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

### Functional Description

The CY62137CV18 is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces

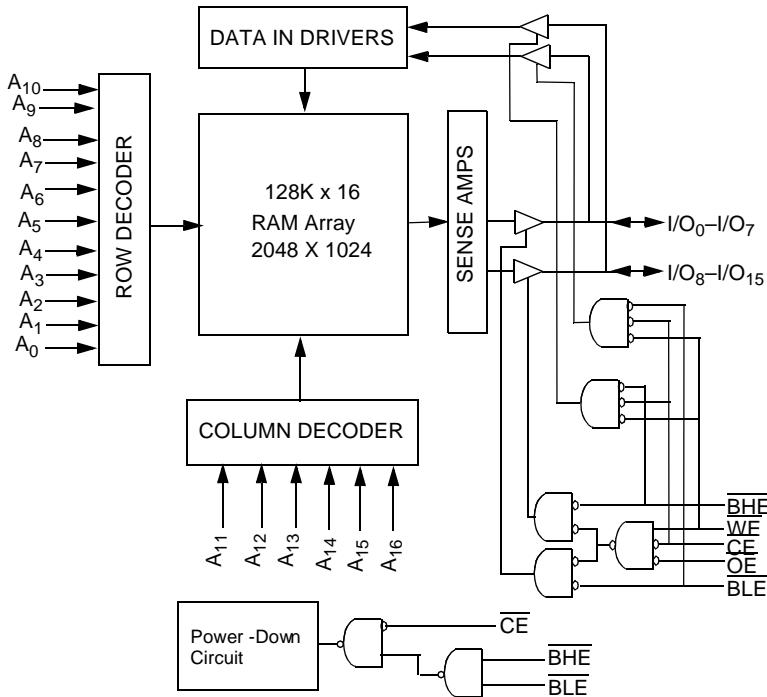
power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (CE HIGH or both BLE and BHE are HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected (CE HIGH), outputs are disabled (OE HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the Truth Table at the back of this data sheet for a complete description of read and write modes.

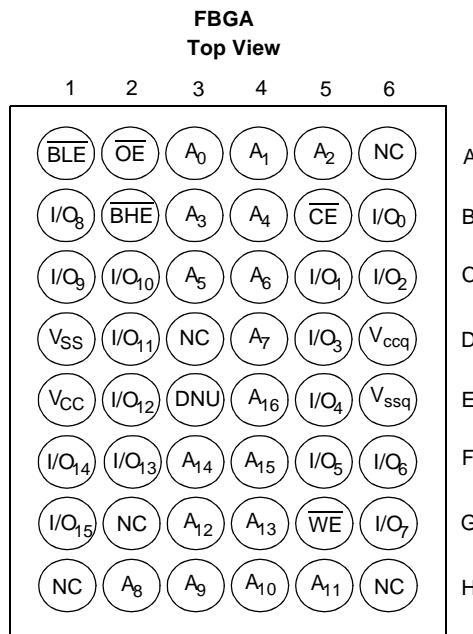
The CY62137CV18 is available in a 48-ball FBGA package.

### Logic Block Diagram



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### Pin Configuration<sup>[1, 2]</sup>



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.2V to +2.4V

DC Voltage Applied to Outputs in High Z State<sup>[3]</sup> ..... -0.2V to V<sub>CC</sub> + 0.2V  
 DC Input Voltage<sup>[3]</sup> ..... -0.2V to V<sub>CC</sub> + 0.2V  
 Output Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

### Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub>
CY62137CV18	Industrial	-40°C to +85°C	1.65V to 1.95V

### Product Portfolio

Product	V <sub>CC</sub> Range			Speed	Power Dissipation (Industrial)				
					Operating (I <sub>CC</sub> )		Standby (I <sub>SB2</sub> )		
					f = 1 MHz				
	V <sub>CC(min.)</sub>	V <sub>CC(typ.)</sub> <sup>[4]</sup>	V <sub>CC(max.)</sub>		Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.	
CY62137CV18	1.65V	1.80V	1.95V	55 ns	0.5 mA	2 mA	2 mA	7 mA	1 μA
				70 ns	0.5 mA	2 mA	1.5 mA	6 mA	

#### Notes:

1. NC pins are not connected to the die.
2. E3 (DNU) can be left as NC or V<sub>SS</sub> to ensure proper application.
3. V<sub>IL(min)</sub> = -2.0V for pulse durations less than 20 ns.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	CY62137CV18-55			CY62137CV18-70			Unit
			Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -0.1$ mA	$V_{CC} = 1.65$ V	1.4			1.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 0.1$ mA	$V_{CC} = 1.65$ V			0.2			V
$V_{IH}$	Input HIGH Voltage			1.4		$V_{CC} + 0.2$ V	1.4		V
$V_{IL}$	Input LOW Voltage			-0.2		0.4	-0.2		V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		-1		+1	-1		$\mu$ A
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled		-1		+1	-1		$\mu$ A
$I_{CC}$	$V_{CC}$ Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	$V_{CC} = 1.95$ V		2	7		1.5	mA
		$f = 1$ MHz	$I_{OUT} = 0$ mA CMOS levels		0.5	2		0.5	mA
$I_{SB1}$	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V $f = f_{MAX}$ (Address and Data Only), $f = 0$ (OE, WE, BHE, and BLE)			1	8		1	$\mu$ A
$I_{SB2}$	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ , $V_{CC} = 1.95$ V							

**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ C$ , $f = 1$ MHz	6	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = V_{CC(\text{typ})}$	8	pF

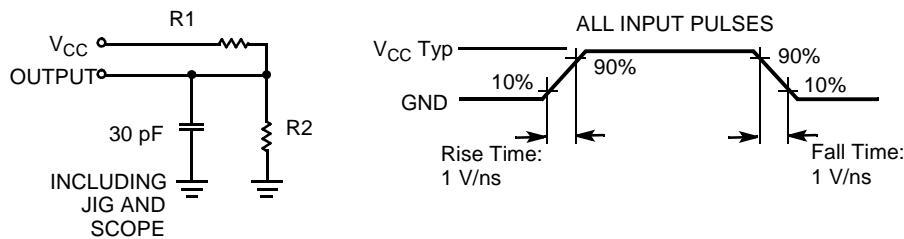
**Thermal Resistance**

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient) <sup>[5]</sup>	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	$\Theta_{JA}$	55	$^\circ C/W$
Thermal Resistance (Junction to Case) <sup>[5]</sup>		$\Theta_{JC}$	16	$^\circ C/W$

**Note:**

5. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

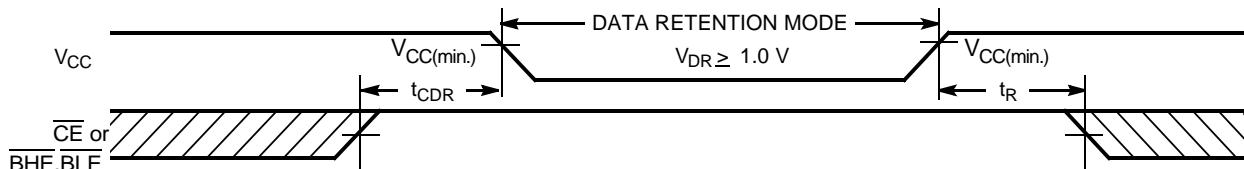


Parameters	1.8V	UNIT
R1	13500	Ohms
R2	10800	Ohms
R <sub>TH</sub>	6000	Ohms
V <sub>TH</sub>	0.80	Volts

## Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.0		1.95	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.0V CE $\geq$ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> $\geq$ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> $\leq$ 0.2V		0.5	5	$\mu$ A
t <sub>CDR</sub> <sup>[5]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[6]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

## Data Retention Waveform<sup>[7]</sup>



### Notes:

6. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub>  $\geq$  100  $\mu$ s or stable at V<sub>CC(min.)</sub>  $\geq$  100  $\mu$ s.
7. BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

**Switching Characteristics** Over the Operating Range<sup>[8]</sup>

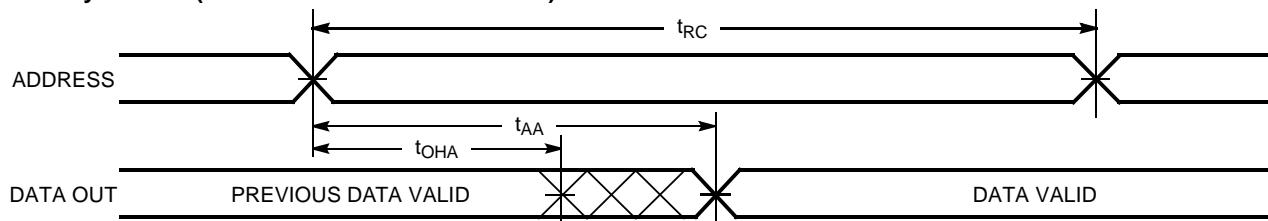
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	55		70		ns
$t_{AA}$	Address to Data Valid		55		70	ns
$t_{OHA}$	Data Hold from Address Change	10		10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		55		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[9]</sup>	5		5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[9, 10]</sup>		20		25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[9]</sup>	5		10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[9, 10]</sup>		20		25	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		55		70	ns
$t_{DBE}$	BLE/BHE LOW to Data Valid		55		70	ns
$t_{LZBE}$	BLE/BHE LOW to Low Z <sup>[9]</sup>	5		5		ns
$t_{HZBE}$	BLE/BHE HIGH to High Z <sup>[9, 10]</sup>		20		25	ns
<b>WRITE CYCLE<sup>[11]</sup></b>						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	40		60		ns
$t_{AW}$	Address Set-Up to Write End	40		60		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	40		50		ns
$t_{BW}$	BLE/BHE LOW to Write End	40		60		ns
$t_{SD}$	Data Set-Up to Write End	25		30		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[9, 10]</sup>		20		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[9]</sup>	5		10		ns

**Notes:**

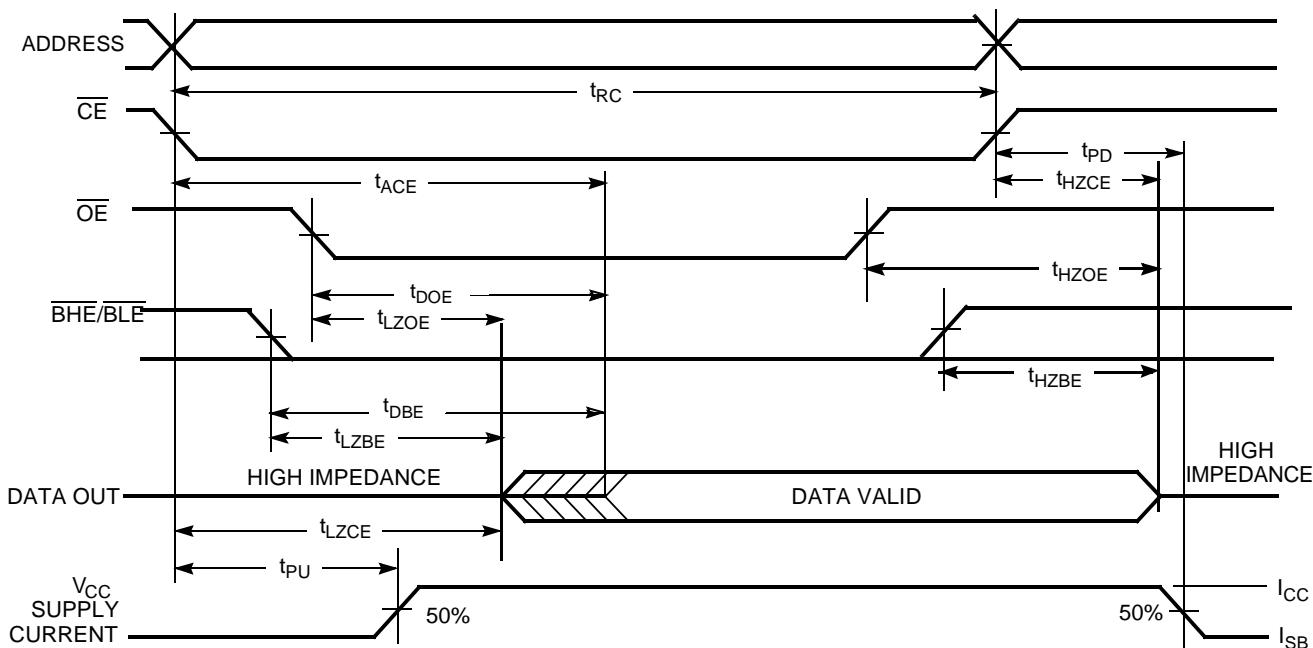
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of  $V_{CC(\text{typ})}/2$ , input pulse levels of 0 to  $V_{CC(\text{typ})}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
9. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
10.  $t_{LZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$  and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
11. The internal write time of the memory is defined by the overlap of WE, CE =  $V_{IL}$ , BHE and/or BLE =  $V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

## Read Cycle No. 1(Address Transition Controlled)<sup>[12, 13]</sup>



## Read Cycle No. 2 (OE Controlled) [13, 14]



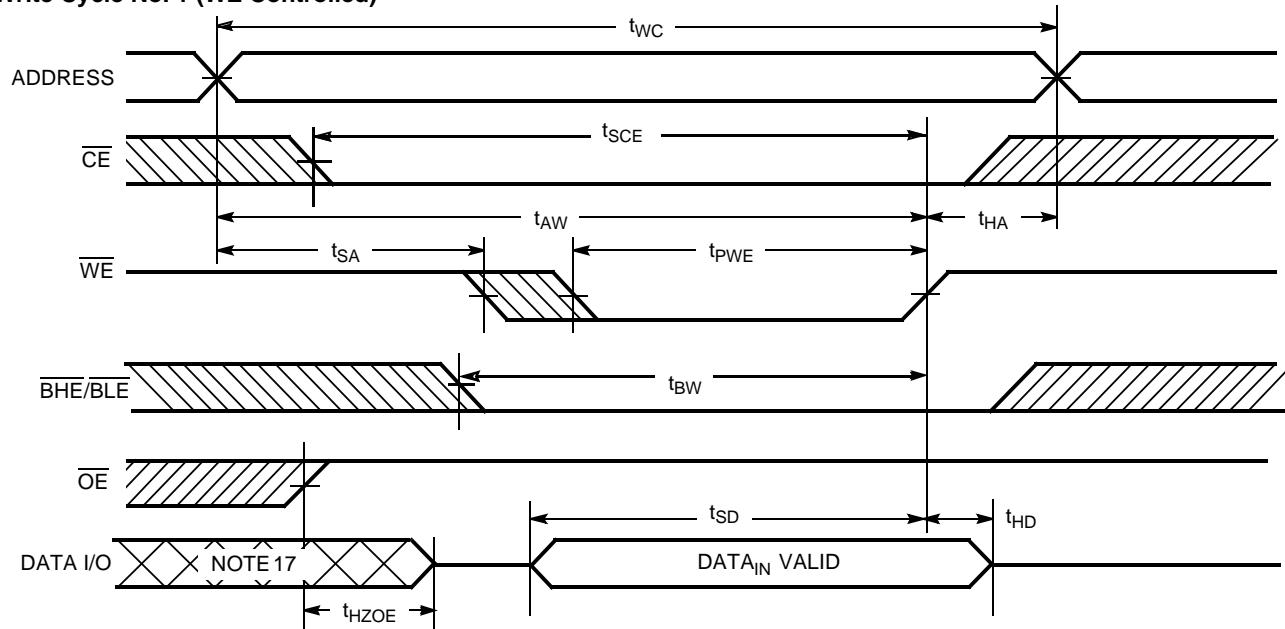
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**Notes:**

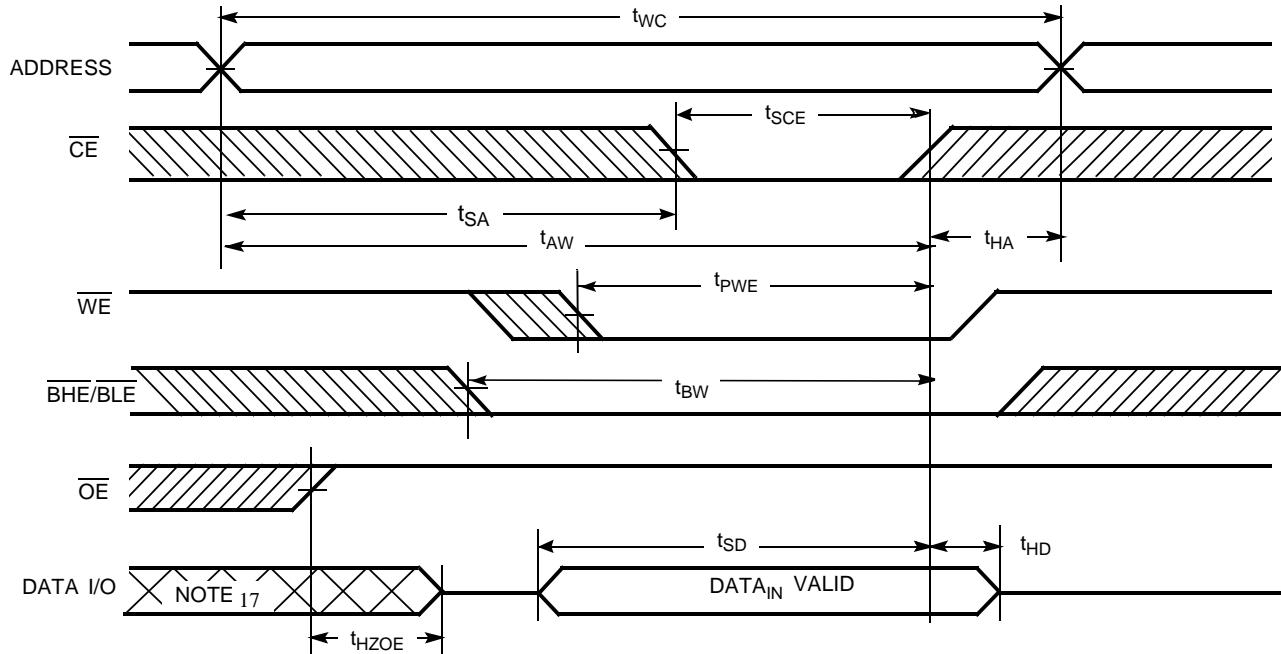
12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE} = V_{IL}$  and/or  $\overline{BLE} = V_{IL}$ .
13.  $WE$  is HIGH for read cycle.
14. Address valid prior to or coincident with  $CE$ ,  $BHE$ ,  $BLE$ , transition LOW.

## Switching Waveforms

### Write Cycle No. 1 ( $\overline{WE}$ Controlled) [11, 15, 16]



### Write Cycle No. 2 ( $\overline{CE}$ Controlled) [11, 15, 16]

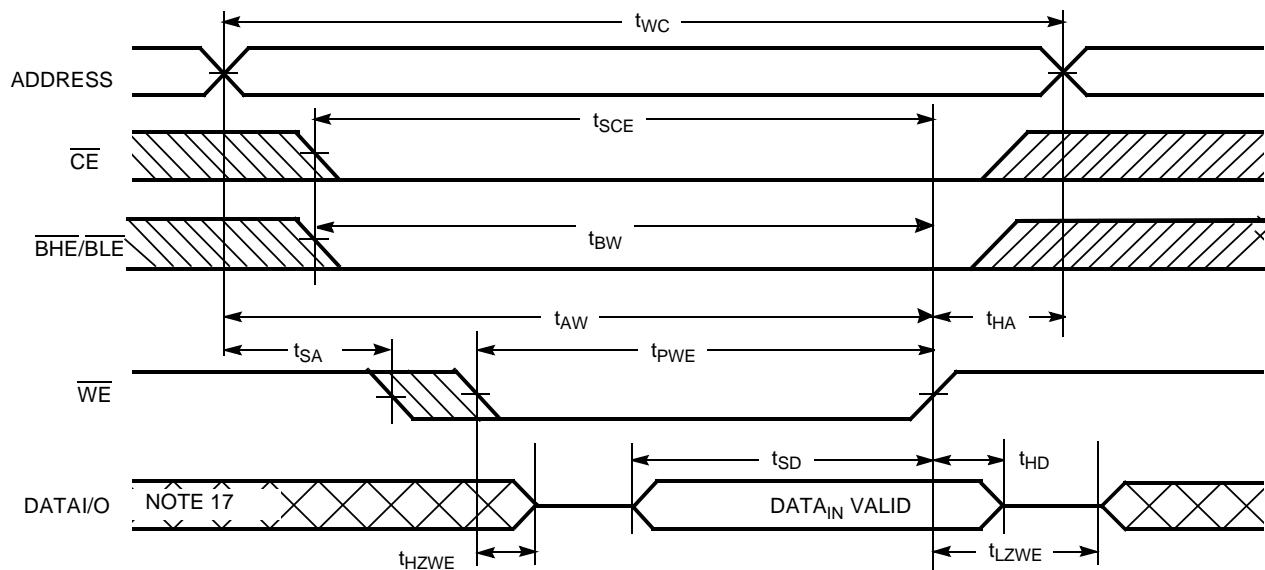


#### Notes:

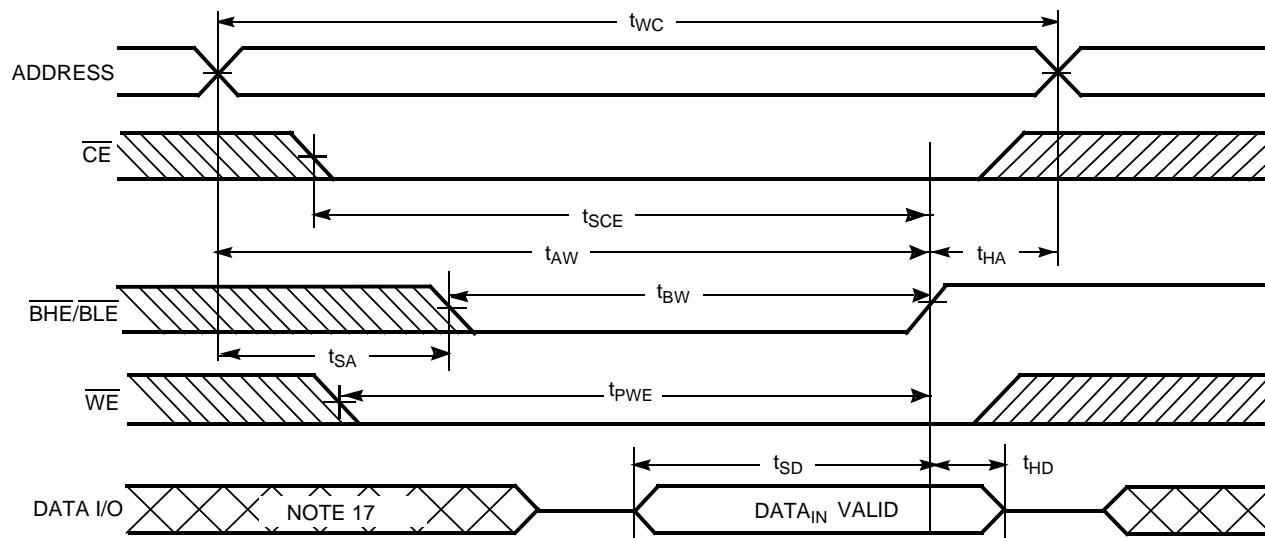
15. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
16. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms

### Write Cycle No. 3 ( $\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)<sup>[16]</sup>

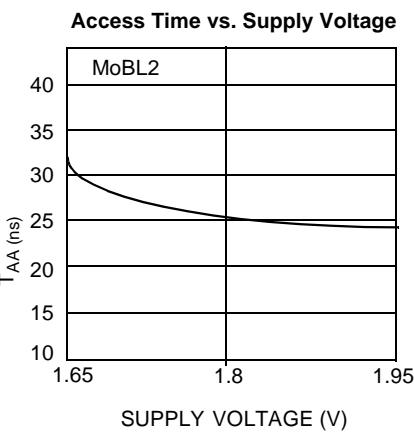
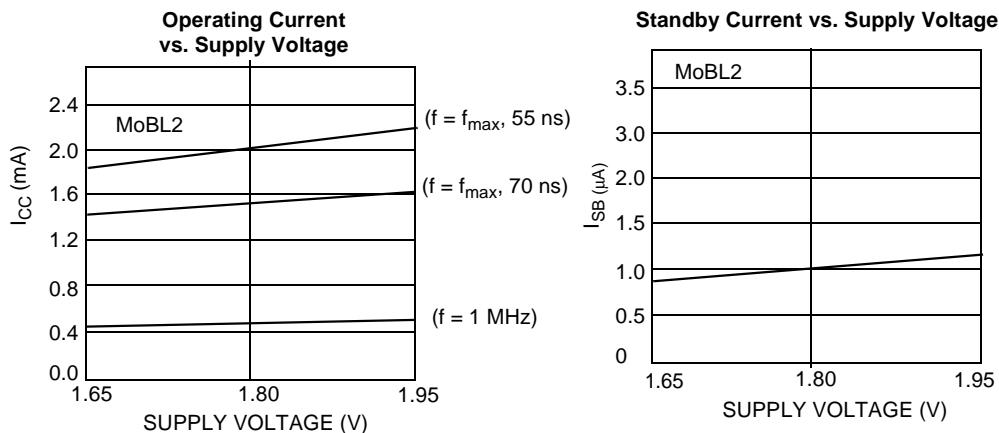


### Write Cycle No. 4 (BHE/BLE Controlled, $\overline{\text{OE}}$ LOW)<sup>[16]</sup>



## Typical DC and AC Characteristics

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(\text{typ})}$  Typ,  $T_A = 25^\circ\text{C}$ .)



## Truth Table

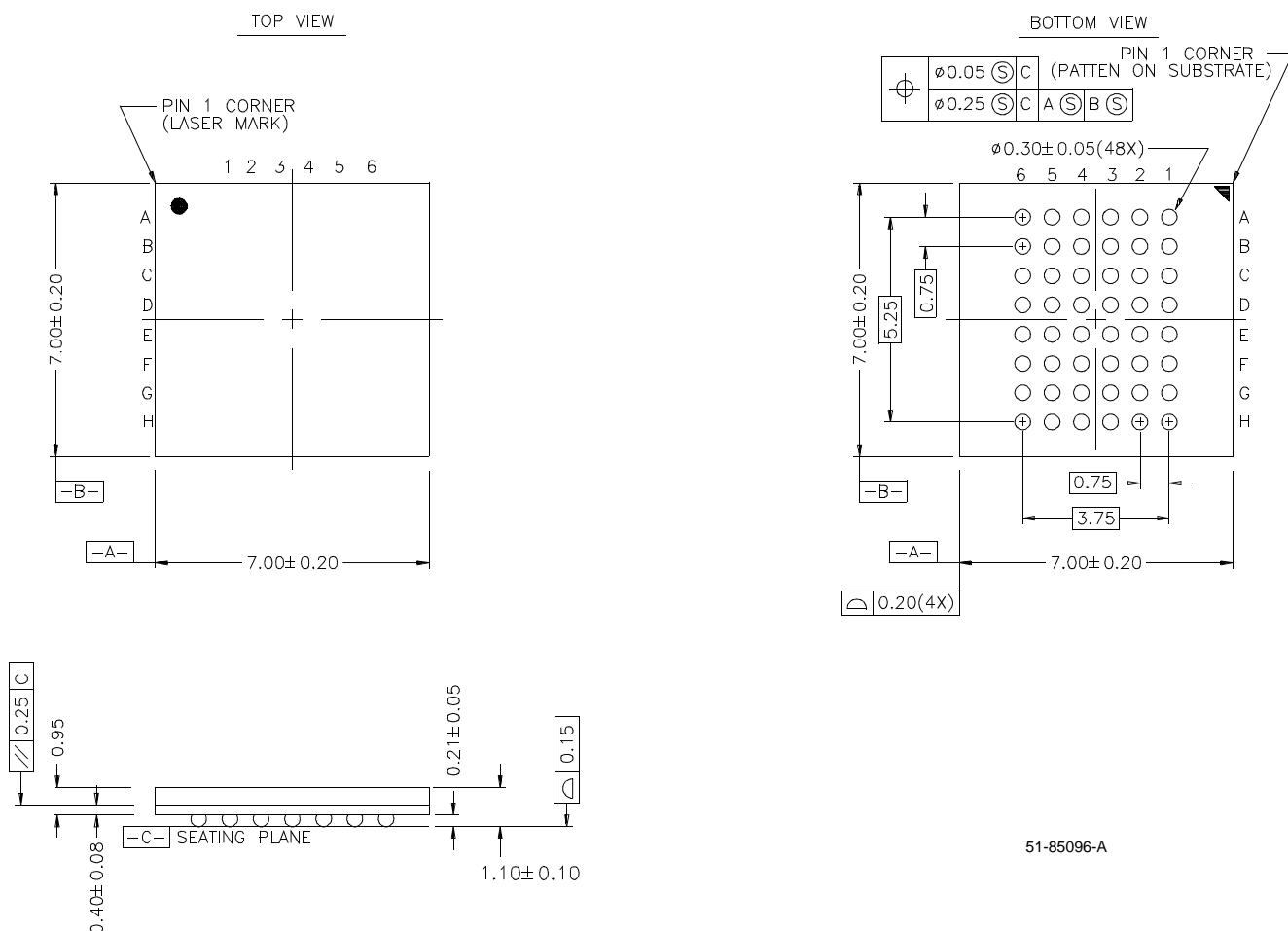
<b>CE</b>	<b>WE</b>	<b>OE</b>	<b>BHE</b>	<b>BLE</b>	<b>Inputs/Outputs</b>	<b>Mode</b>	<b>Power</b>
H	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	X	X	H	H	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In (I/O <sub>0</sub> –I/O <sub>15</sub> )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Write	Active ( $I_{CC}$ )

## Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62137CV18LL-70BAI	BA48A	48-Ball Fine Pitch BGA	Industrial
55	CY62137CV18LL-55BAI			

## Package Diagram

48-Ball (7.00 mm x 7.00 mm x 1.20 mm) Fine Pitch BGA BA48A



**Document Title: CY62137CV18 MoBL2™, 128K x 16 Static RAM**  
**Document Number: 38-05017**

<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	106265	5/7/01	HRT/MGN	New Data Sheet
*A	108941	08/24/01	MGN	From Preliminary to Final
*B	110572	11/02/01	MGN	Format standardization. Improved Typical I <sub>cc</sub> @ f = 1 MHz for 55 ns & 70 ns and Max I <sub>cc</sub> @ f = f <sub>MAX</sub> for 70 ns. Improved Typical and Max I <sub>CCDR</sub> .