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Description

PD70210, PD70210A & PD70210AL is an advanced PD Interface Controller (Front-end IC) for Powered Devices in PoE applications. It supports IEEE802.3af, IEEE802.3at, HDBaseT, and general 2/4-pair configurations.

PD70210, PD70210A & PD70210AL includes an advanced classification block that supports 2, 3, 4, and 6 event classification. Using the SUPP_Sx pins it also identifies which of the four pairs of the cable actually receives power and generates appropriate flags.

The IC features an internal bleeder for discharging the input capacitor of the DC/DC converter rapidly, so as to ensure fast re-detection and port power-up in case of sudden removal and re-insertion of Ethernet cable into RJ-45.

Features

- ◆ Supports IEEE802.3af/at, HDBaseT, and other 2-pair/4-pair configurations.
- ◆ PD detection & programmable classification
- ◆ 2,3,4, and 6 event classification
- ◆ Integrated 0.3Ω isolating (series-pass) FET
- ◆ Inrush current limiting
- ◆ Wall adapter support (PD70210A and PD70210AL Only)
- ◆ Less than 5μA offset current during detection
- ◆ Lead-free DFN-16 / QFN-38 package

Applications

- ◆ HDBaseT up to 95 Watts
- ◆ IEEE802.3af and 802.3at
- ◆ Indoor and outdoor PoE

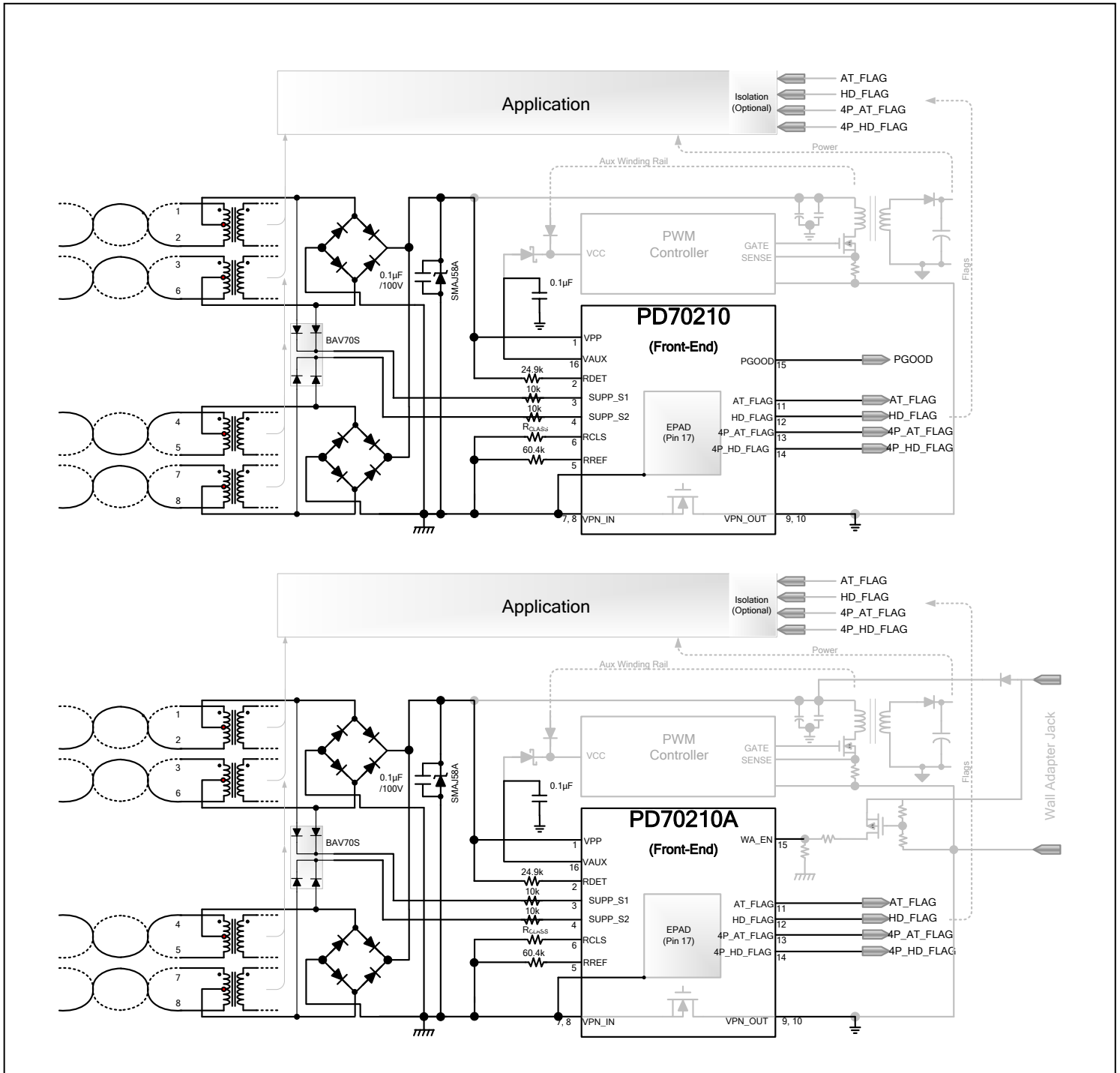
PD70210/PD70210A/PD70210AL

Front-End PD Interface Controller for
AF/AT/UPOE/HDBaseT/4-pair PoE Applications



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Typical application



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PD70210/PD70210A/PD70210AL

Front-End PD Interface Controller for AF/AT/UPOE/HDBaseT/4-pair PoE Applications

Pin Configuration

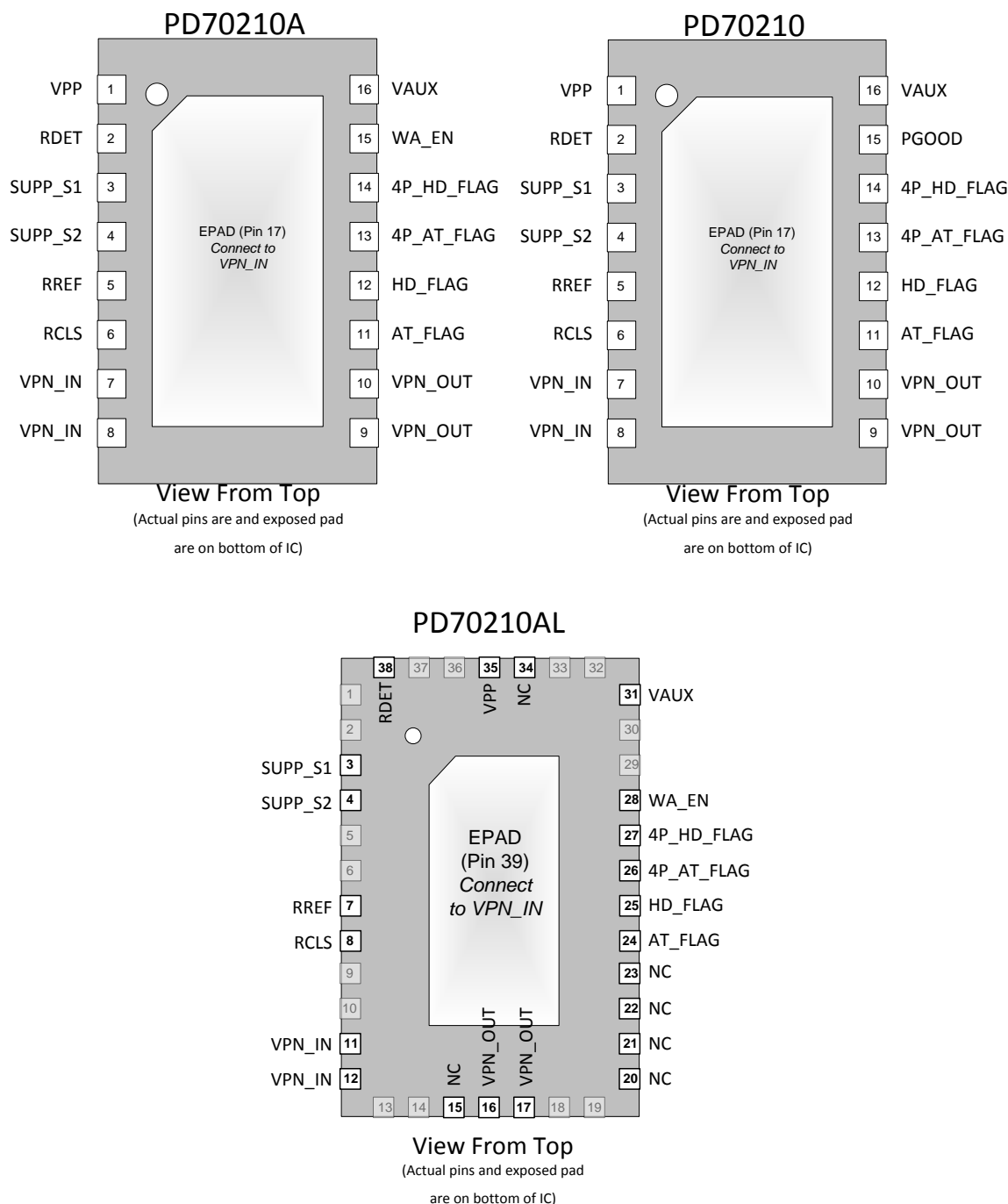


Figure 2: Pinout

** Shaded pins are not exist

PD70210/PD70210A/PD70210AL

Front-End PD Interface Controller for
AF/AT/UPOE/HDBaseT/4-pair PoE Applications



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Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type	Part Marking
-40°C to 85°C	RoHS compliant, Pb-free	DFN 5 × 4 mm 16L (0.5mm pitch)	PD70210AILD	Bulk	Microsemi Logo 70210A YYWWX* MSC
			PD70210AILD-TR	Tape and Reel	
-40°C to 85°C	RoHS compliant, Pb-free	DFN 5 × 4 mm 16L (0.5mm pitch)	PD70210ILD	Bulk	Microsemi Logo 70210 YYWWX* MSC
			PD70210ILD-TR	Tape and Reel	
-40°C to 85°C	RoHS compliant, Pb-free	QFN 5 × 7 mm 38L (0.5mm pitch)	PD70210ALILQ	Bulk	Microsemi Logo MSC 70210AL YYWWX*
			PD70210ALILQ-TR	Tape and Reel	

*Year / Week / Lot number

Selection guide

Feature / IC	PD70210	PD70210A	PD70210AL
Wall adapter support	NA	Available	Available
2P/4P/HDBaseT support	Available	Available	Available
Package	DFN 5 × 4 mm 16L	DFN 5 × 4 mm 16L	QFN 5 × 7 mm 38L
Clearance between HV pins	0.2mm	0.2mm	1mm



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PD70210/PD70210A/PD70210AL

Front-End PD Interface Controller for AF/AT/UPOE/HDBaseT/4-pair PoE Applications

Pin Description

(PD70210 / PD70210A - DFN 5 × 4 mm 16L)

Pin #	Designator PD70210A	Designator PD70210	Description
1	VPP	VPP	Upper rail of the incoming “48V” PoE rail – from the positive terminal of the two OR-ed bridge rectifiers (the corresponding lower PoE rail is VPN_IN)
2	RDET	RDET	Internally connects to VPN_IN during detection phase and disengages after it is over. A 25K Ω (or 24.9K), 1% resistor is connected between this pin and VPP
3	SUPP_S1	SUPP_S1	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin along with the SUPP_S2 pin can be used to distinguish between 2-pair and 4-pair operation. (For PSEs that operate in 4 pairs but do not generate the classification procedure on both pair but one pair only). Signal is referenced to VPN_IN. Place a 10K resistor in the input of this pin.
4	SUPP_S2	SUPP_S2	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin along with the SUPP_S1 pin can be used to distinguish between 2-pair and 4-pair operation. (For PSEs that operate in 4 pairs but do not generate the classification procedure on both pair but one pair only). Signal is referenced to VPN_IN. Place a 10K resistor in the input of this pin.
5	RREF	RREF	Bias current resistor. A 60.4k, 1% resistor is connected between RREF and IC ground (VPN_IN)
6	RCLS	RCLS	Sets the Class of the PD. Connect R _{CLASS} (programming resistor) between this pin and IC ground (VPN_IN). Allowed values are 133 Ω , 69.8 Ω , 45.3 Ω , and 30.9 Ω for Class 1, 2, 3, and 4 respectively. If R _{CLASS} is not present, the PD will draw up to 3 mA during classification, thus indicating Class 0 (default Type 1) to the PSE. Signal is referenced to VPN_IN
7, 8	VPN_IN	VPN_IN	Lower rail of the incoming “48V” PoE rail – from the negative terminal of the two OR-ed bridge rectifiers (the corresponding upper PoE rail is VPP)
9, 10	VPN_OUT	VPN_OUT	This is in effect, the switched ground for establishing continuity to the PWM section after successful detection, classification, and Power-up. It is connected to the Power ground and PWM controller IC’s ground plane of the DC-DC converter section
11	AT_FLAG	AT_FLAG	Open Drain Output. This pin gets actively pulled low when a Type 2 PD-PSE mutually identifies each other via classification. Signal is referenced to VPN_OUT
12	HD_FLAG	HD_FLAG	Open Drain Output. The pin gets actively pulled low when a 2-pair HDBaseT PD-PSE mutually identify each other via classification. Signal is referenced to VPN_OUT
13	4P_AT_FLAG	4P_AT_FLAG	Open Drain Output. The pin gets actively pulled low when a 4-pair version of a (non-standard) Type 2 PD-PSE mutually identifies each other via classification. Signal is referenced to VPN_OUT
14	4P_HD_FLAG	4P_HD_FLAG	Open Drain Output. The pin gets actively pulled low when a 4-pair HDBaseT PD-PSE mutually identify each other via classification. Signal is referenced to VPN_OUT
15	WA_EN		While this input is low (referenced to VPN_IN) the chip work according to internal flow diagram. When this input is high, it enable wall adapter feature
		PGOOD	Open Drain Output. Power Good output signal from the Front-End stage. This pin gets actively pulled low when power-on occurs. There is a minimum 80 ms delay from the moment VPort exceeds UVLO (~36V), to this PGOOD signal being driven low as per the IEEE standard, to allow the PSE to increase its current limit after power-up is completed. Signal is referenced to VPN_OUT
16	VAUX	VAUX	Auxiliary voltage rail. This can be used to provide a few mA of startup current for the PWM controller (at typically 10.5V). It is gated with the power-good signal internally, so it is released to the PWM controller only when the PoE power is up (power-on phase). Signal is referenced to VPN_OUT
17	EPAD	EPAD	Connected on PCB plane to VPN_IN

PD70210/PD70210A/PD70210AL

Front-End PD Interface Controller for AF/AT/UPOE/HDBaseT/4-pair PoE Applications



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(PD70210AL - QFN 5 × 7 mm 38L)

Pin #	Designator PD70210AL	Description
1-2	NA	
3	SUPP_S1	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin along with the SUPP_S2 pin can be used to distinguish between 2-pair and 4-pair operation. (For PSEs that operate in 4 pairs but do not generate the classification procedure on both pair but one pair only). Signal is referenced to VPN_IN Place a 10K resistor in the input of this pin.
4	SUPP_S2	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin along with the SUPP_S1 pin can be used to distinguish between 2-pair and 4-pair operation. (For PSEs that operate in 4 pairs but do not generate the classification procedure on both pair but one pair only) . Signal is referenced to VPN_IN Place a 10K resistor in the input of this pin.
5-6	NA	
7	RREF	Bias current resistor. A 60.4k, 1% resistor is connected between this and IC ground (VPN_IN)
8	RCLS	Sets the Class of the PD. Connect R _{CLASS} (programming resistor) between this pin and IC ground (VPN_IN). Allowed values are 133 Ω, 69.8 Ω, 45.3 Ω, and 30.9 Ω for Class 1, 2, 3, and 4 respectively. If R _{CLASS} is not present, the PD will draw up to 3 mA during classification, thus indicating Class 0 (default Type 1) to the PSE. Signal is referenced to VPN_IN
9-10	NA	
11-12	VPN_IN	Lower rail of the incoming “48V” PoE rail – from the negative terminal of the two OR-ed bridge rectifiers (the corresponding upper PoE rail is VPP)
13-14	NA	
15	NC	
16-17	VPN_OUT	This is in effect, the switched ground for establishing continuity to the PWM section after successful detection, classification, and Power-up. It is connected to the Power ground and PWM controller IC’s ground plane of the DC-DC converter section
18-19	NA	
20-23	NC	
24	AT_FLAG	Open Drain Output. This pin gets actively pulled low when a Type 2 PD-PSE mutually identifies each other via classification. Signal is referenced to VPN_OUT
25	HD_FLAG	Open Drain Output. The pin gets actively pulled low when a 2-pair HDBaseT PD-PSE mutually identify each other via classification. Signal is referenced to VPN_OUT
26	4P_AT_FLAG	Open Drain Output. The pin gets actively pulled low when a 4-pair version of a (non-standard) Type 2 PD-PSE mutually identifies each other via classification. Signal is referenced to VPN_OUT
27	4P_HD_FLAG	Open Drain Output. The pin gets actively pulled low when a 4-pair HDBaseT PD-PSE mutually identify each other via classification. Signal is referenced to VPN_OUT
28	WA_EN	While this input is low (referenced to VPN_IN) the chip work according to internal flow diagram. When this input is high, it enable wall adapter feature
29-30	NA	
31	VAUX	Auxiliary voltage rail. This can be used to provide a few mA of startup current for the PWM controller (at typically 10.5V). It is gated with the power-good signal internally, so it is released to the PWM controller only when the PoE power is up (power-on phase) . Signal is referenced to VPN_OUT
32-33	NA	

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Front-End PD Interface Controller for AF/AT/UPOE/HDBaseT/4-pair PoE Applications



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34	NC	
35	VPP	Upper rail of the incoming “48V” PoE rail – from the positive terminal of the two OR-ed bridge rectifiers (the corresponding lower PoE rail is VPN_IN)
36-37	NA	
38	RDET	Internally connects to VPN_IN during detection phase and disengages after it is over. A 25K Ω (or 24.9K), 1% resistor is connected between this pin and VPP
39	EPAD	Connected on PCB plane to VPN_IN

PD70210/PD70210A/PD70210AL

Front-End PD Interface Controller for
AF/AT/UPOE/HDBaseT/4-pair PoE Applications



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Functional Block Diagram

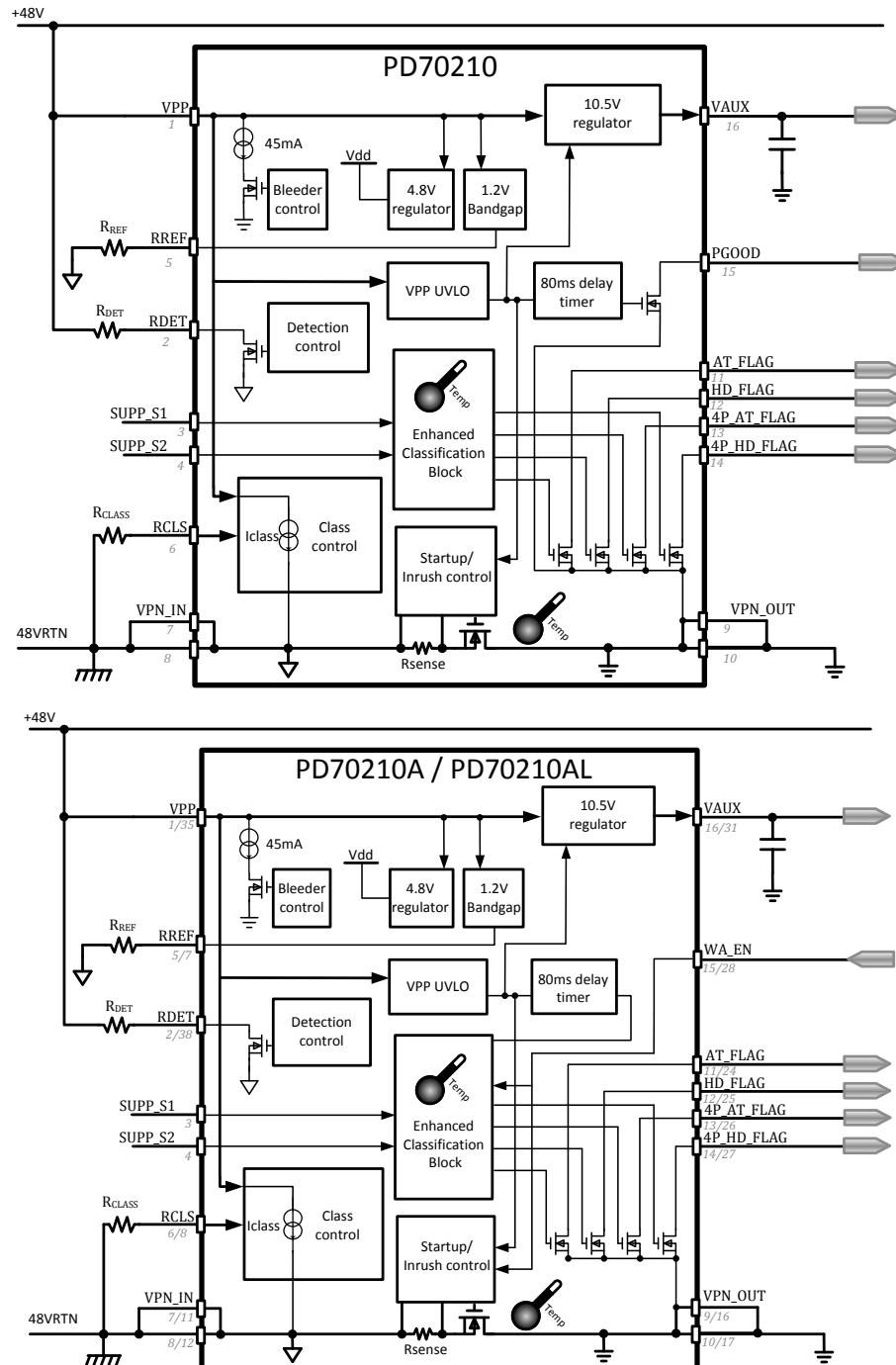


Figure 3: Block Diagram


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Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability. Voltages are with respect to IC ground (VPN_IN) unless otherwise specified.

		Min	Max	Units
VPP, RDET		-0.3	74	V
PGOOD, AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG referenced to VPN_OUT		-0.3	74	V
SUPP_S1, SUPP_S2		0	V _{VPP} + 1.5	V
RREF, RCLS, WA_EN		-0.3	5	V
Junction Temperature		-40	150	°C
Lead Soldering Temperature (40s, reflow)			260	°C
Storage Temperature		-65	150	°C
ESD rating	HBM (PD70210 / PD70210A / PD70210AL)		±1.5 / ±1.25	kV
	MM		±100	V
	CDM		±500	V

Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics. Voltages are with respect to IC ground (VPN_IN).

	Min	Max	Units
VPP	0	57	V
Ambient Temperature*	-40	85	°C
Detection Range	1.1	10.1	V
Mark Event Range	4.9	10.1	V
Class Event Range	13.7	20.9	V

* Corresponding Max Operating Junction Temperature is 125°C.

Thermal Properties

Thermal Resistance	Min	Typ	Max	Units
θ _{JA}		31		°C/W

Note: θ_{Jx} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. θ_{JA} in particular is a function of the PCB construction. Stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).



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Electrical Characteristics

Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating ratings of the device. Typ values state, are either by design or by production testing at 25°C ambient. Voltages are with respect to IC ground (V_{PN_IN}).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input Voltage						
I _{IN}	IC input current with I _{CLASS} off	V _{PP} =55V		1	3	mA
Detection phase						
V _{DET}	Detection range		1.1		10.1	V
R _{DET_TH}	R _{DET} disconnect threshold		10.1		12.8	V
R _{DS_DET_ON}	On-resistance of internal FET during detection				50	Ω
R _{DS_DET_OFF}	Off-resistance of internal FET after detection		2			MΩ
I _{OFFSET_DET}	Input offset current	1.1V ≤ V _{PP} ≤ 10.1V, T _J ≤ 85°C			5	μA
V _{R_DET_ON}	R _{DET} reconnection threshold when V _{PP} goes low		2.8	3.0	4.85	V
Classification phase						
V _{CLS_ON}	Classification sink turn-on threshold		11.4		13.7	V
V _{CLS_OFF}	Classification sink turn-off threshold		20.9		23.9	V
V _{HYS_CLS_ON}	Hysteresis of V _{CLS_ON} threshold			1		V
V _{MARK_TH}	Mark detection threshold (V _{PP} falling)		10.1		11.4	V
I _{MARK}	Current sink in Mark event region		0.25		4	mA

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Front-End PD Interface Controller for AF/AT/UPOE/HDBaseT/4-pair PoE Applications



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Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _{CLASS_CLIM}	Current limit of class current		50	68	80	mA
I _{CLASS}	Classification current sink	R _{CLASS} = not present (Class 0)			3	mA
		R _{CLASS} = 133 Ω (Class 1)	9.5	10.5	11.5	
		R _{CLASS} = 69.8 Ω (Class 2)	17.5	18.5	19.5	
		R _{CLASS} = 45.3 Ω (Class 3)	26.5	28.0	29.5	
		R _{CLASS} = 30.9 Ω (Class 4)	38.0	40.0	42.0	
Isolation FET						
R _{DS(on)}	On resistance	Total resistance between VPN_IN to VPN_OUT; I _{LOAD} < 600mA, -40°C <T _A < 85°C		0.22	0.3	Ω
I _{CLIM_INRUSH}	Inrush current limit		105	240	325	mA
OCP	Overcurrent protection		2.2			A
Undervoltage Lockout						
UVLO _{ON}	Threshold that marks start of Inrush phase		36			V
UVLO _{OFF}	Threshold where pass-FET turns off as VPP collapses		30.5		34.5	V
DC-DC Input Cap Discharger						
I _{CAP_DIS}	Discharge current (PD70210)	12V ≤ VPP ≤ 30V	22.8		60	mA
		7V ≤ VPP ≤ 12V	10			mA
	Discharge current (PD70210A)	7V ≤ VPP ≤ 30V	22.8		60	mA
timer _{dis}	Discharge timer	Time for which discharge circuit is activated	430			ms
References, Rails and Logic						
V _{AUX}	Auxiliary voltage	0mA < I _{AUX} < 4mA	9.5	10.5	12.0	V
I _{AUX_CLIM}	Aux current limit		10		32	mA
V _{REF}	Bias current reference voltage		1.17	1.2	1.23	V

PD70210/PD70210A/PD70210AL

Front-End PD Interface Controller for AF/AT/UPOE/HDBaseT/4-pair PoE Applications



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Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{FLAG_LO}	Low level flag	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG, I _{FLAG} = 3mA			0.4	V
V _{PGOOD_LO}	Power good active low voltage	I _{PGOOD} = 3mA *PD70210 Only			0.4	V
t _{FLAG}	Delay timer between start of inrush and flags declared	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG	80			ms
t _{PGOOD}	Delay timer between start of inrush and power good declared	*PD70210 Only	80			ms
I _{FLAG_max}	Flag Current driving capability	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG	5			mA
I _{PGOOD_max}	Power good current capability	*PD70210 Only	5			mA
V _{SUPP_HI}	SUPP_Sx high voltage threshold	For SUPP_S1 and SUPP_S2	25		35	V
Wall Adapter						
V _{IH}	Input high logic	*PD70210A, PD70210AL Only	2.4			V
V _{IL}	Input low logic	*PD70210A, PD70210AL Only			0.8	V



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Truth Table for Status of Flags

Number of Fingers "N" (N-Event Classification)	SUPP_S1	SUPP_S2	AT_FLAG	HD_FLAG	4P_AT_FLAG	4P_HD_FLAG
1	X	X	Hi Z	Hi Z	Hi Z	Hi Z
2	H	L	0V	Hi Z	Hi Z	Hi Z
2	L	H	0V	Hi Z	Hi Z	Hi Z
2	H	H	0V	Hi Z	0V	Hi Z
3	L	H	0V	0V	Hi Z	Hi Z
3	H	L	0V	0V	Hi Z	
3	H	H	0V	0V	0V	Hi Z
4	X	X	0V	0V	0V	Hi Z
5	RESERVED FOR FUTURE					
6	X	X	0V	0V	0V	0V

Wall Adapter mode (PD70210A/L)

PD70210A / PD70210AL support wall adapter functionality, i.e. by setting WA_EN pin high it will give priority to the wall adapter jack to supply the load.

Thermal Protection

PD70210, PD70210A & PD70210AL are protected from excessive internal temperatures that may occur during various operating procedures. Two temperature sensors are located on the chip, monitoring the temperatures of the following:

- Isolating Switch (pass-FET)
- Classification Current Sink

Each of the over temperature sensor activates a protection mechanism that will disconnect the Isolation (pass) FET or the classification circuit respectively. This protects the device from being permanently damaged or even from long-term degradation.



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Worst-Case Power Estimates

Table below includes minimum guaranteed available power at PD-side (at the entrance of its RJ-45). It takes into account expected channel resistance and imbalances in resistance across the pairs.

PSE Type	Current per pair	Balance between pairs	PSE output Power	Max load Current	Min PSE Voltage	Channel Resistance	PD input Power
TYPE 1 (AF)	350mA	NA	15.4W	350mA	44V	20	12.95W
TYPE 2 (AT)	600mA	NA	30W	600mA	50V	12.5	25.5W
MSCC Extended AT	720mA	NA	36W	720mA	50V	12.5	29.52W
4-Pair (600mA)	600mA	87.33%	60W	1123mA	50V	12.5	48.267W
4-pair (720mA)	720mA	87.33%	72W	1348mA	50V	12.5	56.016W
2-pair HDBaseT	950mA	NA	47.5W	950mA	50V	12.5	36.219W
4-pair HDBaseT	950mA	87.33%	95W	1779mA	50V	12.5	69.096W

PD70210/PD70210A/PD70210AL

Front-End PD Interface Controller for
AF/AT/UPOE/HDBaseT/4-pair PoE Applications

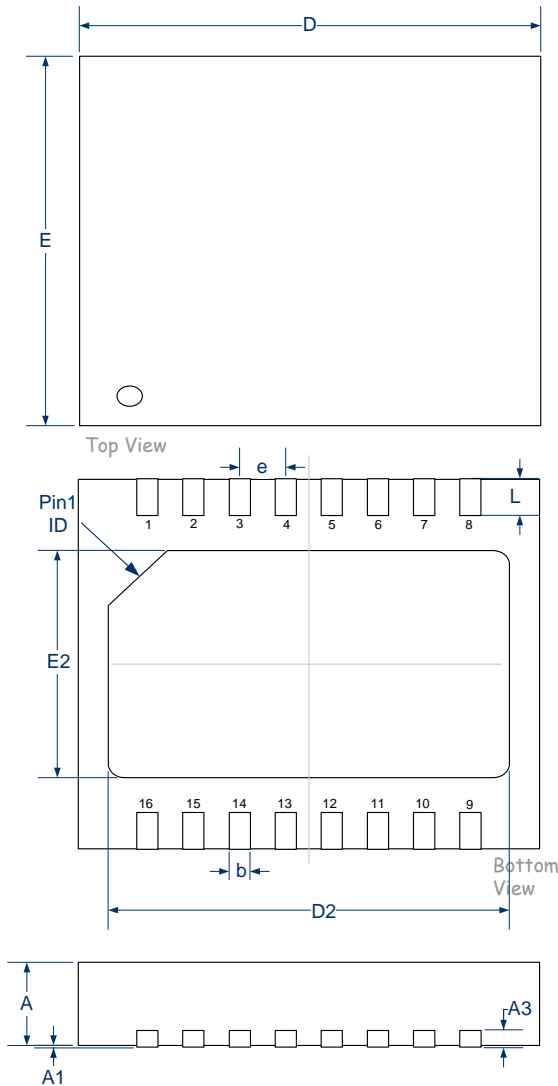


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Package Dimensions

LD

16 Pin Plastic DFN 5x4 mm



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
D	5.00 BSC		0.197 BSC	
E	4.00 BSC		0.157 BSC	
D2	4.20	4.45	0.165	0.175
E2	2.30	2.55	0.091	0.100
e	0.50 BSC		0.0197 BSC	
K	0.20 MIN		0.008 MIN	
L	0.30	0.50	0.012	0.020
b	0.18	0.30	0.007	0.012

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

PD70210/PD70210A/PD70210AL

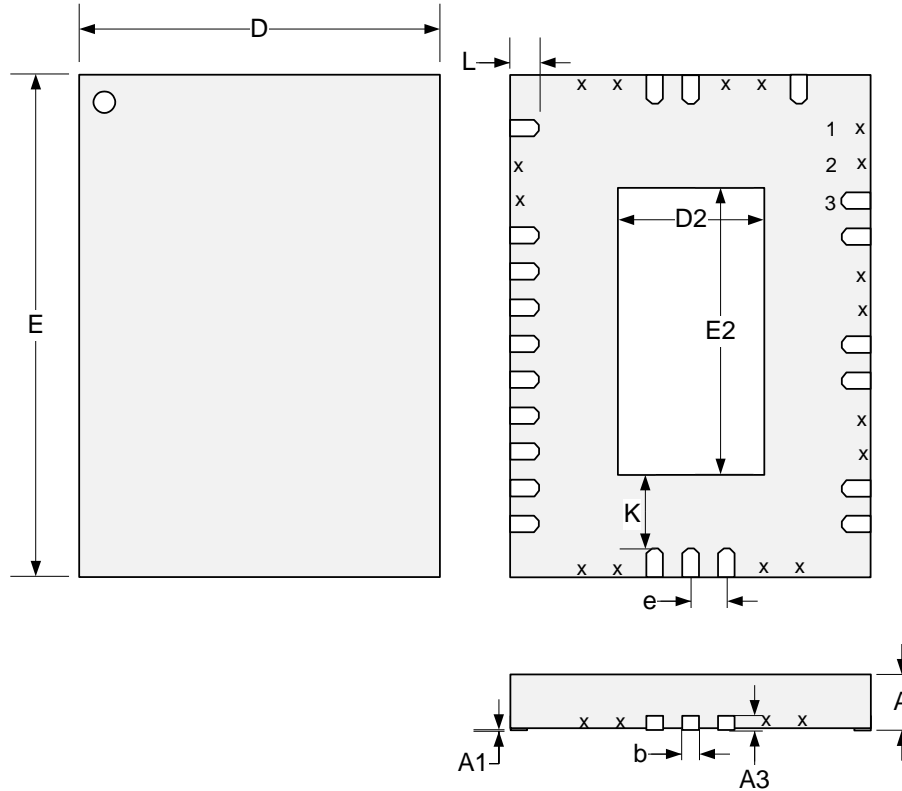
Front-End PD Interface Controller for
AF/AT/UPOE/HDBaseT/4-pair PoE Applications



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LD

38 Pin Plastic QFN 5x7 mm



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	5.00 BSC		0.196 BSC	
E	7.00 BSC		0.275 BSC	
D2	1.85	2.10	0.073	0.083
E2	3.85	4.10	0.152	0.161
e	0.50 BSC		0.020 BSC	
K	1.016	-	0.040	-
L	0.30	0.50	0.012	0.020

Note:

1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in millimeters, inches for reference only.



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Revision History

Revision Level / Date	Para. Affected	Description
1.0 / 10 June 2013	-	Initial Release
1.1 / 16 Oct 2013	-	Fix Vaux description and cap GND symbol
1.2 / 05 Nov 2013	-	Fix Figure 1 RREF
1.34 / 31 Dec 2013	Package	Add new package option PD70210AL 38pin 5 X 7 QFN Update package drawing and add application diagram for the new package Update Flag table and typos
1.36 / 07 Jan 2014		Adding IC marking information
1.37 / 24 Jan 2014		Fix ILQ package information

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