19-1835; Rev 0; 10/00

EVALUATION KIT AVAILABLE

Small, Dual, High-Efficiency Buck Controller for Notebooks

MAX1761

General Description

The MAX1761 dual pulse-width-modulation (PWM), step-down controller provides high efficiency, excellent transient response, and high DC output accuracy in an extremely compact circuit topology. These features are essential for stepping down high-voltage batteries to generate low-voltage CPU core, I/O, and chipset RAM supplies in PC board area critical applications, such as notebook computers and smart phones.

Maxim's proprietary Quick-PWM™ quick-response, constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The MAX1761 achieves high efficiency at reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Efficiency is further enhanced by its ability to drive large synchronous-rectifier MOSFETs. The MAX1761 employs a complementary MOSFET output stage, which reduces component count by eliminating external bootstrap capacitors and diodes.

Single-stage buck conversion allows this device to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the +5V system supply instead of the battery) at a higher switching frequency allows the minimum possible physical size.

The MAX1761 is intended for CPU core, chipset, DRAM, or other low-voltage supplies. The MAX1761 is available in a 16-pin QSOP package. For applications requiring greater output power, refer to the MAX1715 data sheet. For a single-output version, refer to the MAX1762/MAX1791 data sheet.

Applications

Notebooks and PDAs

Digital Cameras

Handy-Terminals

Smart Phones

1.8V/2.5V Logic and I/O Supplies

Quick-PWM and Dual Mode are trademarks of Maxim Integrated Products.

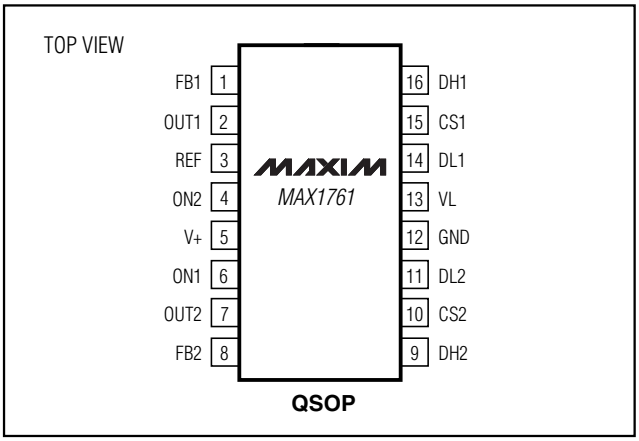
Features

- **Free-Running On-Demand PWM**
- **Selectable Light-Load Pulse-Skipping Operation**
- **±1% Total DC Error in Forced-PWM Mode**
- **5V to 20V Input Range**
- **Flexible Output Voltages**
  - **OUT1: Dual Mode™ Fixed 2.5V or 1V to 5.5V Adjustable**
  - **OUT2: Dual Mode Fixed 1.8V or 1V to 5.5V Adjustable**
- **Output Undervoltage Protection**
- **Complementary Synchronous Buck**
- **No Current-Sense Resistor**
- **4.65V at 25mA Linear Regulator Output**
- **4µA V+ Shutdown Supply Current**
- **5µA VL Shutdown Supply Current**
- **950µA Quiescent Supply Current**
- **Tiny 16-Pin QSOP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1761EEE	-40°C to +85°C	16 QSOP

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +22V
VL to GND .....-0.3V to +6V
VL to V+ .....+0.3V
OUT_, ON2 to GND .....-0.3V to +6V
ON1, DH_ to GND .....-0.3V to (V+ + 0.3V)
FB_, REF, DL_ to GND.....-0.3V to (VL + 0.3V)
CS_ to GND .....-2V to (V+ + 0.3V)
REF Short Circuit to GND .....Continuous

Continuous Power Dissipation
16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature.....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, C_{VL} = 4.7µF, C_{REF} = 0.1µF, VL not externally driven unless otherwise noted, **T_A = 0°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLERS							
Input Voltage Range	V+	(Note 2)		4.5		20	V
DC Output Voltage Accuracy (Note 3)	$V_{OUT\_}$	V+ = 4.5V to 20V, VL = 4.75V to 5.25V, ON2 = VL	FB_ = OUT_	0.99	1	1.01	
			FB1 = GND	2.475	2.5	2.525	V
			FB2 = GND	1.782	1.8	1.818	
Output Voltage Adjust Range				1		5.5	V
OUT_ Input Resistance				80	160	300	kΩ
FB_ Input Bias Current		$V_{FB\_}$ = 1V, VL = 5V		-0.1		0.1	µA
CS_ Input Bias Current		$V_{CS\_}$ = 0, VL = 5V		-1		1	µA
Soft-Start Ramp Time		Zero to full ILIM			1700		µs
On-Time (Note 4)	t_{ON}	V+ = 10V, V_{OUT1} = 2.5V, V_{OUT2} = 1.8V	OUT1	661	735	809	ns
			OUT2	648	720	792	
Minimum Off-Time (Note 4)	t_{OFF}				400	500	ns
BIAS AND REFERENCE							
Quiescent Supply Current	IL	FB1 = FB2 = GND, VL = 5V, V_{OUT1} and V_{OUT2} forced above regulation point			0.60	1.20	mA
	I+	FB1 = FB2 = GND, V_{OUT1} and V_{OUT2} forced above regulation point	VL undriven		0.95	1.70	mA
			VL = 5V		0.38	0.65	
Shutdown Supply Current	IL	VL = 5V, ON1 = ON2 = GND			5	10	µA
	I+	VL = 0, 5V			4	10	µA
VL Output Voltage	VL	I_{LOAD} = 0 to 25mA, V+ = 5V to 20V		4.5	4.65	4.75	V
Reference Voltage	V_{REF}	V+ = 5V to 20V, no load		1.98	2	2.02	V
Reference Load Regulation	I_{REF}	I_{REF} = 0 to 50µA				8	mV
REF Sink Current		REF in regulation		10			µA
REF Fault Lockout Voltage		Falling edge			1.6		V
		Rising edge			1.94		

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, C_{VL} = 4.7µF, C_{REF} = 0.1µF, VL not externally driven unless otherwise noted, **T_A = 0°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAULT PROTECTION						
Output Undervoltage Threshold (Foldback)	$V_{FB,UVFB}$	With respect to the regulation point, no load	60	70	80	%
Output Undervoltage Blanking Time	$V_{FB,UVLO(t)}$	Measured from ON_ signal going high	10		32	ms
Current-Limit Threshold		GND - CS_, positive direction	92	100	108	mV
		GND - CS_, negative direction, ON2 = floating	-135	-120	-105	
		GND - CS_, zero crossing, ON2 = 5V		2.5		
Thermal Shutdown Threshold		Hysteresis = 10°C		160		°C
VL Undervoltage Lockout Threshold	$V_{VL,UVLO}$	Rising edge, hysteresis = 20mV, PWM is disabled below this voltage	4.1		4.4	V
GATE DRIVERS						
DH_ Gate Driver On-Resistance (Pullup)		V+ = 6V to 20V, DH_, high state		3.7	8	Ω
DH_ Gate Driver On-Resistance (Pulldown)		DH_, low state		6.2	10	Ω
DL_ Gate Driver On-Resistance (Pullup)		DL_ , high state		3.4	8	Ω
DL_ Gate Driver On-Resistance (Pulldown)		DL_, low state		2.0	5	Ω
DH_ Gate Driver Source/Sink Current		$V_{DH\_}$ = 3V, V+ = 6V		0.6		A
DL_ Gate Drive Sink Current		$V_{DL\_}$ = 2.5V		0.9		A
DL_ Gate Drive Source Current		$V_{DL\_}$ = 2.5V		0.5		A
LOGIC CONTROLS						
ON_ Logic Input High Voltage			2.05			V
ON2 Logic Input Float Voltage (Forced-PWM Mode)		2.0V < V_{ON1} < VL	1.3	1.7	1.95	V
ON_ Logic Input Low Voltage					0.5	V
ON1 Logic Input Current			-1		1	µA
ON2 Logic High Input Current		V_{ON2} > 2.0V	0	1	3	µA
ON2 Logic Low Input Current		V_{ON2} < 0.5V, V_{ON1} > 2.0V	-2	-1	0	µA
FB_ Dual Mode Threshold			50	100	150	mV

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ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, C_{VL} = 4.7µF, C_{REF} = 0.1µF, VL not externally driven unless otherwise noted, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLERS							
Input Voltage Range	V+	(Note 2)		4.5		20	V
	VL	VL externally driven (Note 2)		4.75		5.25	
DC Output Voltage Accuracy (Note 3)	$V_{OUT\_}$	V+ = 4.5V to 20V, VL = 4.75V to 5.25V, ON2 = VL	FB_ = OUT_	0.99		1.01	
			FB1 = GND	2.475		2.525	V
			FB2 = GND	1.782		1.818	
Output Voltage Adjust Range				1		5.5	V
OUT_ Input Resistance				80		300	kΩ
FB_ Input Bias Current		$V_{FB\_}$ = 1V, VL = 5V		-0.1		0.1	µA
CS_ Input Bias Current		$V_{CS\_}$ = 0, VL = 5V		-1		1	µA
Soft-Start Ramp Time		Zero to full ILIM					µs
On-Time (Note 4)	t_{ON}	V+ = 10V, V_{OUT1} = 2.5V, V_{OUT2} = 1.8V	OUT1	661		809	ns
			OUT2	648		792	
Minimum Off-Time (Note 4)	t_{OFF}	Above regulation point				500	ns
BIAS AND REFERENCE							
Quiescent Supply Current	IL	FB1 = FB2 = GND, VL = 5V, V_{OUT1} and V_{OUT2} forced above regulation point				1.2	mA
	I+	FB1 = FB2 = GND, V_{OUT1} and V_{OUT2} forced above regulation point	VL undriven			1.7	mA
			VL = 5V			0.5	
Shutdown Supply Current	IL	VL = 5V, ON1 = ON2 = GND				10	µA
	I+	VL = 0, 5V				10	µA
VL Output Voltage	VL	I_{LOAD} = 0 to 25mA, V+ = 5V to 20V		4.5		4.75	V
Reference Voltage	V_{REF}	V+ = 5V to 20V, no load		1.98		2.02	V
Reference Load Regulation	I_{REF}	I_{REF} = 0 to 50µA				8	mV
REF Sink Current		REF in regulation		10			µA
FAULT PROTECTION							
Output Undervoltage Threshold (Foldback)	$V_{FB,UVFB}$	With respect to the regulation point, no load		60		80	%
Output Undervoltage Lockout Timer	$V_{FB,UVLO(t)}$	Measured from ON_ signal going high		10		32	ms
Current-Limit Threshold		GND – CS_, positive direction		92		108	mV
		GND – CS_, negative direction, ON2 = floating		-135		-105	
VL Undervoltage Lockout Threshold	$V_{VL,UVLO}$	Rising edge, hysteresis = 20mV, PWM is disabled below this voltage		4.1		4.4	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, C_{VL} = 4.7µF, C_{REF} = 0.1µF, VL not externally driven unless otherwise noted, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVERS						
DH_ Gate Driver On-Resistance (Pullup)		V+ = 6V to 20V, DH_, high state			8	Ω
DH_ Gate Driver On-Resistance (Pulldown)		DH_, low state			10	Ω
DL_ Gate Driver On-Resistance (Pullup)		DL_, high state			8	Ω
DL_ Gate Driver On-Resistance (Pulldown)		DL_, low state			5	Ω
DH_ Gate Driver Source/Sink Current		$V_{DH\_}$ = 3V, V+ = 6V				A
DL_ Gate Drive Sink Current		$V_{DL\_}$ = 2.5V				A
DL_ Gate Driver Source Current		$V_{DL\_}$ = 2.5V				A
LOGIC CONTROLS						
ON_ Logic Input High Voltage			2.05			V
ON2 Logic Input Float Voltage (Forced-PWM Mode)		V_{ON1} > 2.0V	1.3		1.95	V
ON_ Logic Input Low Voltage					0.5	V
ON1 Logic Input Current			-1		1	µA
ON2 Logic High Input Current		V_{ON2} > 2.0V	0		3	µA
ON2 Logic Low Input Current		V_{ON2} < 0.5V, V_{ON1} > 2.0V	-2		0	µA
FB_ Dual Mode Threshold			50		150	mV

Note 1: Specifications to -40°C are guaranteed by design, not production tested.

Note 2: If V+ is less than 5V, V+ must be connected to VL. If VL is connected to V+, V+ must be between 4.5V and 5.5V.

Note 3: DC output accuracy specifications refer to the trip-level error of the error amplifier. The output voltage will have a DC regulation higher than the trip level by 50% of the ripple. In PFM mode, the output will rise by approximately 1.5% when transitioning from continuous conduction to no load.

Note 4: One-shot times are measured at the DH pin (V+ = 15V, C_{DH} = 400pF, 90% point to 90% point). Actual in-circuit times may be different due to MOSFET switching speeds.This effect can also cause the switching frequency to vary.

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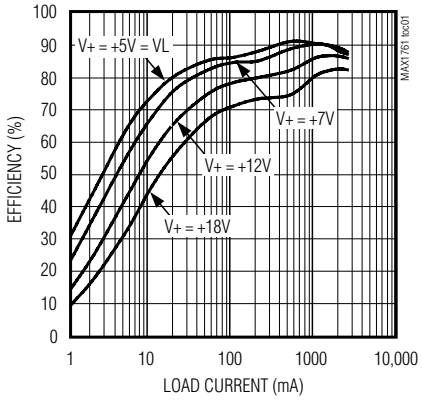
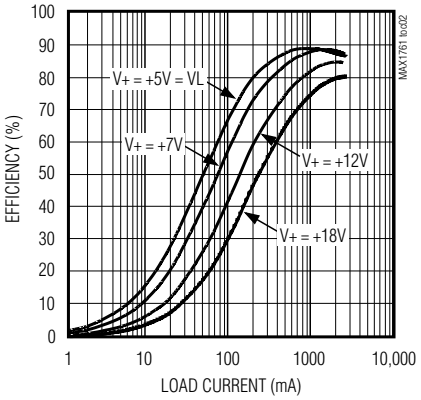
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

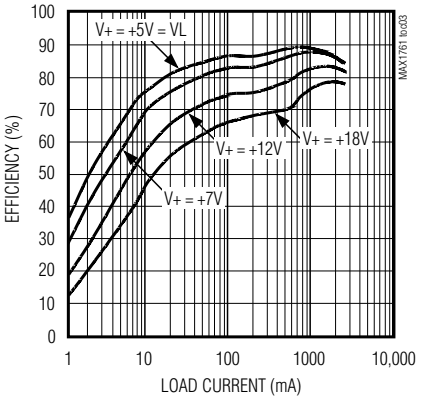
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 2.5V, SKIP MODE)



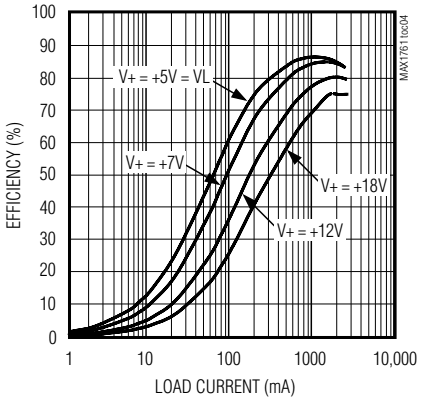
EFFICIENCY vs. LOAD CURRENT (2.5V, PWM MODE)



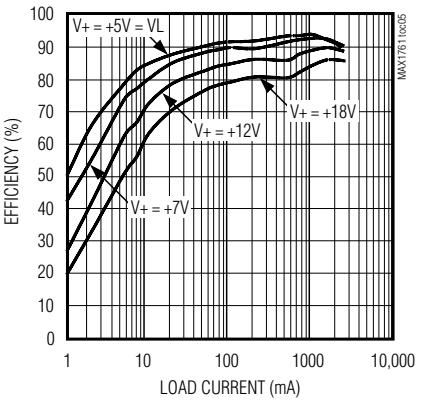
EFFICIENCY vs. LOAD CURRENT (1.8V, SKIP MODE)



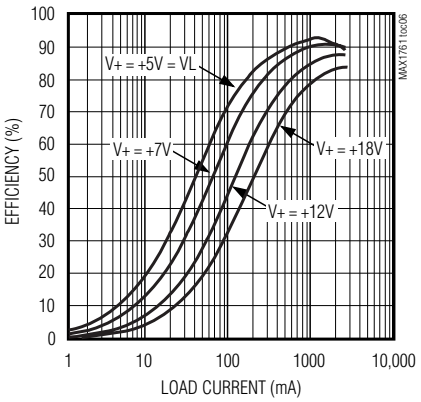
EFFICIENCY vs. LOAD CURRENT (1.8V, PWM MODE)



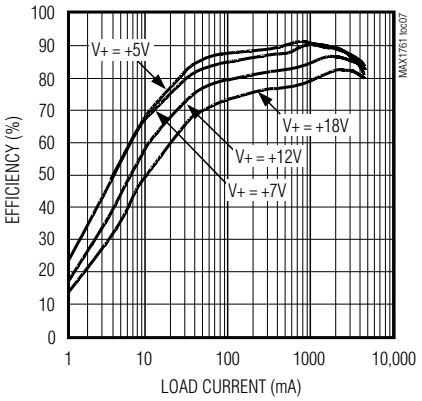
EFFICIENCY vs. LOAD CURRENT (3.3V, SKIP MODE)



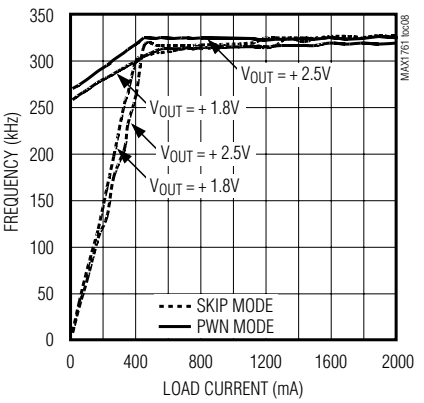
EFFICIENCY vs. LOAD CURRENT (3.3V, PWM MODE)



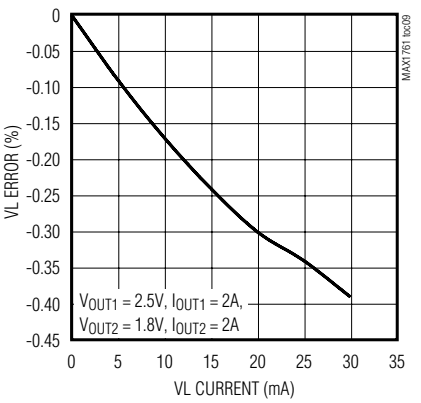
EFFICIENCY vs. LOAD CURRENT (2.5V, SKIP MODE, 3.5A COMPONENTS)



FREQUENCY vs. LOAD CURRENT



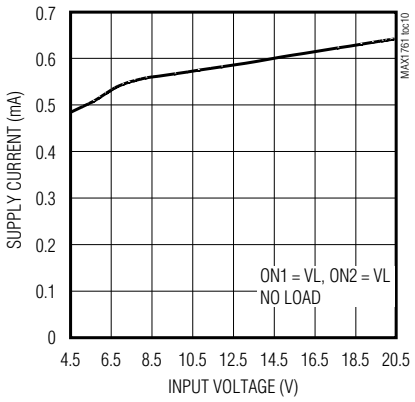
VL VOLTAGE vs. OUTPUT CURRENT



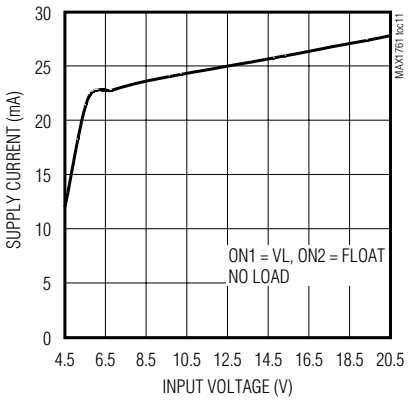
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

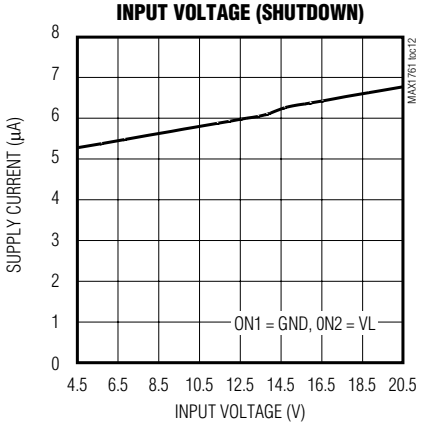
SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP MODE)



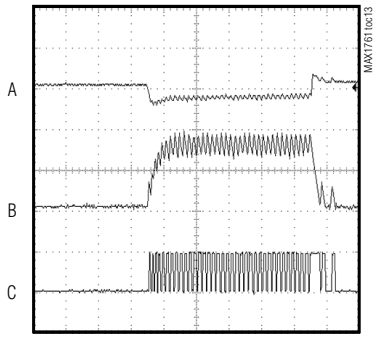
SUPPLY CURRENT vs. INPUT VOLTAGE (PWM MODE)



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (SHUTDOWN)



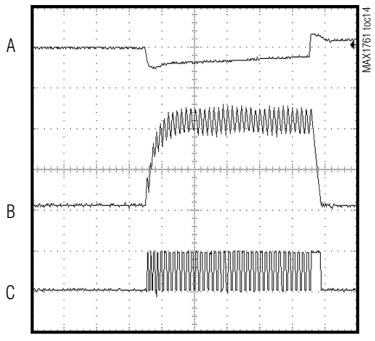
LOAD-TRANSIENT RESPONSE (2.5A COMPONENTS, V_{OUT} = 2.5V)



20 µs/div

A: V_{OUT}, AC-COUPLED, 10mV/div
B: INDUCTOR CURRENT, 1A/div
C: DL1, 5V/div

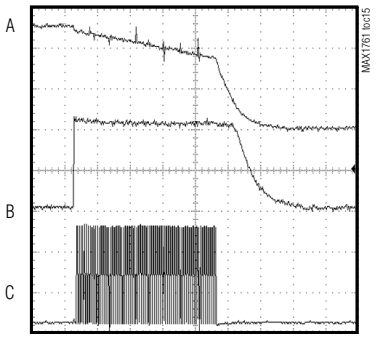
LOAD-TRANSIENT RESPONSE (2.5A COMPONENTS, V_{OUT} = 1.8V)



20 µs/div

A: V_{OUT}, AC-COUPLED, 5mV/div
B: INDUCTOR CURRENT, 1A/div
C: DL1, 5V/div

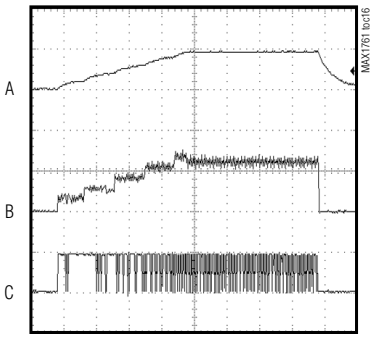
OUTPUT OVERLOAD WAVEFORMS (I_{OUT} = 4V, V_{OUT} = 2.5V)



100 µs/div

A: V_{OUT}, 1V/div
B: INDUCTOR CURRENT, 2A/div
C: DL1, 2V/div

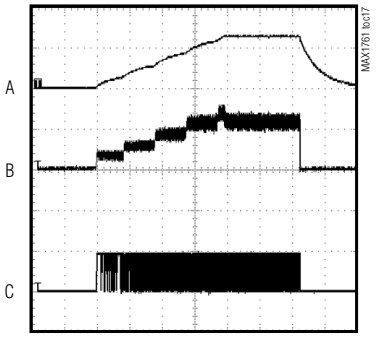
STARTUP AND SHUTDOWN WAVEFORMS (V_{OUT} = 1.8V)



500 µs/div

A: V_{OUT}, 2V/div
B: INDUCTOR CURRENT, 2A/div
C: DL1, 5V/div

STARTUP AND SHUTDOWN WAVEFORMS (V_{OUT} = 2.5V)



500 µs/div

A: V_{OUT}, 2V/div
B: INDUCTOR CURRENT, 2A/div
C: DL1, 5V/div

Small, Dual, High-Efficiency Buck Controller for Notebooks

Pin Description

PIN	NAME	FUNCTION	
1	FB1	Feedback Input for the 2.5V PWM. Connect FB1 to GND for a fixed 2.5V output. Connect a resistive voltage-divider to FB1 to adjust OUT1 from 1V to 5.5V. FB1 regulates to 1V (see *Adjusting V_{OUT}* section) .	
2	OUT1	Output Voltage Connection for PWM1. OUT1 senses the output voltage to set the regulator on-time and is connected internally to a 160kΩ feedback input in fixed-output mode.	
3	REF	2V Reference Voltage Output. Bypass REF to GND with 0.1µF (min) capacitor. Can supply 50µA for external loads.	
4	ON2	When ON1 = High, Normal/Forced PWM Mode Selection and OUT2 On/$\overline{\text{Off}}$ Control Input	
		ON2 CONDITION	**MODE SELECTED**
		LOW (ON2 < 0.5V)	OUT1 is enabled in normal mode; OUT2 is shut down.
		HIGH (2V < ON2 < VL)	Both outputs are enabled in normal mode.
		Floating	Both outputs are enabled in forced-PWM mode.
5	V+	Battery Voltage. V+ is the input for the VL regulator and DH gate drivers and is also used for PWM one-shot timing.	
6	ON1	On/$\overline{\text{Off}}$ Control Input. Drive ON1 high to enable the device. Drive ON1 low to enter micropower shutdown mode. Both REF and VL are disabled in shutdown. ON1 may be pinstrapped to V+.	
7	OUT2	Output Voltage Connection for PWM2. OUT2 senses the output voltage to set the regulator on-time and is connected internally to a 160kΩ feedback input in fixed-output mode.	
8	FB2	Feedback Input for the 1.8V PWM. Connect FB2 to GND for a fixed 1.8V output. Connect a resistive voltage-divider to FB2 to adjust OUT2 from 1V to 5.5V. FB2 regulates to 1V (see *Adjusting V_{OUT}* section) .	
9	DH2	High-Side Gate Driver Output for PWM2. Swings between GND and V+.	
10	CS2	Current-Sense Connection for PWM2. Connect CS2 to the drain of the low-side driver. Alternatively, connect CS2 to the junction of the source of the low-side FET and a current-sense resistor to GND.	
11	DL2	Low-Side Gate Driver Output for PWM2. DL2 swings between GND and VL.	
12	GND	Combined Power and Analog Ground	
13	VL	Linear Regulator Output. VL is the output of the 4.65V internal linear regulator, capable of supplying 25mA for external loads. The VL pin also serves as the supply input for the DL gate driver and the analog/logic blocks. VL can be overdriven by an external 5V supply to improve efficiency. Bypass VL to GND with a 4.7µF ceramic capacitor.	
14	DL1	Low-Side Gate Driver Output for PWM1. DL1 swings between GND and VL.	
15	CS1	Current-Sense Connection for PWM1. Connect CS1 to the drain of the low-side driver. Alternatively, connect CS1 to the junction of the source of the low-side FET and a current-sense resistor to GND.	
16	DH1	High-Side Gate Driver Output for PWM1. DH1 swings between GND and V+.	

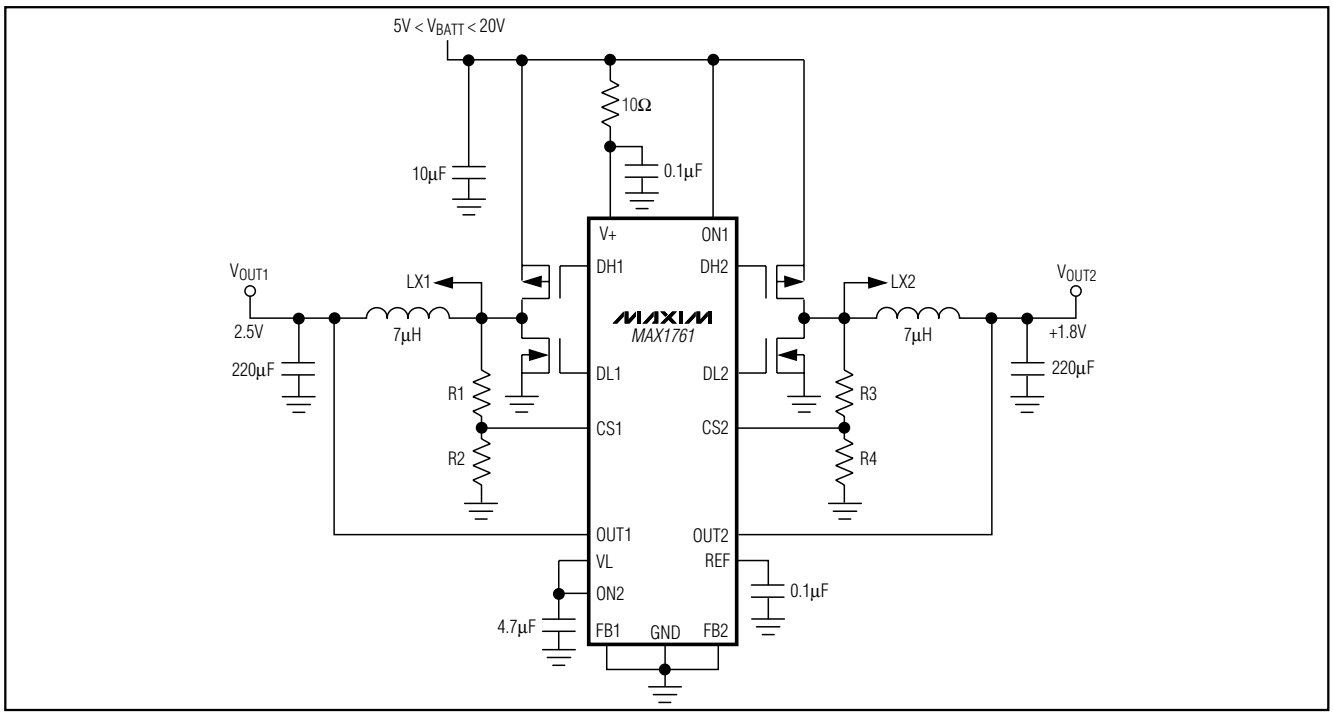


Figure 1. Typical Application Circuit

Typical Application Circuit

The typical application circuit in Figure 1 generates two low-voltage rails for general-purpose use in notebook and subnotebook computers (I/O supply, fixed CPU core supply, DRAM supply). This DC-DC converter steps down a battery or AC adapter voltage to voltages from 1.0V to 5.5V with high efficiency and accuracy. See Table 1 for a list of components for common applications. Table 2 lists component manufacturers.

Detailed Description

The MAX1761 dual buck controller is designed for low-voltage power supplies in notebook and subnotebook computers. Maxim's proprietary Quick-PWM pulse-width modulation circuit (Figure 2) is specifically designed for handling fast load steps while maintaining a relatively constant operating frequency over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs while preventing problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes.

This MAX1761 controls two synchronously rectified outputs with complementary N- and P-channel MOSFETs. Using the P-channel for the high-side MOSFET eliminates external boost capacitors and diodes, reducing PC board area and cost. The MAX1761 can step down input voltages from 5V to 20V, to outputs ranging from 1V to 5.5V on either output. Dual Mode feedback inputs allow fixed output voltages of 2.5V and 1.8V for OUT1 and OUT2, respectively; or, a resistive voltage-divider can be used to adjust the output voltages from 1V to 5.5V. Other appropriate applications for this device are digital cameras, large PDAs, and handy-terminals.

V+ Input and VL +5V Logic Supplies

The MAX1761 has a 5V to 20V input voltage supply range. A linear regulator powers the control logic and other internal circuitry from the input supply pin (V+). The linear regulator's 4.65V output is available at VL and can supply 25mA to external circuitry. When used as an external supply, bypass VL to GND with a 4.7µF capacitor. VL is turned off when the device is in shutdown, and drops to approximately 4V when the device experiences an output voltage fault.

The MAX1761 includes an input undervoltage lockout (UVLO) circuit that prevents the device from switching until VL > 4.25V (max). UVLO ensures there is sufficient drive for the external MOSFETs, prevents the high-side MOSFET from being turned on for near 100% duty cycle, and keeps the output in regulation. The UVLO

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Table 1. Component Selection for Standard Applications

COMPONENT	2.5V AT 2.0A	2.5V AT 3.5A	1.8V AT 2.0A	3.3V AT 2A
Input Range	5V to 18V	5V to 18V	5V to 18V	5V to 18V
Frequency	350kHz	350kHz	250kHz	350kHz
Complementary P- and N-Channel MOSFETs	Fairchild FDS8958A	Siliconix IRF7319	Fairchild FDS8958A	Fairchild FDS8958A
Inductor	7µH Sumida CDRH104-7R0NC	3.5µH Sumida CDRH127-3R5NC	7µH Sumida CDRH104-7R0NC	10µH Sumida CDRH104-100NC
Input Capacitor	10µF, 25V Taiyo Yuden TMK432BJ106KM	2 x 10µF, 25V Taiyo Yuden TMK432BJ106KM	10µF, 25V Taiyo Yuden TMK432BJ106KM	10µF, 25V Taiyo Yuden TMK432BJ106KM
Output Capacitor	330µF, 10V Kemet T510X337K101	2 x 330µF, 10V Kemet T510X337K010	330µF, 10V Kemet T510X337K010	330µF, 10V Kemet T510X337K010
Current-Sense Feedback Resistors	R_1 = Short	R_1 = 1k	R_3 = Short	R_1 = Short
	R_2 = Open	R_2 = 1k	R_4 = Open	R_2 = Open

Table 2. Component Suppliers

SUPPLIER	PHONE	WEB
Fairchild Semiconductor	408-822-2181	www.fairchildsemi.com
Kemet	408-986-0424	www.kemet.com
Panasonic	847-468-5624	www.panasonic. com
Rohm	760-929-2100	www.rohmelectronics.com
Sanyo	619-661-6835	www.secc.co.jp
Siliconix	408-988-8000	www.vishay.com
Sumida	847-956-0666	www.sumida.com
Taiyo Yuden	408-573-4150	www.t-yuden.com

comparator has 40mV hysteresis to prevent startup oscillations on slowly rising input voltages.

If VL is not driven externally, then V+ should be at least 5V to ensure proper operation. If V+ is running from a 5V (±10%) supply, V+ should be externally connected to VL. Overdriving the VL regulator with an external 5V supply also increases the MAX1761's efficiency.

Voltage Reference (REF)

The internal 2V reference is accurate to ±1% (max) over temperature and can supply a 50µA load current. Bypass REF to GND with a 0.1µF capacitor when REF is unloaded. Use a 0.22µF capacitor when applying an external load.

Free-Running Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a constant-on-time, current-mode type with voltage feed-forward (Figure 3). This architecture relies on the output ripple voltage to provide the PWM ramp signal. Thus, the output filter capacitor's ESR acts as a feedback resistor. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time (400ns typical). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

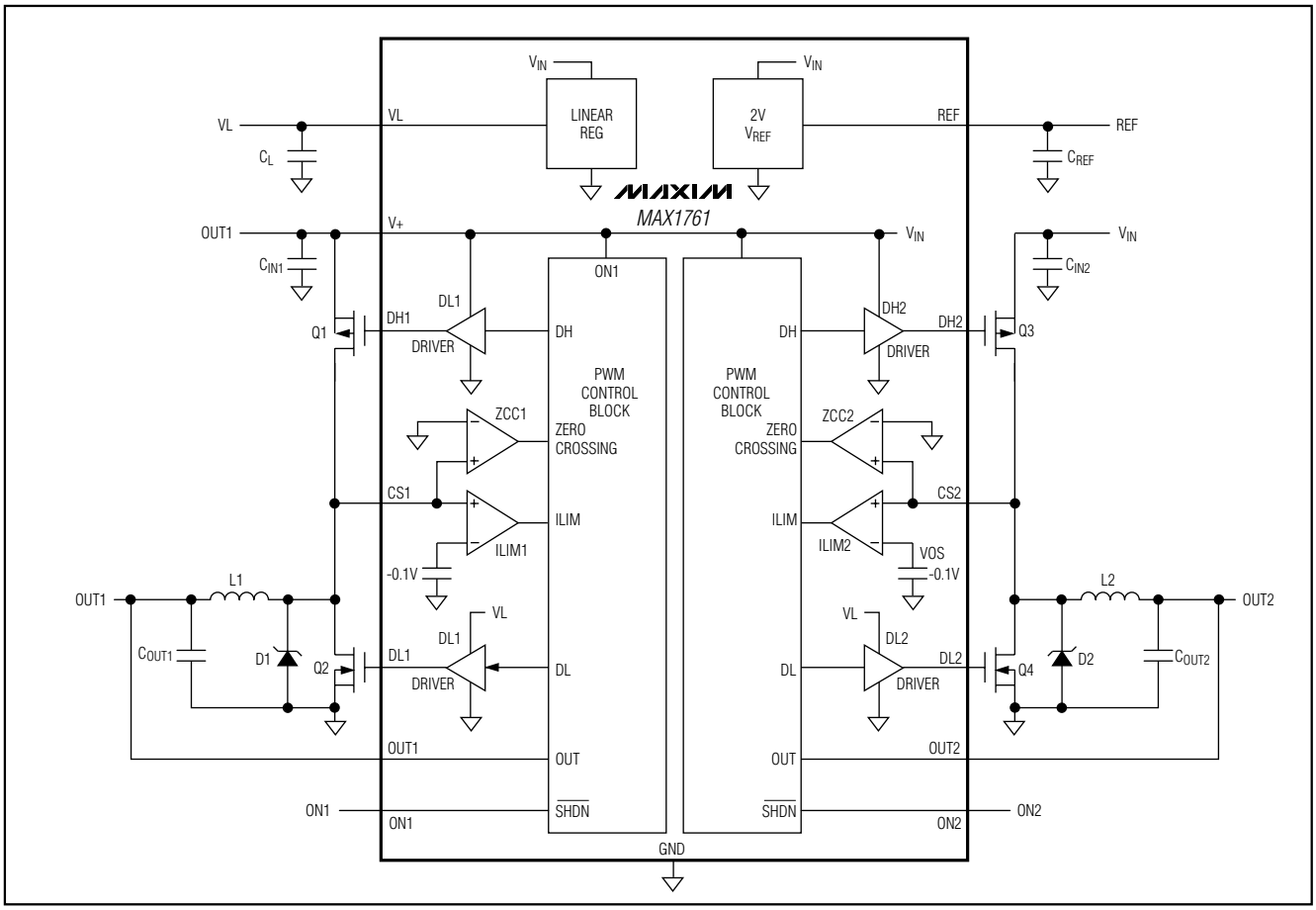

Figure 2. Functional Diagram

On-Time One-Shot

The heart of the PWM core is the one-shot that sets the high-side switch on-time for both controllers. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V+ input, and proportional to the output voltage. This algorithm results in a nearly constant switching frequency despite the absence of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the switching noise occurs at a known frequency and is easily filtered; second, the inductor ripple current remains relatively constant, resulting in predictable output voltage ripple and a relatively simple design procedure. The difference in frequencies between OUT1 and OUT2 prevents audio-frequency "beating" and minimizes crosstalk between the two SMPS. The on-times can be calculated by using the equation below that references the K values listed in Table 3.

$$On\text{-}Time = K\left(\frac{V_{OUT\_} + 0.1V}{V_{IN}}\right)$$

The 0.1V offset term accounts for the expected drop across the low-side MOSFET switch.

Table 3. On-Time One-Shot

DEVICE	K (µs)	MIN (kHz)	TYP (kHz)	MAX (kHz)
OUT1	2.857	318	350	428
OUT2	4.000	227	250	278

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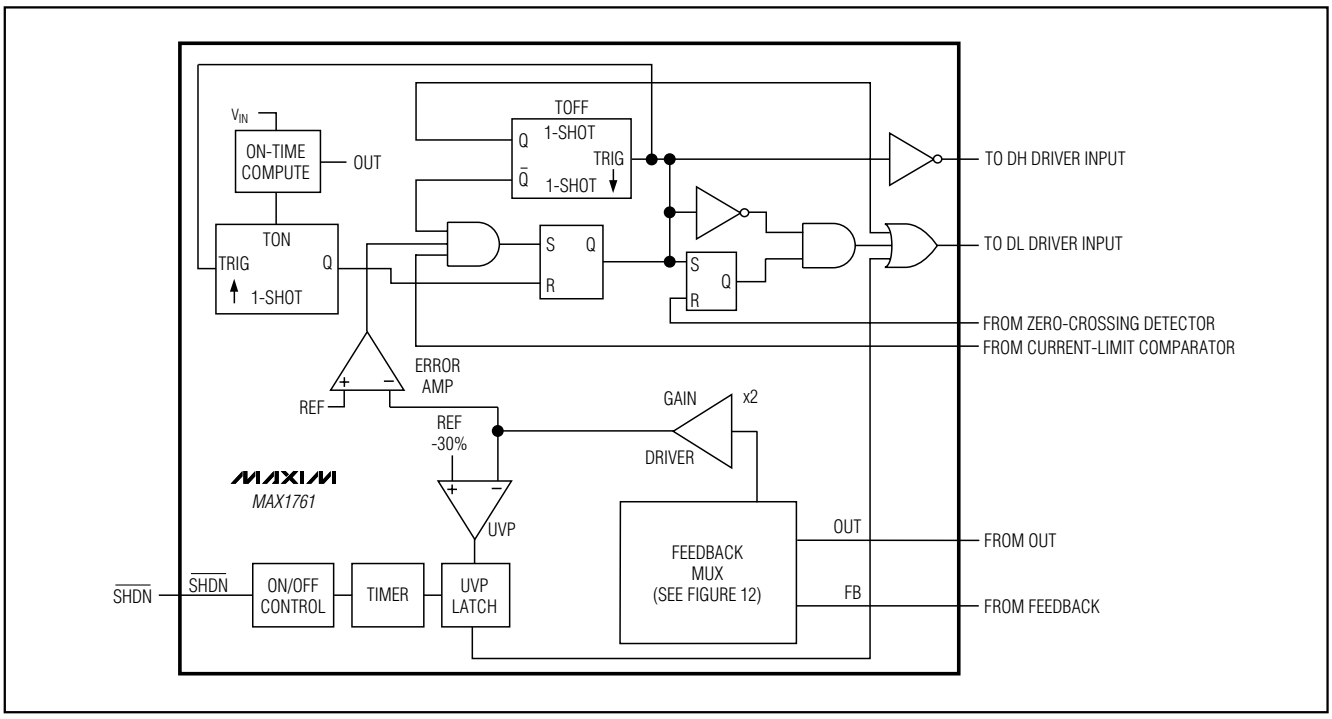

Figure 3. PWM Controller (One Side Only)

The maximum on-time and minimum off-time, $t_{OFF(MIN)}$, one-shots restrict the continuous-conduction output voltage. The worst-case dropout performance occurs with the minimum on-time and the maximum off-time, so the worst-case duty cycle for V_{IN} = 6V, V_{OUT1} = 5V is given by:

$$\text{Duty Cycle} = \frac{t_{ON(MIN)}}{t_{ON(MIN)} + t_{OFF(MAX)}} = \frac{2.054\mu s}{2.054\mu s + 500ns} = 80.4\%$$

The duty cycle is ideally determined by the ratio of input-to-output voltage (Duty Cycle = V_{OUT}/V_{IN}). Voltage losses in the loop cause the actual duty cycle to deviate from this relationship. See the *Dropout Performance* section for more information. Equate the off-time duty cycle restriction to the nonideal input/output voltage duty cycle ratio. Typical units will exhibit better performance. Operation of any power supply in dropout will greatly reduce the circuit's transient response, and some additional bulk capacitance may be required to support fast load changes.

Resistive voltage drops in the inductor loop and the dead-time effect cause switching-frequency variations. Parasitic voltage losses decrease the effective voltage applied to the inductor. The MAX1761 compensates by shifting the duty cycle to maintain the regulated output voltage. The resulting change in frequency is:

$$f = \frac{V_{OUT} + V_{DROP1}}{t_{ON}(V_{IN} + V_{DROP2})}$$

V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path; and t_{ON} is the on-time calculated by the MAX1761.

In forced PWM mode, the dead-time effect increases the effective on-time, reducing the switching frequency as one or both dead times. This occurs only at light or negative loads when the inductor current reverses. Under these conditions, the inductor's EMF causes the switching node of the inductor to go high during the dead time, extending the effective on-time.

Automatic Pulse-Skipping Switchover

In normal operation, the MAX1761's PWM control algorithm automatically skips pulses at light loads. Comparators at each CS_ input in the MAX1761 truncate the low-side switch's on-time at the point where the inductor current drops to zero. This occurs when the inductor current is operating at the boundary between continuous and discontinuous conduction mode (Figure 4). This threshold is equal to 1/2 the peak-to-peak ripple current, which is inversely proportional to the inductor value:

$$I_{LOAD(SKIP)} \approx \frac{K \times V_{OUT}}{2L}\left(\frac{V+ - V_{OUT}}{V+}\right)$$

where K is the on-time scale factor listed in Table 3. For example, in the typical application circuit (Figure 1), with V_{OUT1} = 2.5V, V+ = 15V, L = 9µH, and K = 2.857µs (Table 3), switchover to pulse-skipping operation occurs at I_{LOAD} = 0.33A or about 1/8 full load. The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used.

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation; this is a normal operating condition that improves light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, lower inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

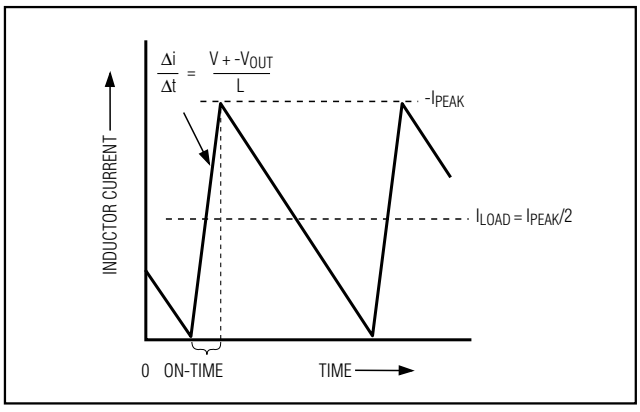

Figure 4. Pulse-Skipping/Discontinuous Crossover Point

Forced PWM Operation (ON2 floating)

The low-noise, forced-PWM mode (ON2 floating) disables the zero-crossing current comparator that controls the low-side switch on-time. The resulting low-side gate-drive waveform is forced to become the complement of the high-side gate-drive waveform. This, in turn, causes the inductor current to reverse at light loads as the PWM loop strives to maintain a constant duty ratio of V_{OUT}/V+. The benefit of forced-PWM mode is that it keeps the switching frequency nearly constant, but it results in a higher no-load battery current that can be 10mA to 40mA, depending on the gate capacitance of the external MOSFETs.

Forced-PWM mode is most useful for reducing audio-frequency noise, improving load-transient response, and providing sink-current capability for dynamic output voltage adjustment. Multiple-output applications that use a flyback transformer or coupled inductor also benefit from forced-PWM operation because the continuous switching action improves cross-regulation.

Low-Side Current-Limit Sensing

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses the on-state resistance of the low-side MOSFET as a current-sensing element. If the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle (Figure 5). The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the MOSFET on-resistance, inductor value, and input voltage. The reward for this uncertainty is robust, lossless overcurrent sensing. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current (forced PWM mode only). The negative current-limit threshold is set to approximately 120% of the positive current limit.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by CS_. Mount or place the IC close to the low-side MOSFET with short, direct traces, making a Kelvin-sense connection to the source and drain terminals.

If greater current-limit accuracy is desired, CS can be connected to an external sense resistor inserted between the source of the low-side switch and ground (Figure 6). The resulting current limit will be ILIM = 0.1V / R_{SENSE}, and it will have ±8% error.

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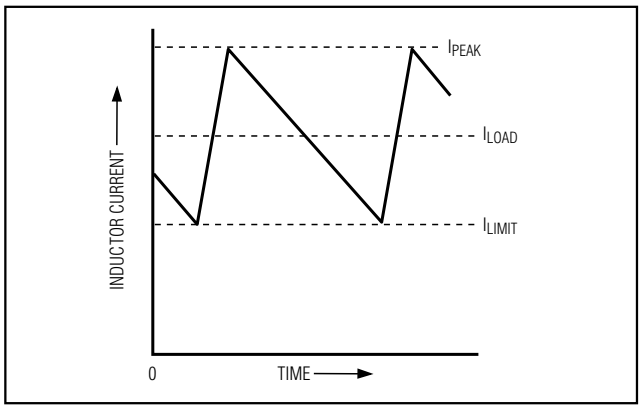

Figure 5. "Valley" Current-Limit Threshold Point

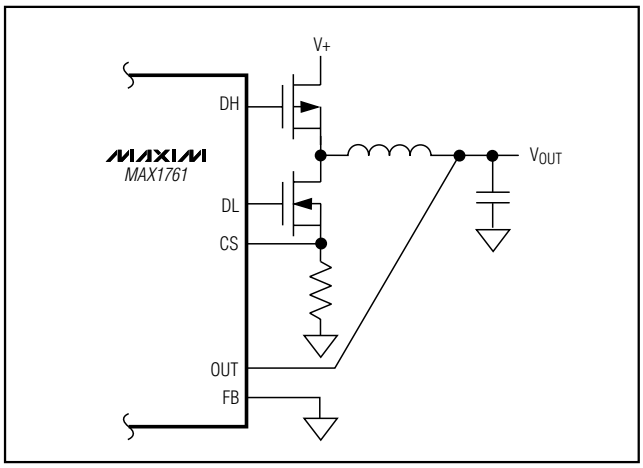

Figure 6. Using a Low-Side Current-Sense Resistor

MOSFET Gate Drivers

The DH and DL outputs are optimized for driving moderate-sized power MOSFETs. The MOSFET drive capability is stronger for the low-side switch. This is consistent with the low duty factor seen in the notebook computer environment where a large V+ to V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully off. There must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX1761 will interpret the MOSFET gate as "off" while there is still charge left on the gate. Use very short, wide traces measuring 10 to 20 squares or less (50mils to 100mils wide if the MOSFET is 1 inch from the device). Similar to the DL output, an adaptive dead-time circuit also monitors the DH output and prevents the low-side FET from turning on until DH is fully off. The same considerations should be used for routing the DH signal to the high-side FET.

Since the transition time for a P-channel switch can be much longer than an N-channel switch, the dead time prior to the high-side PMOS turning on will be more pronounced than in other synchronous step-down regulators, which use high-side N-channel switches. On the high-to-low transition, the voltage on the inductor's "switched" terminal flies below ground until the low-side switch turns on. A similar dead-time spike occurs on the opposite low-to-high transition. Depending upon the magnitude of the load current, these spikes usually have a minor impact on efficiency.

The high-side drivers (DH_) swing from V+ to GND and will typically source/sink 0.6A from the gate of the P-channel MOSFET. The low-side driver (DL_) swings from VL to ground and will typically source 0.5A and sink 0.9A from the gate of the N-channel FET.

The internal pulldown transistors that drive DL low are robust, with a 2.0Ω (typ) on-resistance. This helps prevent DL from being pulled up when the high-side switch turns on, due to capacitive coupling from the drain to the gate of the low-side MOSFET. This places some restrictions on the FETs that can be used. Using a low-side FET with smaller gate-to-drain capacitance can prevent these problems.

Shutdown and Mode Control Inputs

The MAX1761 has two inputs (ON1, ON2) that control the operating modes of the two regulators. Asserting ON1 low places both regulators in micropower shutdown mode, in which both VL and REF are disabled. When ON1 is high, OUT1 is enabled, with VL and REF active. ON2 serves a dual function: it is a shutdown control for OUT2, and it determines the switching mode for both regulators. When ON2 is low (ON2 < 0.5V), OUT2 is disabled and OUT1 operates in normal mode. Floating ON2 places both outputs in forced PWM mode. When ON2 is high (2V < ON2 < V_L), both regulators run in normal operating mode. Toggling ON1 from low to high resets the fault latch (Table 4).

Output Undervoltage Protection

The output undervoltage protection function is similar to foldback current limiting but employs a timer rather than a variable current limit. If the MAX1761 output voltage is under 70% (typ) of the nominal output voltage 20ms after coming out of shutdown, then both PWMs are latched off and will not restart until V+ is cycled or ON1 is toggled low to high.

Table 4. Operating Mode Control Summary

MODE	ON1	ON2	DESCRIPTION
Shutdown	ON1 < 0.5V	X	Both OUT1 and OUT2 off, VL and REF disabled
ON1 Enabled	2.0V < ON1 < V+	ON2 < 0.5V	OUT1 on in normal mode, OUT2 off
Forced PWM	2.0V < ON1 < V+	Floating	Both OUT1 and OUT2 on in forced PWM mode
Normal Operation	2.0V < ON1 < V+	2.0V < ON2 ≤ VL	Both OUT1 and OUT2 on in normal mode

Thermal Fault Protection

The MAX1761 features a thermal fault protection circuit. When the temperature rises above +160°C, the DL low-side gate-driver outputs latch high until ON1 is toggled or V+ is cycled. The fault threshold has 10°C of thermal hysteresis, which prevents the regulator from restarting until the die cools off.

POR and Soft-Start

Power-on reset (POR) occurs when V+ falls below approximately 2V, resetting the fault latch and preparing the PWM for operation once the power is cycled. VL undervoltage lockout (UVLO) circuitry inhibits switching and forces the DL gate driver low until VL rises above 4.25V, whereupon an internal digital soft-start timer begins to ramp up the maximum allowed current limit. The ramp occurs in five steps: 20%, 40%, 60%, 80%, and 100%; 100% current is available after 1.7ms.

Design Procedure

Firmly establish the input voltage range and the maximum load current before choosing the inductor operating point (ripple current ratio). The following three factors determine the SMPS design using the MAX1761:

1) **Input Voltage Range.** The maximum value (V+(max)) must accommodate the worst-case high AC adapter voltage. The minimum value (V+(min)) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
2) **Maximum Load Current.** There are two values to consider, the *peak load current* ($I_{LOAD(MAX)}$) and the *continuous load current* (I_{LOAD}). The peak load current determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.
3) **Inductor Operating Point.** This choice provides trade-offs between size and efficiency. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output noise. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit.

The MAX1761's pulse-skipping algorithm initiates skip mode at the critical conduction point. So, the inductor operating point also determines the load-current value at which PWM/skip mode switchover occurs. The optimum point is usually found between 20% and 50% ripple current.

The inductor ripple current also impacts transient-response performance, especially at low $V_{IN} - V_{OUT}$ differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{(\Delta I_{LOAD(MAX)})^2 \times L}{2C_F \times DUTY(V+_{(MIN)} - V_{OUT})}$$

Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as follows:

$$L = \frac{V_{OUT}(V+ - V_{OUT})}{V+ \times f \times LIR \times I_{LOAD(MAX)}}$$

Example: $I_{LOAD(MAX)}$ = 2.5A, V+(max) = 20V, V_{OUT1} = 2.5V, f = 350kHz, 35% ripple current or LIR = 0.35:

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$$L = \frac{2.5V(20V - 2.5V)}{20V \times 350kHz \times 0.35 \times 2.5A} = 7.1\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and works well at 250kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} - 1/2\ LIR \times I_{LOAD(MAX)} = (1 - 0.5\ LIR)\ I_{LOAD(MAX)}$$

Setting Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current plus some safety margin. For the circuit in Figure 1, with a desired 2.5A maximum load current, the worst-case current limit is set at 3.0A, providing a 20% safety margin. Under these conditions, the valley of the inductor current waveform occurs at:

$$I_{VALLEY} = I_{LOAD(MAX)} - 1/2\ LIR \times I_{LOAD(MAX)} = (1 - 0.5\ LIR)\ I_{LOAD(MAX)}$$

The required valley current is I_{VALLEY} = 3A - 1/2 (0.35) × 2.5A = 2.56A. Next, the current-sense feedback voltage must be scaled taking into account the tolerance of the CS_ current-limit threshold and the maximum MOSFET drain-source on-resistance ($R_{DS(ON)}$) variation over temperature. The minimum current-limit threshold at the CS_ pins is 92mV. The worst-case maximum value for ($R_{DS(ON)}$) over temperature is 50mΩ. At 2.56A, the voltage developed across the low-side switch is 128mV. A resistive voltage-divider with a 0.703 attenuation ratio is necessary to scale this voltage to the 92mV CS_ threshold.

A current-sense resistor can be used if a more accurate current limit is needed than is available when using the MOSFET ($R_{DS(ON)}$ (Figure 6). Placing the sense resistor between the source of the low-side MOSFET and ground provides a very accurate sense point for the CS_ inputs. Alternatively, a small sense resistor can be used in series with the low-side MOSFET to ballast the device and reduce the temperature coefficient of the current limit when sensing at the inductor's switched node. This provides a compromise between sensing across the MOSFET device alone or using a large sense resistor.

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy the stability criterion.

In CPU V_{CORE} converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{DIP}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple:

$$R_{ESR} \le \frac{Vp - p}{LIR \times I_{LOAD(MAX)}}$$

The actual required µF capacitance value relates to the physical size needed to achieve low ESR as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, SP, POS, and other electrolytics).

When using low-capacitance filter capacitors, such as ceramic or polymer types, capacitor size is usually determined by the capacitance needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the V_{SOAR} requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} equation in *Design Procedure*). The amount of overshoot due to stored inductor energy can be calculated as:

$$\Delta V \approx \frac{(L \times I_{PEAK}{}^2)}{2CV_{OUT}}$$

where I_{PEAK} is the peak inductor current.

Stability Considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation:

$$f_{ESR} = \frac{f}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_F}$$

For a typical 350kHz application, the ESR zero frequency must be well below 100kHz, preferably below 50kHz. Tantalum and OS-CON capacitors have typical ESR zero frequencies of 15kHz. Sanyo POS capacitors have typical ESR zero frequencies of 20kHz. In the design example used for inductor selection, the ESR needed to support 50mVp-p ripple is 50mV / LIR(2.5A) = 57.1mΩ. A single150µF/6.3V Sanyo POS capacitor provides 55mΩ (max) ESR. This ESR results in a zero at 19.3kHz, well within the bounds of stability.

Don't put high-value ceramic capacitors directly across the fast feedback inputs (FB_/OUT_ to GND) without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and may cause erratic, unstable operation. However, it's easy to add enough series resistance by placing the capacitors a couple of inches downstream from the junction of the inductor and FB_/OUT_ pin.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability.

Double-pulsing occurs due to noise on the output or because the ESR is so low that there isn't enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 500ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient ESR. Loop instability can result in oscillations at the output after line or load perturbations that can cause the output voltage to go outside the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient (refer to the MAX1761 EV kit manual) and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Don't allow more than one cycle of ringing after the initial step-response under- or overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resilience to power-up surge currents.

$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V+ - V_{OUT})}}{V+}\right)$$

Power MOSFET Selection

DC bias and output power considerations dominate the selection of the power MOSFETs used with the MAX1761. Care should be taken not to exceed the device's maximum voltage ratings. In general, both switches are exposed to the supply voltage, so select MOSFETs with $V_{DS(MAX)}$ greater than V+(max). Gate drive to the N-channel and P-channel MOSFETs is not symmetrical. The N-channel device is driven from ground to the logic supply VL. The P-channel device is driven from V+ to ground. The maximum rating for V_{GS} for the N-channel device is usually not an issue. However, $V_{GS(MAX)}$ for the P-channel must be at least V+(max). Since $V_{GS(MAX)}$ is usually lower than $V_{DS(MAX)}$, gate-drive constraints often dictate the required P-channel breakdown rating.

For moderate input-to-output differentials, the high-side MOSFET (Q1) can be sized smaller than the low-side MOSFET (Q2) without compromising efficiency. The high-side switch operates at a very low duty cycle under these conditions, so most conduction losses occur in Q2. For maximum efficiency, choose a high-side MOSFET (Q1) that has conduction losses **(I^2RD)** equal to the switching losses **($fCV+^2$)**. Make sure that the conduction losses at the **minimum** input voltage don't exceed the package thermal limits or violate the overall thermal budget. Similarly check for rating violations for conduction and switching losses at the maximum input voltage (see *MOSFET Power Dissipation*).

The MAX1761 has an adaptive dead-time circuitry that prevents the high-side and low-side MOSFETs from conducting at the same time (see *MOSFET Gate Drivers*). Even with this protection, it is still possible for delays internal to the MOSFET to prevent one MOSFET from turning off when the other is turned on. The maximum mismatch time that can be tolerated is 60ns. Select devices that have low turn-off times, and make sure that NFET($t_{DOFF(MAX)}$) - PFET($t_{DON(MIN)}$) < 60ns, and PFET($t_{DOFF(MAX)}$) - NFET($t_{DON(MIN)}$) < 60ns. Failure to do so may result in efficiency-killing shoot-through currents.

MOSFET selection also affects PC board layout. There are four possible combinations of MOSFETs that can be used with this switcher. The designs include:

- Two dual complementary MOSFETs (Figure 7)

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- A dual N-channel and a dual P-channel MOSFET (Figure 8)
- Two single N-channels and a dual P-channel (Figure 9)
- Two single N-channels and two single P-channels (Figure 10)

There are trade-offs to each approach. Complementary devices have appropriately scaled N- and P-channel $R_{DS(ON)}$ and matched turn-on/turn-off characteristics. However, there are relatively few manufacturers of these specialized devices. Selection may be limited. Dual N- and P-channel MOSFETs are more widely available. As such, more efficient designs that benefit from the large low-side MOSFETs can be realized. This approach is most useful when the output power requirements for both regulators are about the same. This limitation can be sidestepped by using a dual P-channel and two single N-channels. Using four single MOSFETs gives the greatest design flexibility but will require the most board area.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET, the worst-case power dissipation (P_D) due to resistance occurs at the minimum battery voltage:

$$P_D(\text{Q1 resistance}) = \left(\frac{V_{OUT}}{V+_{(MIN)}}\right) \times I_{LOAD}{}^2 \times R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching (AC) losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses don't usually become an issue until the input is greater than approximately 15V.

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the CV^2F switching-loss equation. If the high-side MOSFET you've chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V+_{(MAX)}$, reconsider your MOSFET choice.

Calculating the power dissipation in Q1 due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including a verification using a thermocouple mounted on Q1:

$$P_D(\text{Q1 switching}) = \frac{C_{RSS} \times V+_{(MAX)}{}^2 \times f \times I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of Q1, and I_{GATE} is the peak gate-drive source/sink current (1A typ).

For the low-side MOSFET (Q2) the worst-case power dissipation always occurs at maximum battery voltage:

$$P_D(Q2) = \left(1 - \frac{V_{OUT}}{V+_{(MAX)}}\right) \times I_{LOAD}{}^2 \times Rs$$

The absolute worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD\ (MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, the circuit must be overdesigned to tolerate:

$$I_{LOAD} = I_{LIMIT\ (MAX)} + 1/2 \times LIR \times I_{LOAD\ (MAX)}$$

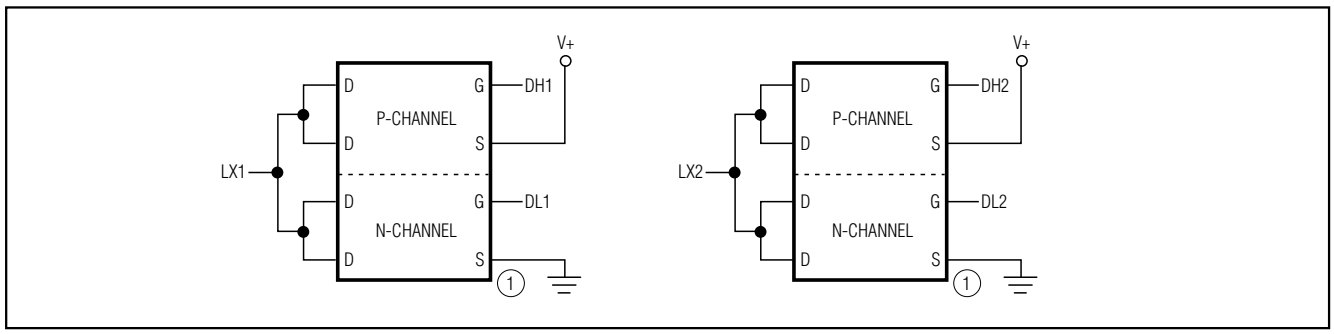

Figure 7. Dual Complementary MOSFET Design

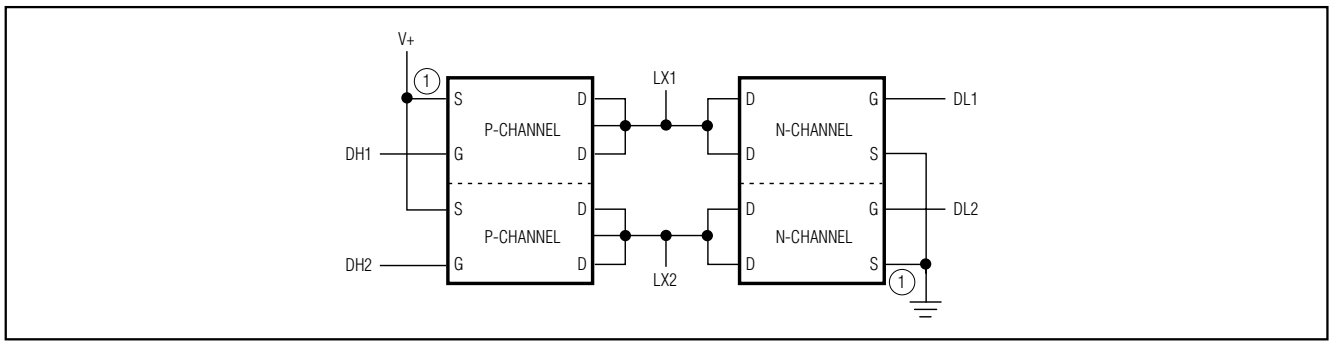

Figure 8. Dual N- and P-Channel MOSFET Design

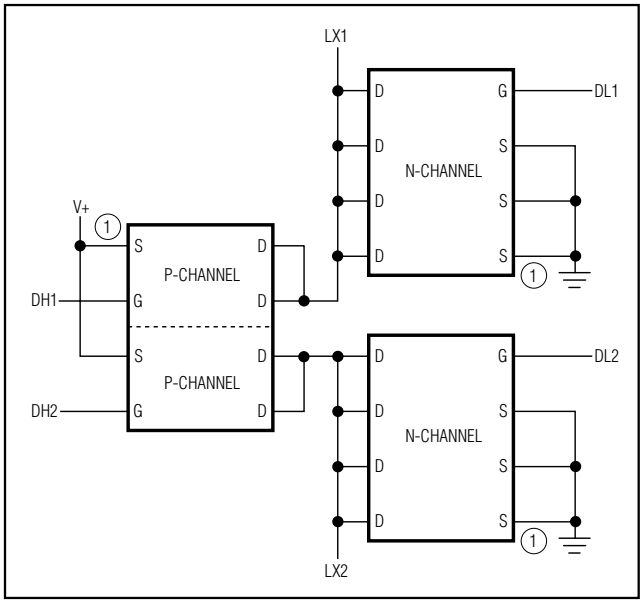

Figure 9. Two Single N-Channel MOSFETs and a Dual P-Channel MOSFET Design

where $I_{LIMIT(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. This means that the MOSFETs must be very well heatsinked. If short-circuit protection without overload protection is enough, a normal I_{LOAD} value can be used for calculating component stresses.

Choose a Schottky diode (D1, Figure 2) having a forward voltage low enough to prevent the Q2 MOSFET body diode from turning on during the dead time. As a general rule, a diode having a DC current rating equal to 1/3 of the load current is sufficient. This diode is optional and can be removed if efficiency isn't critical.

Applications Issues

Dropout Performance

The output voltage adjust range for continuous-conduction operation is restricted by the nonadjustable 500ns (max) minimum off-time one-shot. For best dropout performance, use the side with the lower switching frequency, FB2 (250kHz). When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing

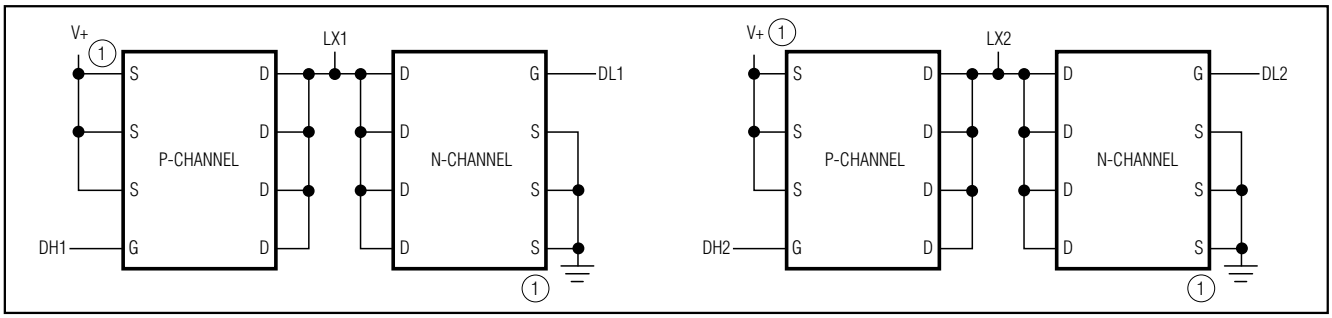

Figure 10. Two Single N-Channel MOSFETs and Two Single P-Channel MOSFETs Design

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tolerances and internal propagation delays introduce an error to the t_{ON} K-factor. Also, keep in mind that transient response performance of buck regulators operated close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in *Design Procedure*).

Dropout design example: V_{IN} = 6.5V (min), V_{OUT} = 5V, f = 350kHz, 250kHz. The required duty is (V_{OUT} + V_{SW}) / (V+ - V_{SW}) = (5V + 0.1V) / (6.5V - 0.1V) = 79.7%. The worst-case on-time for f = 350kHz is (V_{OUT} + 0.1V) / V+ × K = 5.1V / 6.5V × 2.857µs-V × 90% = 2.017µs. The IC duty-factor limitation is:

$$Duty = \frac{t_{ON(MAX)}}{t_{ON(MAX)} + t_{OFF(MIN)}} = \frac{2.017\mu s}{2.017\mu s + 500ns} = 80.1\%$$

Thus, operation at 350kHz meets the required duty cycle. A similar analysis with f = 250kHz (K = 4µs-V) shows that at f = 250kHz, the maximum duty cycle is 85.0%, also meeting the required duty cycle.,

Remember to include inductor resistance and MOSFET on-state voltage drops (V_{SW}) when doing worst-case dropout duty-factor calculations.

Fixed Output Voltages

The MAX1761's dual-mode operation allows the selection of common voltages without requiring external components (Figure 11). Connect FB1 to GND for a fixed +2.5V output at OUT1; otherwise, connect FB1 to a resistive voltage-divider for an adjustable output. Connect FB2 to GND for a +1.8V output; otherwise, connect FB2 to a resistive voltage-divider for an adjustable output.

Adjusting VOUT

The output voltage can be adjusted with a resistive voltage-divider if desired (Figure 12). The equation for adjusting the output voltage is:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right)$$

where V_{FB} is 1.0V, and R2 is about 10kΩ.

Low Input Voltage Operation (V+ = +5V)

The MAX1761 can be used in applications using a 5V ±10% input supply by overdriving VL with the input supply voltage, V+. This not only enables operation of the MAX1761 down to V+ = 4.5V but has the added benefit of increasing overall efficiency. Overdriving the VL regulator will increase the drive on the low-side MOSFETs, thereby lowering their $R_{DS(ON)}$ and reducing power consumption. Note that VL should not be higher than 5.5V if connected to VL. Also note, V+ should not be brought below 5V unless VL is connected directly to V+.

PC Board Layout Guidelines

Careful PC board layout is critical to achieving low switching losses and clean, stable operation. This is especially true for dual converters, where one channel can affect the other. The switching power stages require particular attention (Figure 13). Refer to the MAX1761 EV kit data sheet for a specific layout example. If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Isolate the top-side power components from the sensitive analog components on the bottom side with a ground shield. Use a separate PGND plane under the OUT1 and OUT2 sides (called PGND1 and PGND2). Avoid the introduction of AC currents into the PGND1 and PGND2 ground planes. Run the power plane ground currents on the top side only, if possible.
- Use a star ground connection on the power plane to minimize the crosstalk between OUT1 and OUT2.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Connect AGND and PGND together close to the IC. Do not connect them together anywhere else. Carefully follow the grounding instructions under Step 4 of the *Layout Procedure*.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
- CS_ and PGND connections to the synchronous rectifiers for current limiting must be made using Kelvin sensed connections to guarantee the current-limit accuracy. With SO-8 MOSFETs, this is best done by routing power to the MOSFETs from outside, using the top copper layer, while connecting PGND and CS_ *inside* (underneath) the SO-8 package.

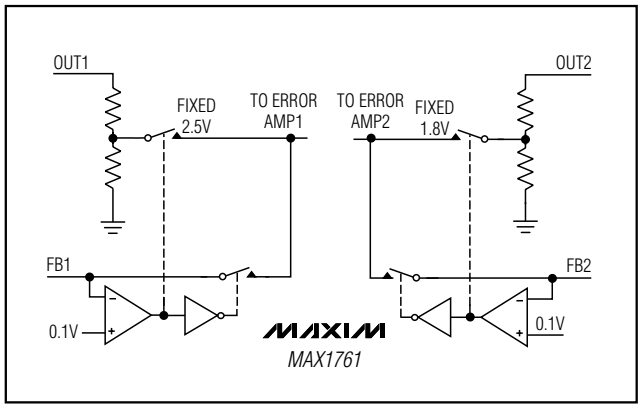

Figure 11. Feedback MUX

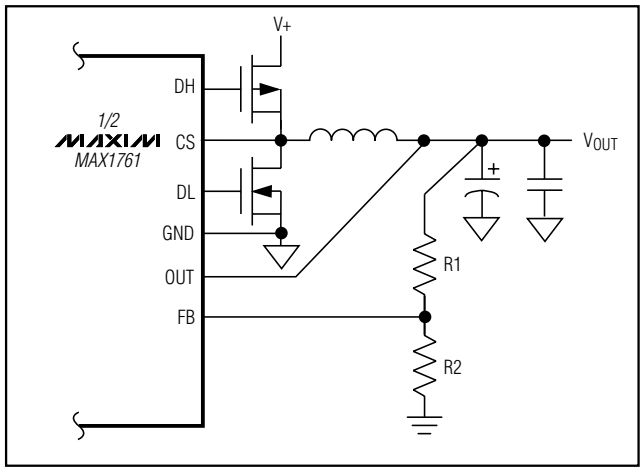

Figure 12. Setting V_{OUT} with a Resistive Voltage-Divider

- When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharge path. For example, it's better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Ensure that the OUT connection to C_{OUT} is short and direct. However, in some cases it may be desirable to deliberately introduce some trace length between the OUT inductor node and the output filter capacitor (see *Stability Considerations*).
- Route high-speed switching nodes (CS_, DH_, and DL_) away from sensitive analog areas (REF, FB_). Use a PGND as an EMI shield to keep radiated switching noise away from the IC, feedback dividers, and analog bypass capacitors.
- Avoid coupling switching noise into control input connections (ON1, ON2, etc.). These pins should be referenced to a quiet analog ground plane.

Layout Procedure

1) Place the power components first, with ground terminals adjacent (Q2 source, $CI_{N\_}$, $C_{OUT\_}$). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the synchronous rectifier MOSFETs, preferably on the back side in order to keep CS_, PGND_, and the DL_ gate-drive line short and wide. The DL_ gate trace must be short and wide, measuring 10 to 20 squares (50mils to 100mils wide if the MOSFET is 1 inch from the controller IC).
3) Place the VL capacitor near the IC controller.
4) Make the DC-DC controller ground connections as follows: near the IC, create a small analog ground plane. Use this plane for the ground connection for the REF and VL bypass capacitor, and FB_ dividers. Create another small ground island for PGND, and use it for the V+ bypass capacitor, placed very close to the IC. Connect the AGND and the PGND together under the IC (this is the only connection between AGND and PGND).
5) On the board's top side (power planes), make a star ground to minimize crosstalk between the two sides. The top-side star ground is a star connection of the input capacitors, side 1 low-side MOSFET, and side 2 low-side MOSFET. Keep the resistance low between the star ground and the sources of the low-side MOSFETs for accurate current limit. Connect the top-side star ground (used for MOSFET, input, and output capacitors) to the small PGND island with a short, wide connection (preferably just a via). If multiple layers are available (highly recommended), create PGND1 and PGND2 islands on the layer just below the top-side layer (refer to the MAX1761 EV kit for an example) to act as an EMI shield. Connect each of these individually to the star ground via, which connects the top side to the PGND plane. Add one more solid ground plane under the IC to act as an additional shield, and also connect that to the star ground via.
6) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias.

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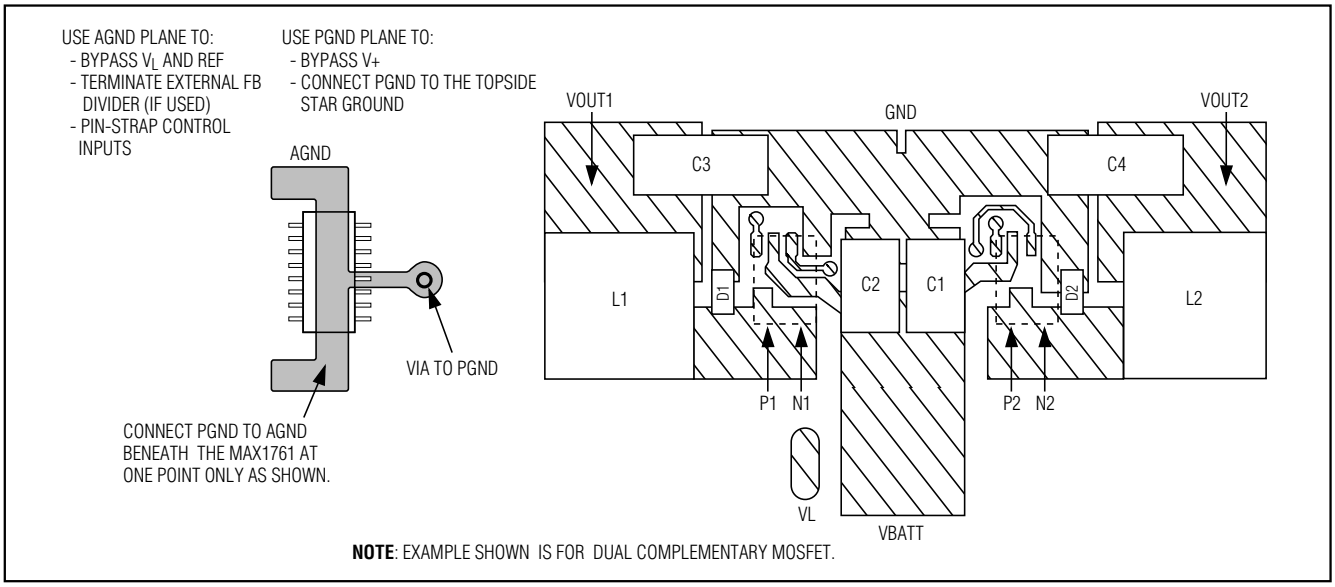


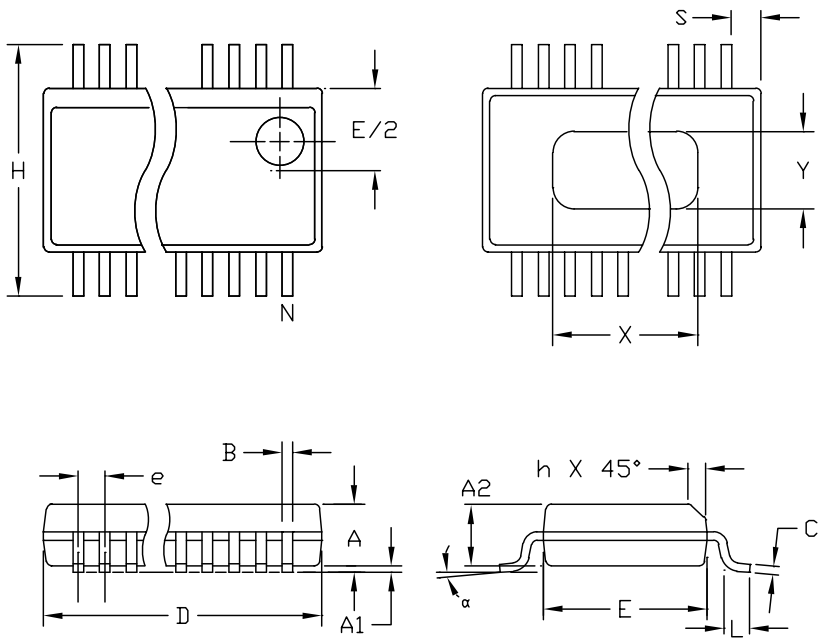
Figure 13. PC Board Layout Example

Chip Information

TRANSISTOR COUNT: 6045

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	B	1/1

Note: *The MAX1761 does not have a heat slug.*