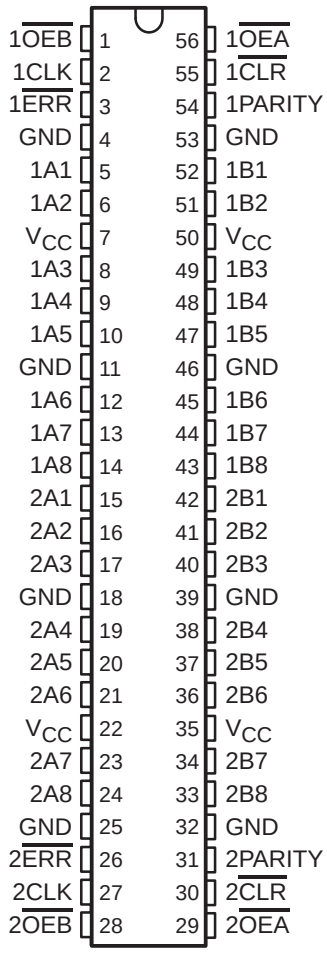
SCAS166A – JUNE 1990 – REVISED APRIL 1996

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **Parity Error Flag With Parity Generator/Checker**
- **Register for Storage of the Parity Error Flag**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

54ACT16833 . . . WD PACKAGE
74ACT16833 . . . DL PACKAGE
(TOP VIEW)



description

The ’ACT16833 consist of two noninverting 8-bit to 9-bit parity bus transceivers and are designed for communication between data buses. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY or 2PARITY is configured as an input and combined with the B-input data to generate an active-low error flag if odd parity is not detected.

The error (1$\overline{\text{ERR}}$ or 2$\overline{\text{ERR}}$) output is configured as an open-collector output. The B-to-A parity error flag is clocked into 1$\overline{\text{ERR}}$ or 2$\overline{\text{ERR}}$ on the low-to-high transition of the clock (1CLK or 2CLK) input. 1$\overline{\text{ERR}}$ or 2$\overline{\text{ERR}}$ is cleared (set high) by taking the clear (1$\overline{\text{CLR}}$ or 2$\overline{\text{CLR}}$) input low.

The output-enable ($\overline{\text{OEA}}$ and $\overline{\text{OEB}}$) inputs can be used to disable the device so that the buses are effectively isolated. When both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The 74ACT16833 is packaged in TI’s shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

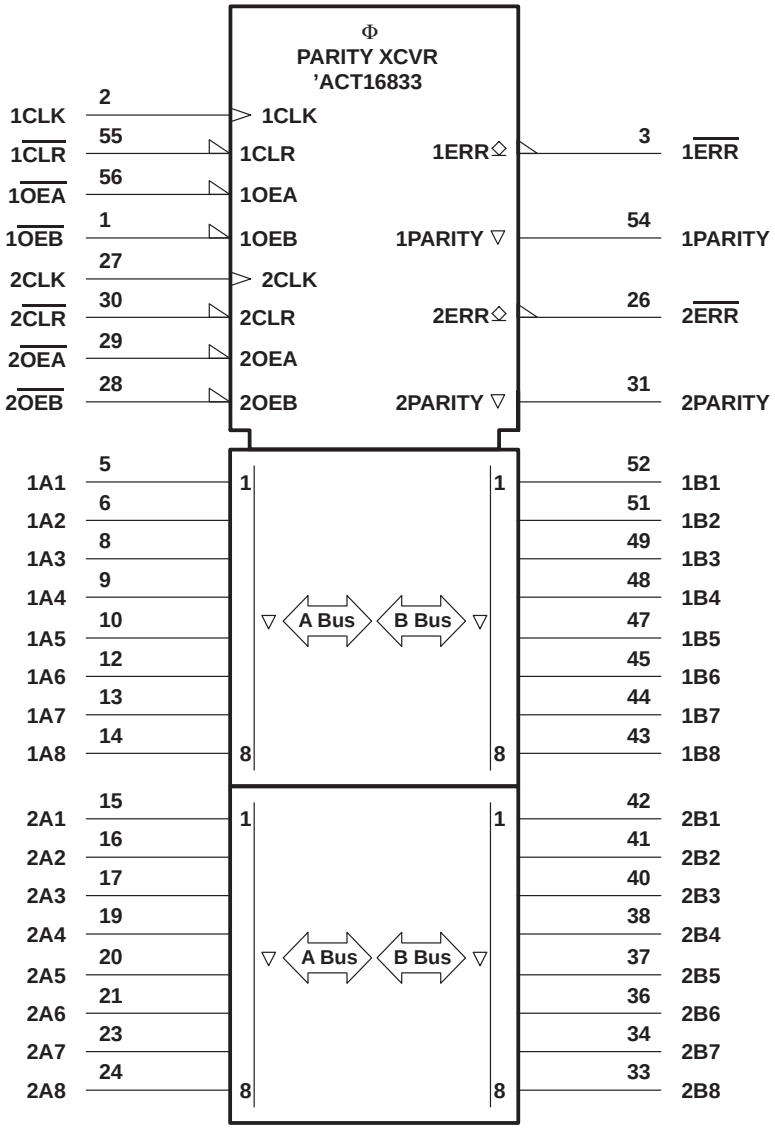
The 54ACT16833 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16833 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai Σ OF H	Bi† Σ OF H	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error-flag register
H	H	H	No↑	X	X	Z	Z	Z	NC	Isolation§
		L	No↑	X					H	
		H	↑	Odd					H	
		H	↑	Even					L	
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

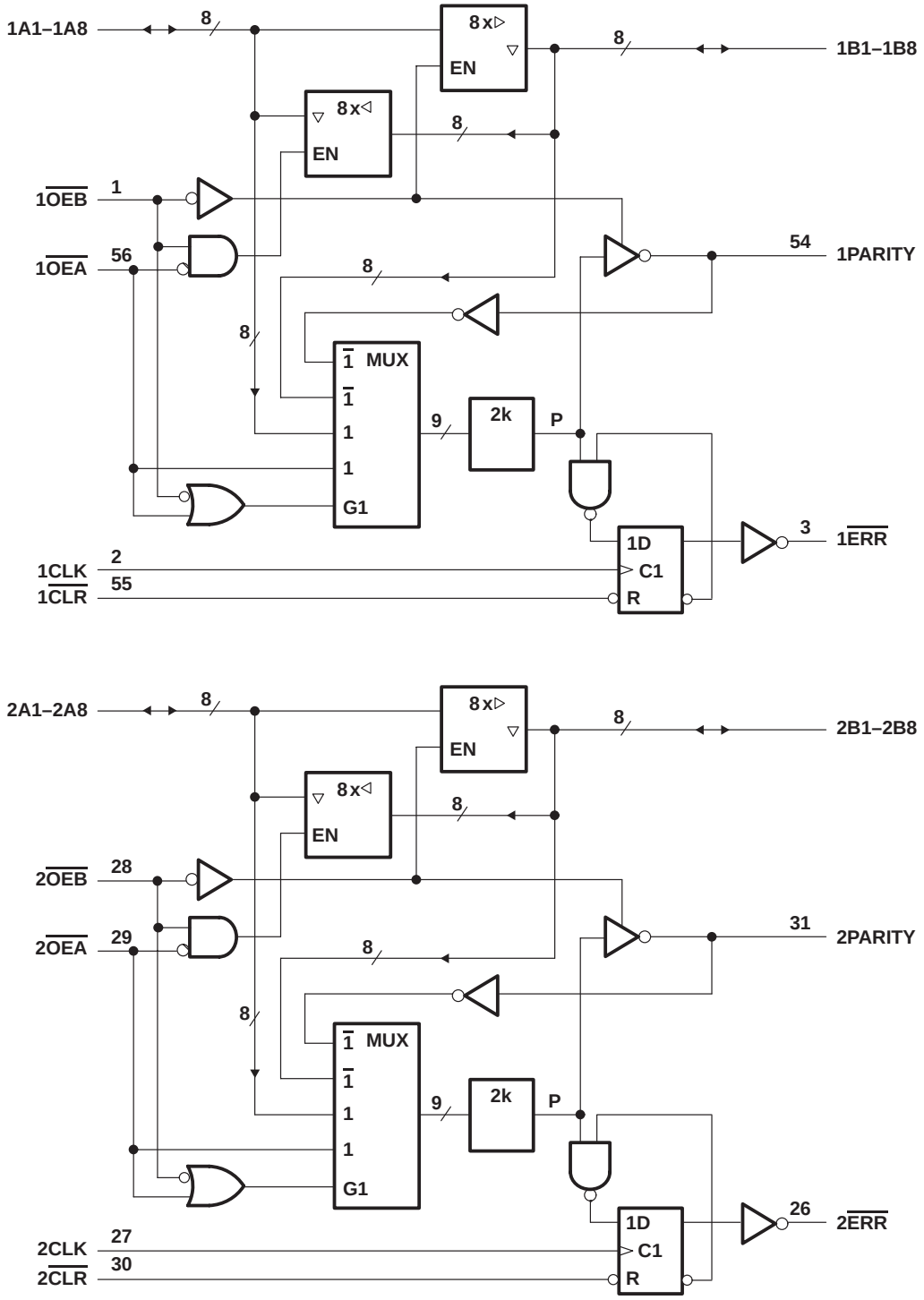
NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume $\overline{ERR}$ was previously high.
§ In this mode, $\overline{ERR}$ (when clocked) shows inverted parity of the A bus.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

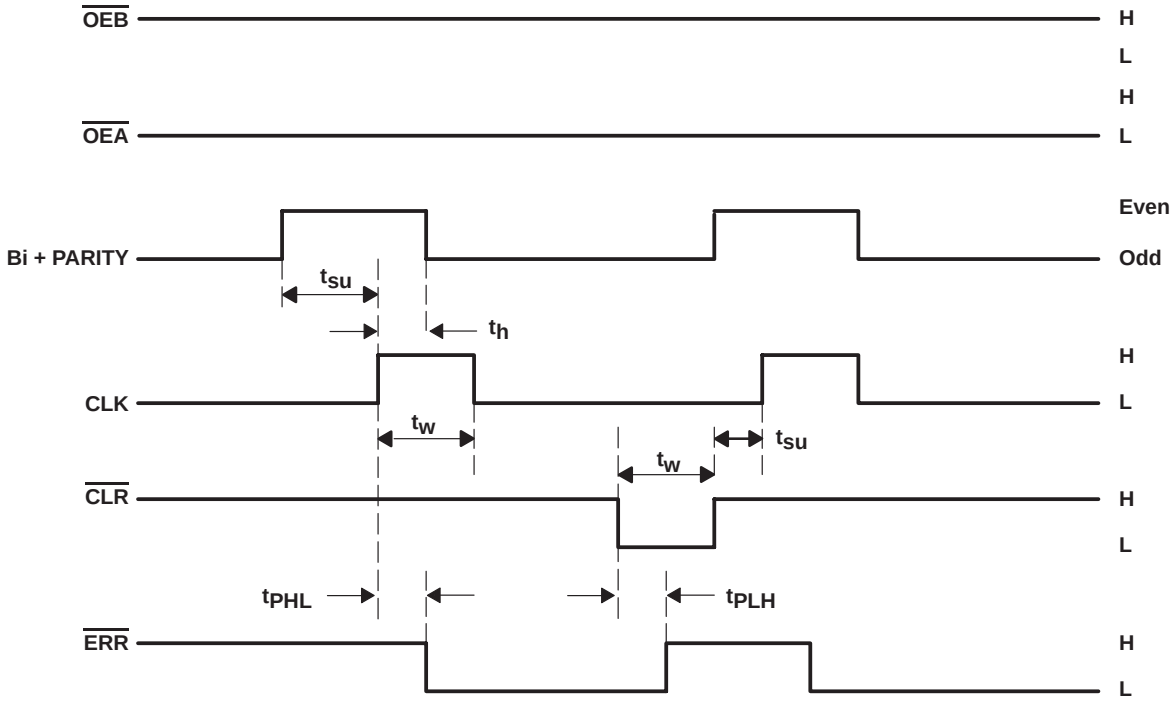


ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT $\overline{ERR}$	FUNCTION
$\overline{CLR}$	CLK	POINT P‡	$\overline{ERR}_{n-1}$†		
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

† The state of $\overline{ERR}$ before any changes at $\overline{CLR}$, CLK, or point P
‡ Location of point P is shown on local diagram.

timing waveforms, error flag



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±450 mA
Maximum power package dissipation at T_A = 55°C (in still air) (see Note 2): DL package . . . . . 1.4 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16833			74ACT16833			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			–24			–24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16833		74ACT16833		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	$\overline{ERR}$	$V_O = V_{CC}$	5.5 V			0.5		5		5	µA
V_{OH}	All outputs except $\overline{ERR}$	I_{OH} = –50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = –24 mA	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		I_{OH} = –75 mA†	5.5 V				3.85		3.85		
V_{OL}		I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65		1.65	
I_I	A or B ports	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}‡	Control inputs	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80		80	µA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		3.5						pF
C_{io}	A or B ports, PARITY	$V_O = V_{CC}$ or GND	5 V		11.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1 and timing waveforms)

			T_A = 25°C		54ACT16833		74ACT16833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	4		4		4		ns
		$\overline{CLR}$ low	4		4		4		
t_{su}	Setup time before CLK↑	Bi + PARITY	7.5		7.5		7.5		ns
		$\overline{CLR}$ inactive	1.5		1.5		1.5		
t_h	Hold time, Bi + PARITY low after CLK↑		0		0		0		ns

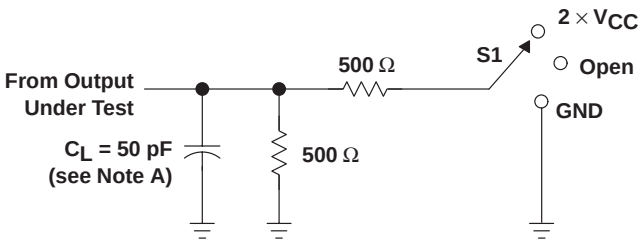
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1 and timing waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16833		74ACT16833		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	4	7.2	9.2	4	10.4	4	10.4	ns
t_{PHL}			3.2	6.6	9.6	3.2	10.7	3.2	10.7	
t_{PLH}	A	PARITY	3.9	7.9	12	3.9	13.5	3.9	13.5	ns
t_{PHL}			4.2	8.3	12.4	4.2	13.8	4.2	13.8	
t_{PZH}	$\overline{OEB}$ or $\overline{OEA}$	A or B	3.1	6.7	10.1	3.1	11.2	3.1	11.2	ns
t_{PZL}			3.8	7.9	11.6	3.8	13	3.8	13	
t_{PHZ}	$\overline{OEB}$ or $\overline{OEA}$	A or B	5.5	7.8	10	5.5	10.8	5.5	10.8	ns
t_{PLZ}			5	7.1	9.3	5	10.1	5	10.1	
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	10.7	13.1	15.4	10.7	15.8	10.7	15.8	ns
t_{PHL}	CLK		4.6	7.8	10.3	4.6	11.6	4.6	11.6	
t_{PLH}	$\overline{OEA}$	PARITY	4	8	11.8	4	13.2	4	13.2	ns
t_{PHL}			4.3	8.5	12.3	4.3	13.6	4.3	13.6	
t_{PZH}	$\overline{OEB}$	PARITY	2.6	5.7	8.5	2.6	9.5	2.6	9.5	ns
t_{PZL}			3.4	6.8	9.8	3.4	10.7	3.4	10.7	
t_{PHZ}	$\overline{OEB}$	PARITY	5.6	7.9	9.5	5.6	10.2	5.6	10.2	ns
t_{PLZ}			5.1	7.2	9.1	5.1	9.7	5.1	9.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

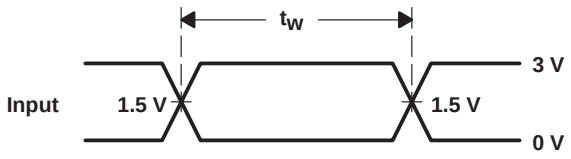
PARAMETER				TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	A to B	CL = 50 pF, f = 1 MHz	64	pF
			B to A		72	
		Outputs disabled	A to B		6	
			B to A		10.5	

PARAMETER MEASUREMENT INFORMATION

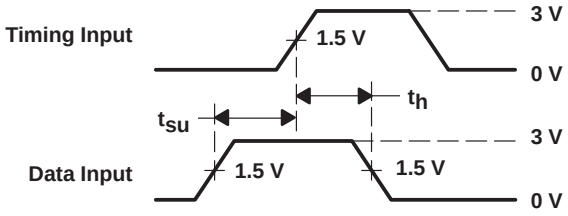


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

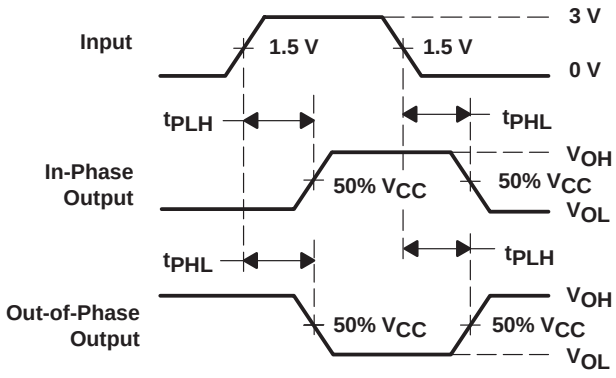
LOAD CIRCUIT



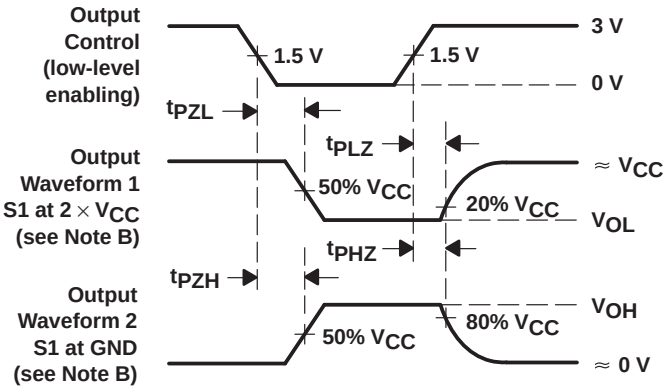
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74ACT16833DL	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
74ACT16833DLR	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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