Programmable FemtoClock® LVPECL Oscillator Replacement

ICS83PR226I-01

DATA SHEET

General Description

The ICS83PR226I-01 is a programmable LVPECL synthesizer that is "forward" footprint compatible with standard 5mm x 7mm oscillators. Forward footprint compatibility means that a board designed to accommodate the crystal oscillator interface and the optional control pins is also fully compatible with a canned oscillator footprint - the canned oscillator will drop onto the 10-VFQFN footprint for second sourcing purposes. This capability provides designers with programability and lead time advantages of silicon/crystal based solutions while maintaining compatibility with industry standard 5mm x 7mm oscillator footprints for ease of supply chain management. Oscillator-level performance is maintained with IDT's 3rd generation FemtoClock® PLL technology, which delivers sub 1ps rms phase jitter.

The ICS83PR226I-01 defaults to 125MHz using a 25MHz crystal with all 4 of the programming pins floating (pulled HIGH with internal pullup resistors) but can be also be set to 15 different frequency multiplier settings to support a wide variety of applications. The below table shows some of the more common application settings.

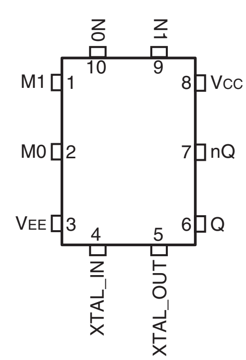
Features

- Footprint compatible with 5mm x 7mm differential oscillators
- One differential LVPECL output pair
- Crystal oscillator interface which can also be overdriven a single-ended or differential reference clock
- Output frequency range: 83.33MHz – 213.33MHz
- Crystal/Input frequency range: 15.625MHz – 32MHz
- VCO range: 500MHz – 640MHz
- PCI Express (2.5Gb/s) and Gen 2 (5 Gb/s) jitter compliant
- Cycle-to-cycle jitter: 45ps (maximum)
- RMS phase jitter @ 125MHz, 1.875MHz – 20MHz: 0.47ps (typical)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

Common Applications and Settings (not exhaustive)

M1	M0	N1	N0	XTAL (MHz)	Output Freq (MHz)	Application(s)
0	0	1	0	19.44	155.52	SONET
0	0	1	0	19.2	153.6	W-CDMA
0	0	1	1	19.2	122.8	W-CDMA
0	1	0	0	26.5625	106.25	1G, 2G Fibre Channel
0	1	0	1	26.5625	212.5	2G, 4G Fibre Channel
1	0	0	1	25	166.66	Processor, PCI-X
1	1	0	0	24	100	Processor, PCI Express 1
1	1	0	1	24	200	Processor, PCI Express 2
1	1	0	1	22.5	187.5	12G Ethernet
1	1	1	0	25	156.25	10 Gb Ethernet
1	1	1	1	25	125	1 Gb Ethernet (default)

Pin Assignment



ICS83PR226I-01

10-Lead VFQFN
5mm x 7mm x 1mm package body
K Package
Top View

Block Diagram

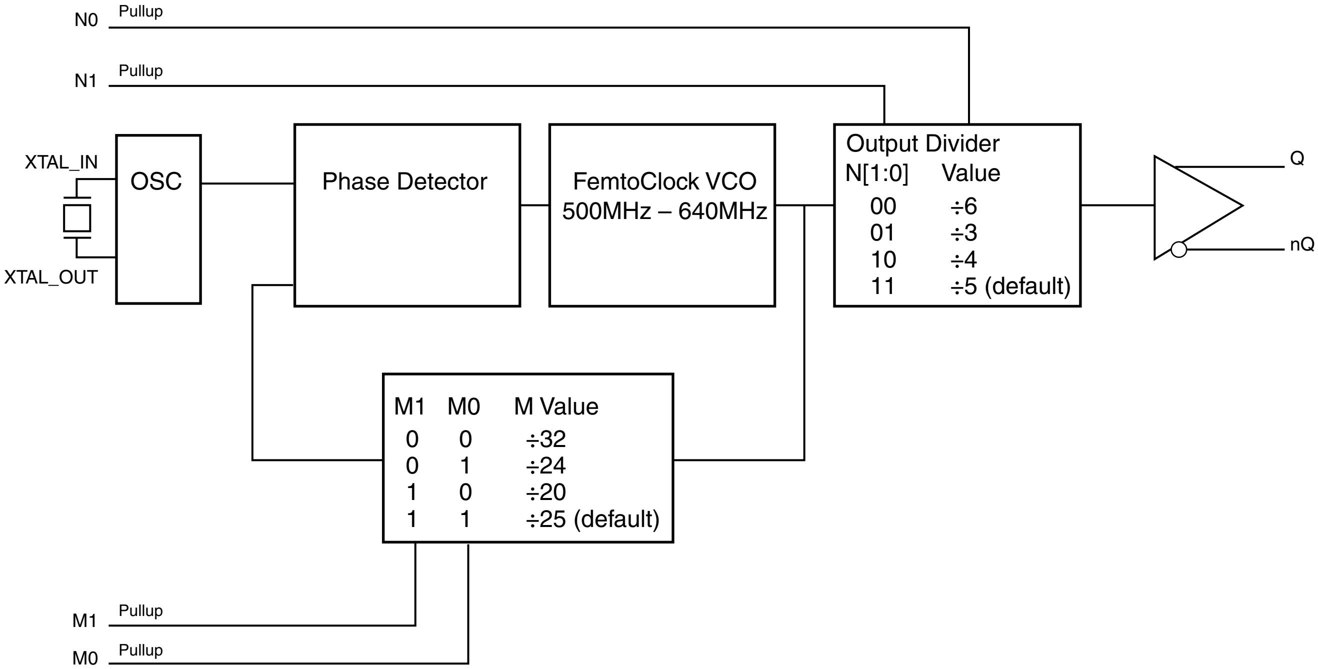


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	M1, M0	Input	Pullup	Feedback divider control inputs. Sets the feedback divider value to one of four values: ÷32, ÷25, ÷24, or ÷20 (see Table 3A). LVCMOS/LVTTL interface levels.
3	V_{EE}	Power		Negative supply pin.
4, 5	XTAL_IN XTAL_OUT	Input		Crystal oscillator interface XTAL_IN is the input, XTAL_OUT is the output. This oscillator interface can also be driven by a single-ended or differential reference clock.
6, 7	Q, nQ	Output		Differential output pair. LVPECL interface levels.
8	V_{CC}	Power		Power supply pin.
9, 10	N1, N0	Input	Pullup	Output divider control inputs. Sets the output divider value to one of four values: ÷3, ÷4, ÷5, or ÷6 (see Table 3B). LVCMOS/LVTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			3.5		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Table 3A. Feedback Divider M Function Table

M1	M0	M Value
0	0	÷32
0	1	÷24
1	0	÷20
1	1	÷25

Table 3B. Output Divider N Function Table

N1	N0	M Value
0	0	÷6
0	1	÷3
1	0	÷4
1	1	÷5

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	38.05°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				172	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				150	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	M[1:0], N[1:0]	V_{CC} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	M[1:0], N[1:0]	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA

Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CC} – 2V.

Table 4E. LVPECL DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CC} – 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		15.625		32	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 6A. AC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		83.33		213.33	MHz
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 1				45	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 2	156.25MHz, Integration Range: 1.875MHz – 20MHz		0.44		ps
		125MHz, Integration Range: 1.875MHz – 20MHz		0.47		ps
		100MHz, Integration Range: 1.875MHz – 20MHz		0.48		ps
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 3	100MHz, (1.2MHz – 21.9MHz), 10^6 samples, 25MHz crystal input		17.20		ps
		125MHz, (1.2MHz – 21.9MHz), 10^6 samples, 25MHz crystal input		16.52		ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 4	100MHz, 25MHz crystal input		1.70		ps
		125MHz, 25MHz crystal input		1.61		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		47		53	%
t_{LOCK}	PLL Lock Time; NOTE 5				100	ms

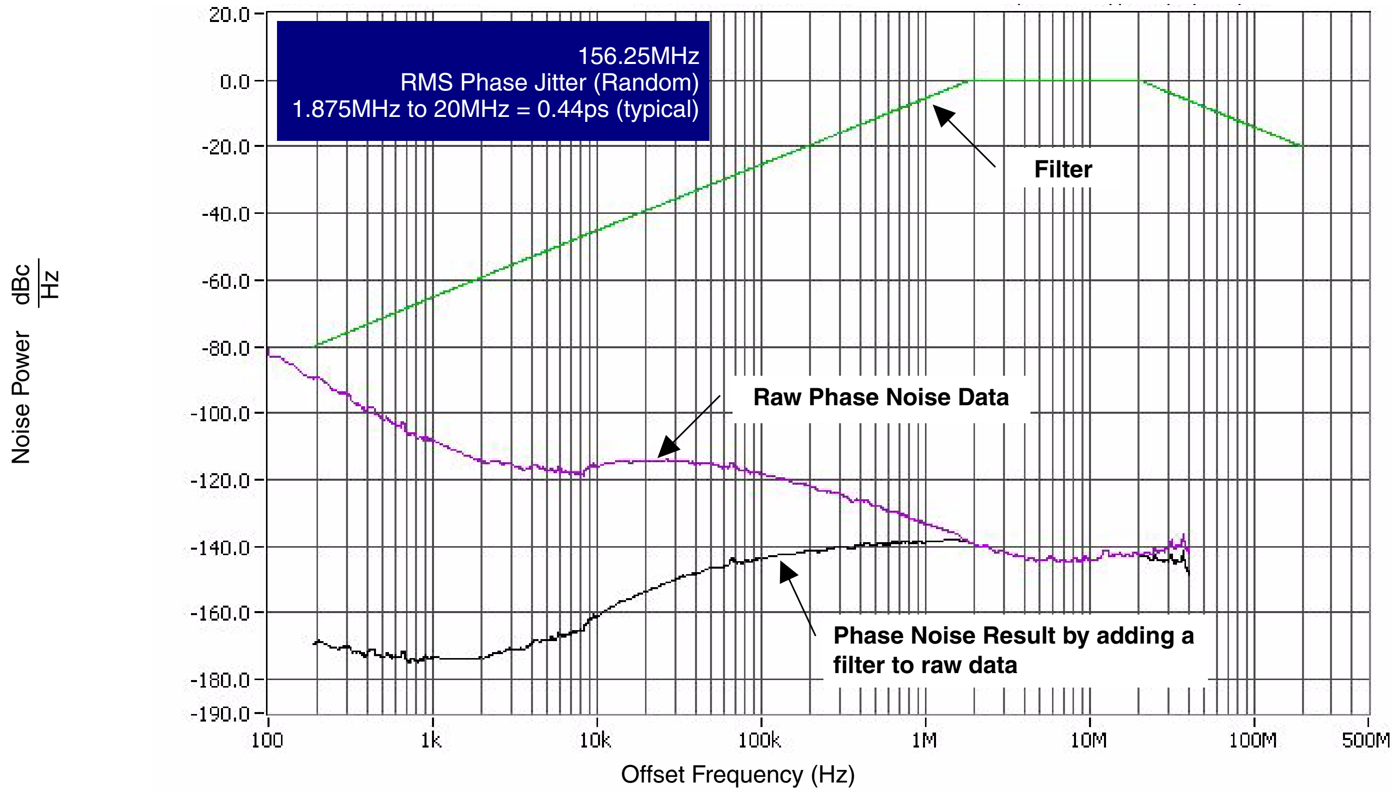
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Please refer to the Phase Noise plots.
NOTE 3: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.
NOTE 4: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE 5: This parameter is guaranteed using a 25MHz crystal.

Table 6B. AC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

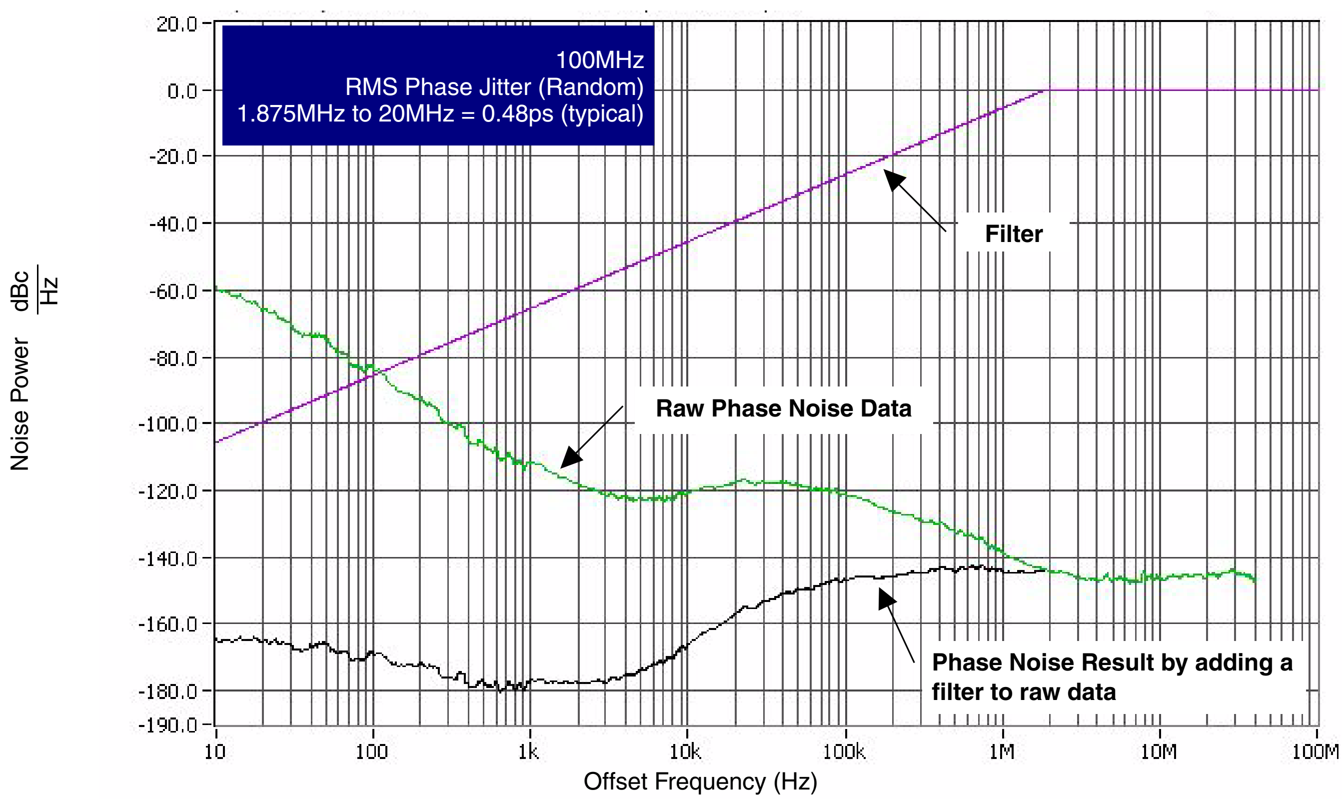
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		83.33		213.33	MHz
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 1				45	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 2	156.25MHz, Integration Range: 1.875MHz – 20MHz		0.44		ps
		125MHz, Integration Range: 1.875MHz – 20MHz		0.48		ps
		100MHz, Integration Range: 1.875MHz – 20MHz		0.49		ps
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 3	100MHz, (1.2MHz – 21.9MHz), 10^6 samples, 25MHz crystal input		12.18		ps
		125MHz, (1.2MHz – 21.9MHz), 10^6 samples, 25MHz crystal input		16.41		ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 4	100MHz, 25MHz crystal input		1.47		ps
		125MHz, 25MHz crystal input		1.74		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		47		53	%
t_{LOCK}	PLL Lock Time; NOTE 5				100	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Please refer to the Phase Noise plots.
NOTE 3: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.
NOTE 4: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE 5: This parameter is guaranteed using a 25MHz crystal.

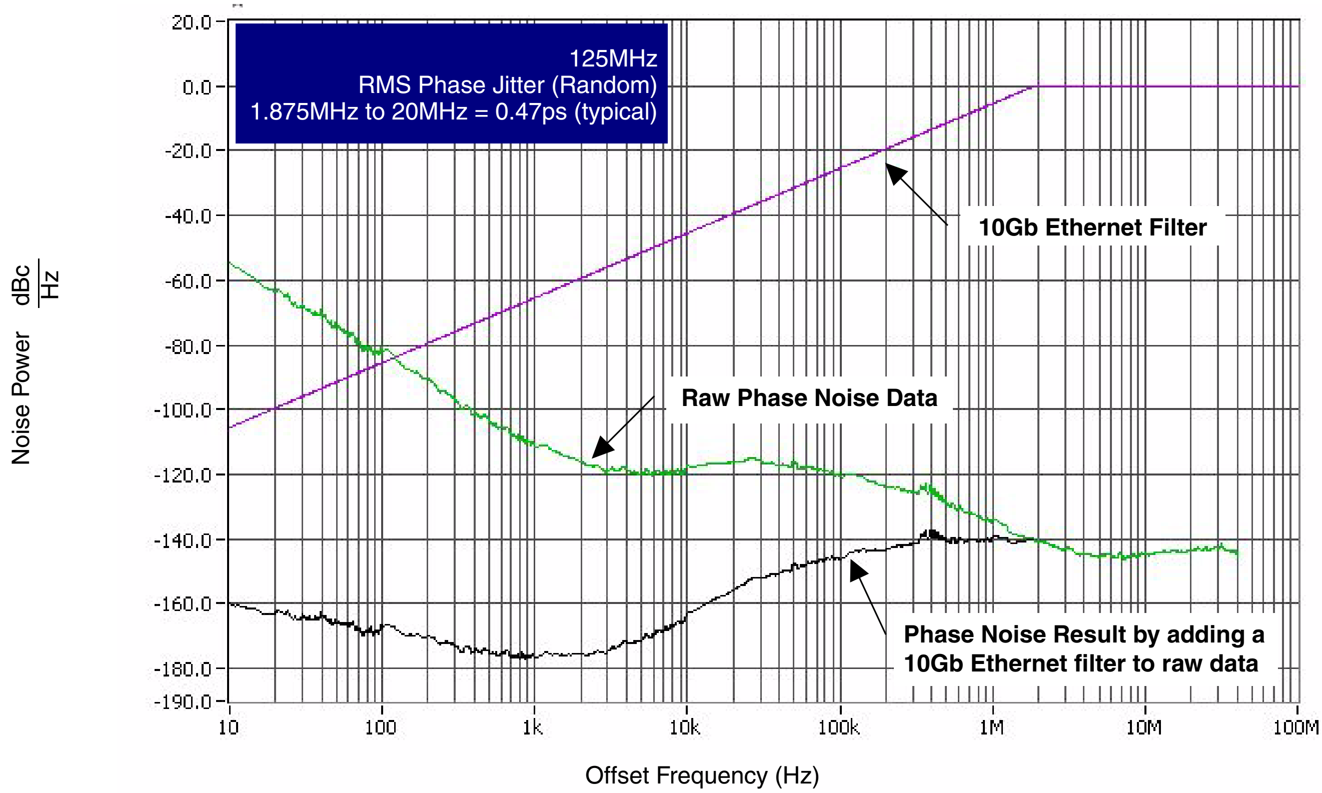
Typical Phase Noise at 156.25MHz (3.3V)



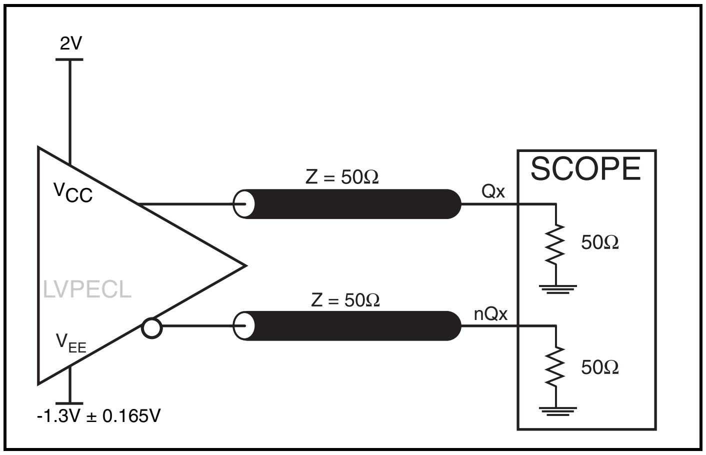
Typical Phase Noise at 100MHz (3.3V)



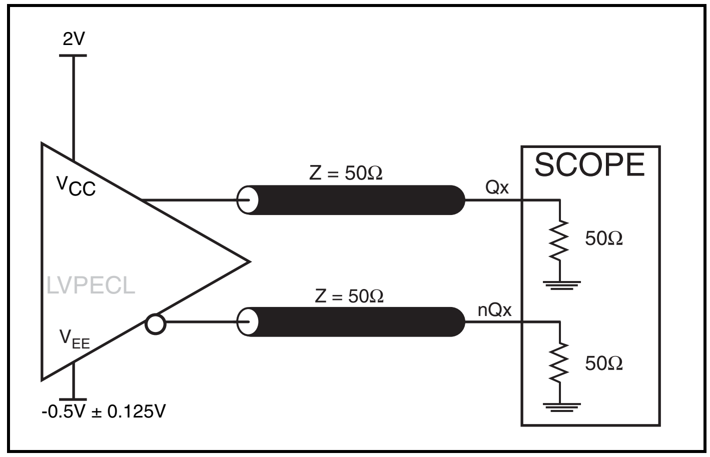
Typical Phase Noise at 125MHz (3.3V)



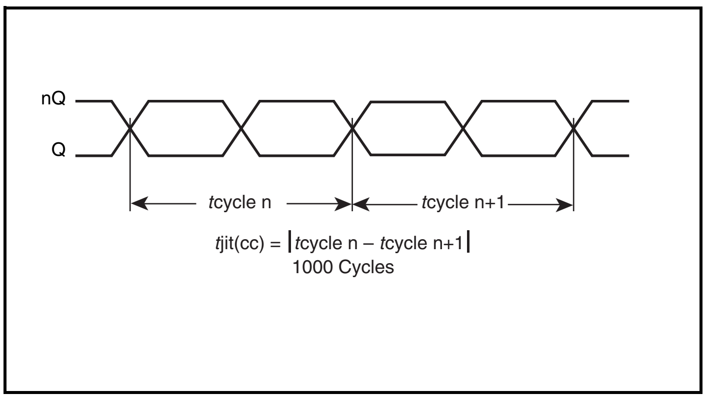
Parameter Measurement Information



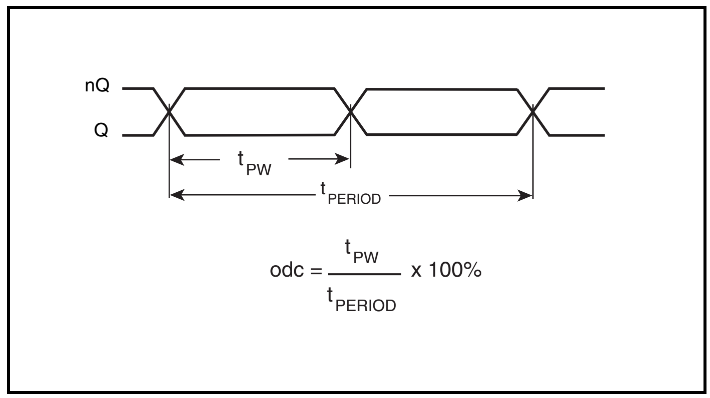
3.3V LVPECL Output Load AC Test Circuit



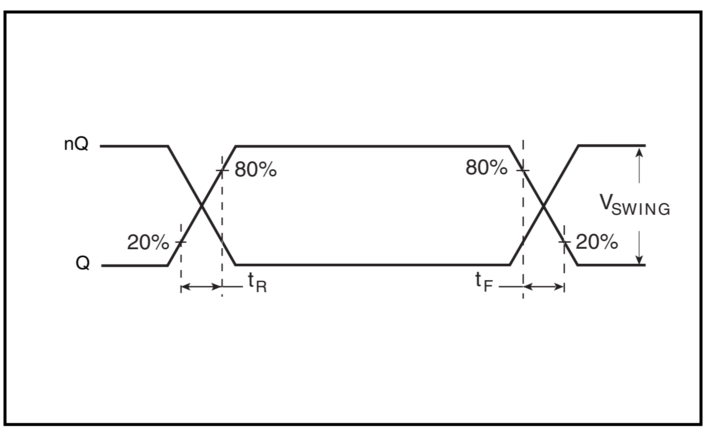
2.5V LVPECL Output Load AC Test Circuit



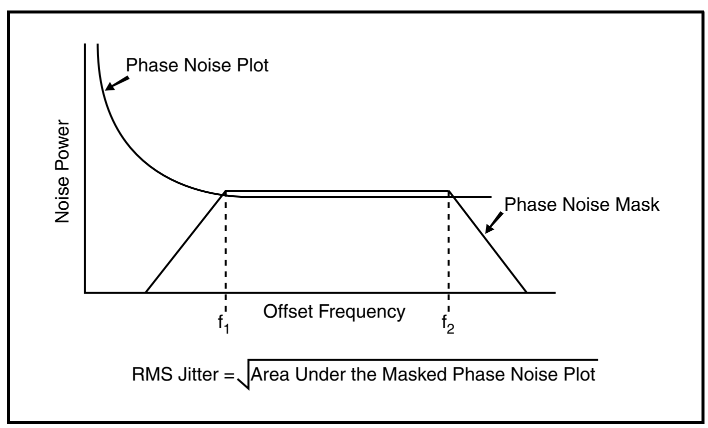
Cycle-to-Cycle Jitter



Output Duty Cycle/Pulse Width/Period

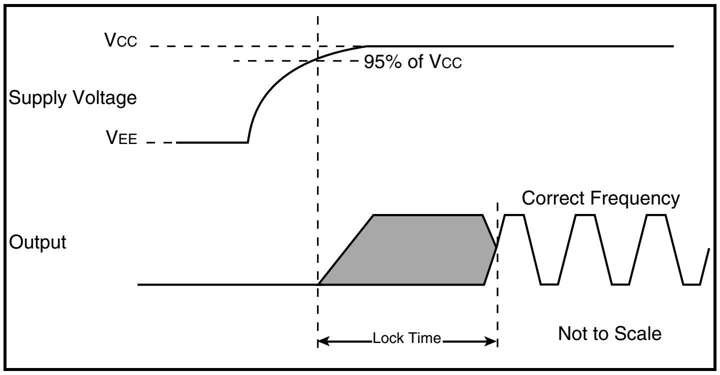


Output Rise/Fall Time



RMS Phase Jitter

Parameter Measurement Information, continued



PLL Lock Time

Application Informations

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Crystal Input Interface

The ICS83PR226I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 1* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

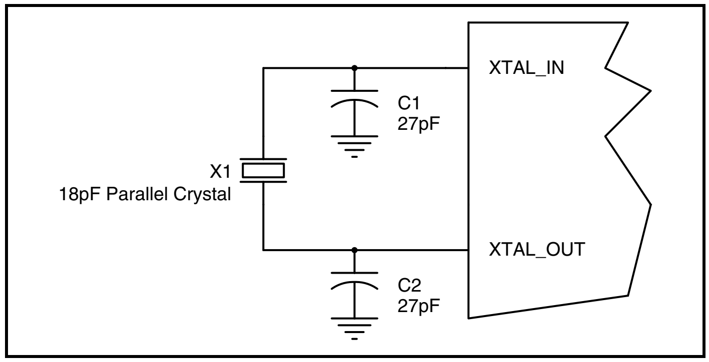


Figure 1. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 2A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

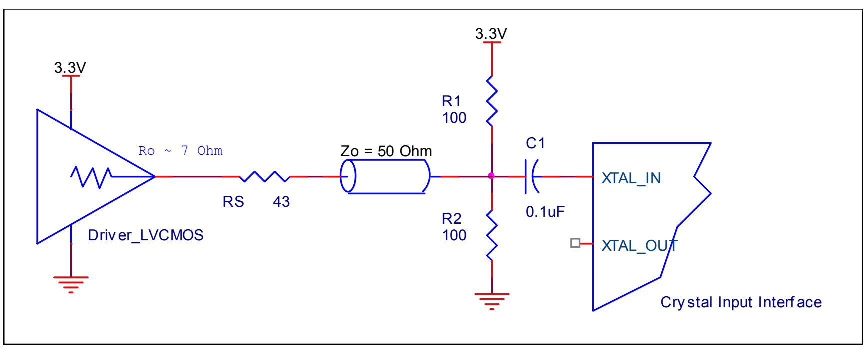


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

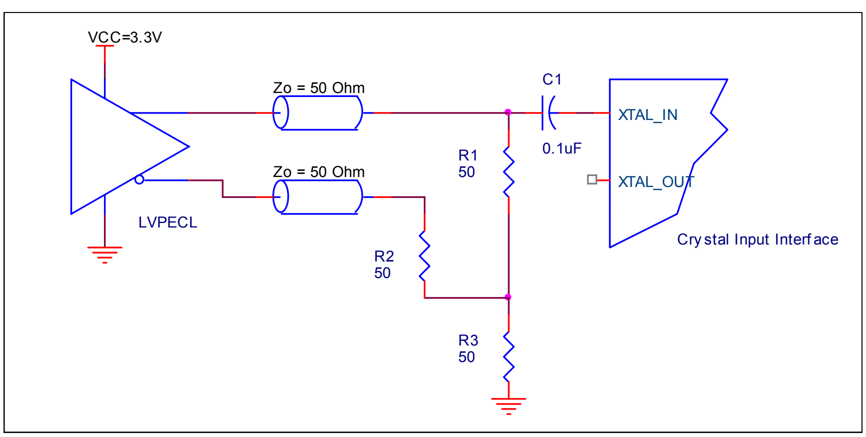


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

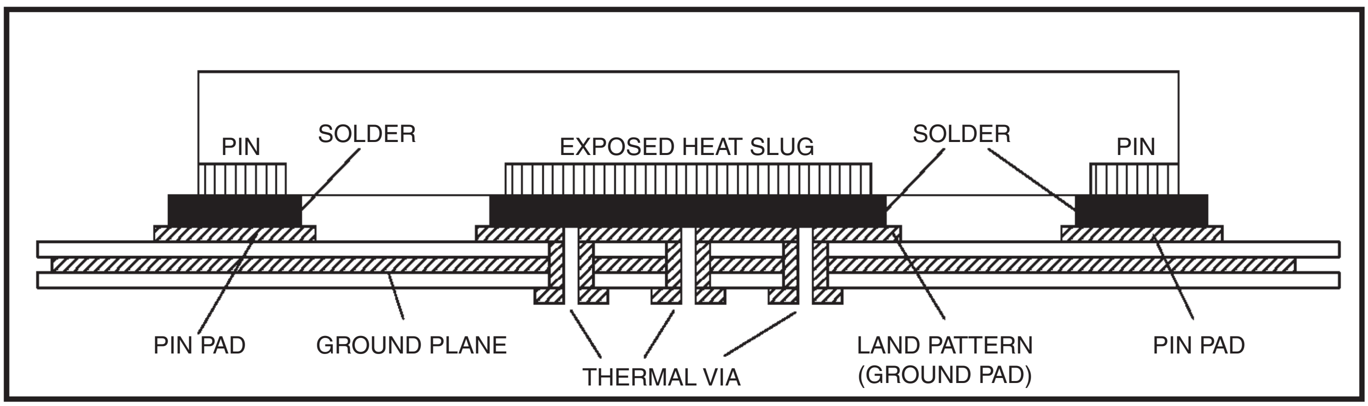


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible signals. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

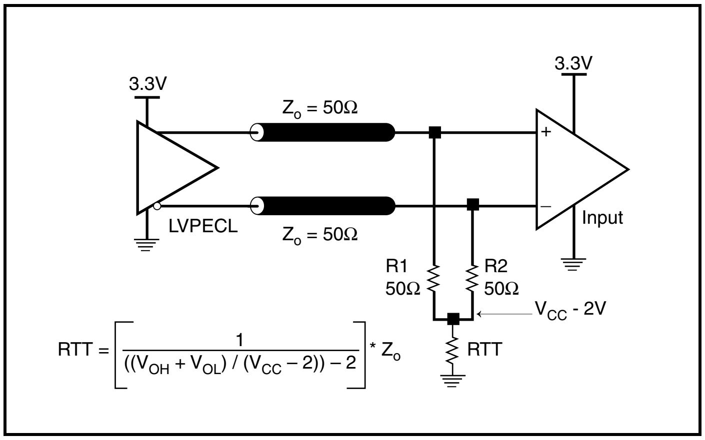


Figure 4A. 3.3V LVPECL Output Termination

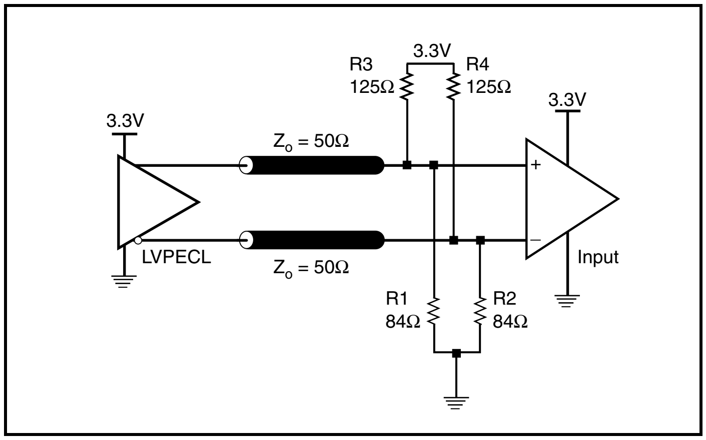


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

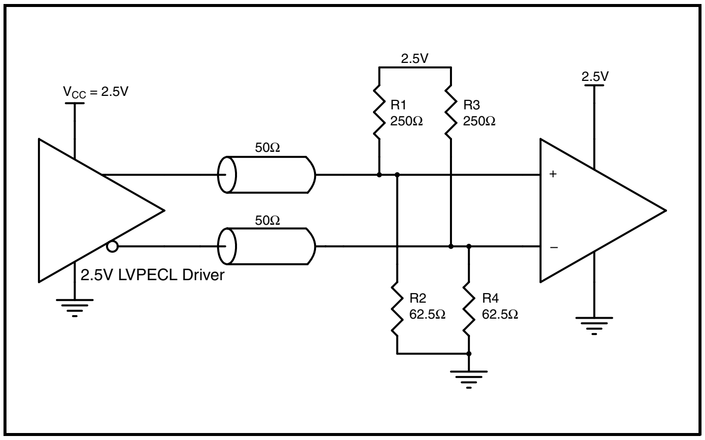


Figure 5A. 2.5V LVPECL Driver Termination Example

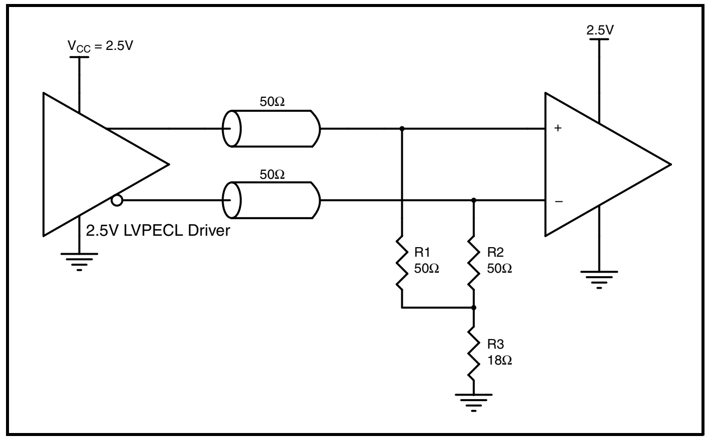


Figure 5B. 2.5V LVPECL Driver Termination Example

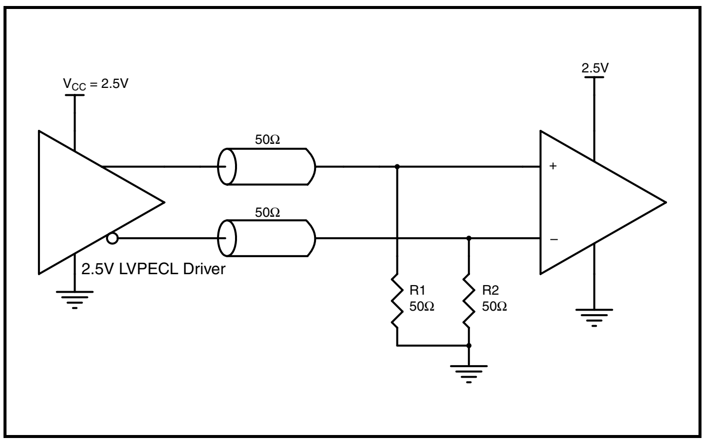


Figure 5C. 2.5V LVPECL Driver Termination Example

Schematic Example

Figure 6 shows an example of ICS83PR226I-01 application schematic. In this example, the device is operated at V_{CC} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL termination are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

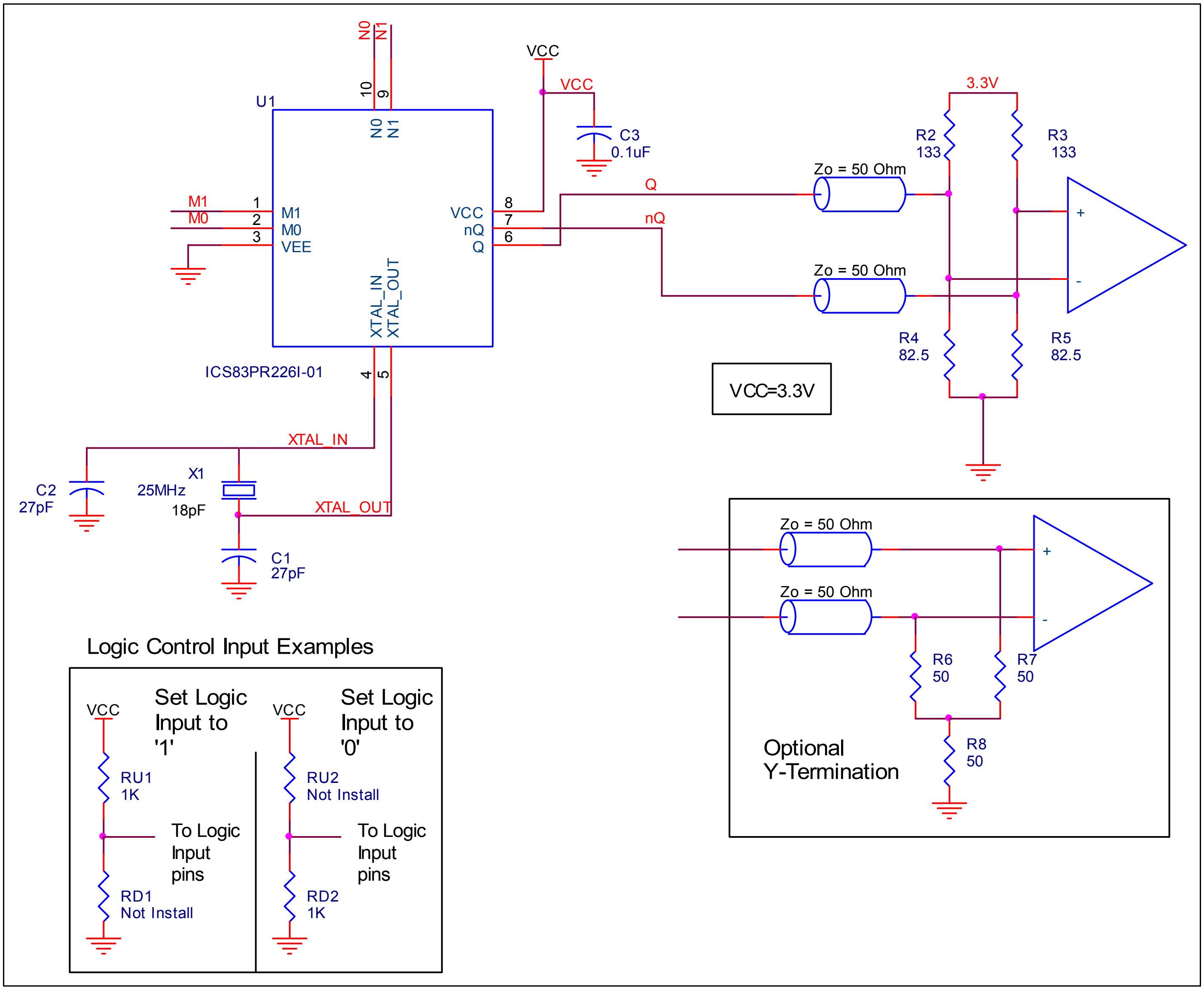


Figure 6. ICS83PR226I-01 Schematic Example

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

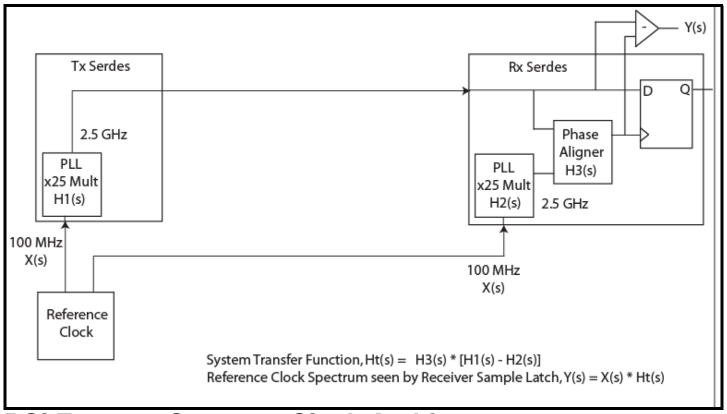
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

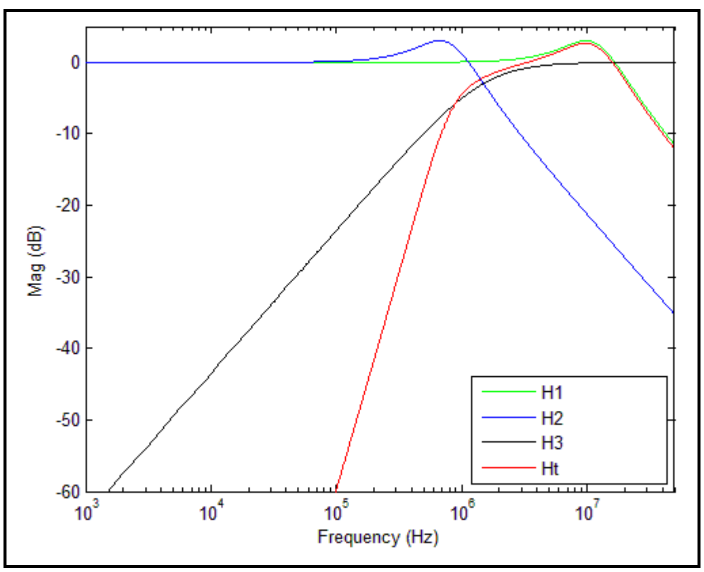
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



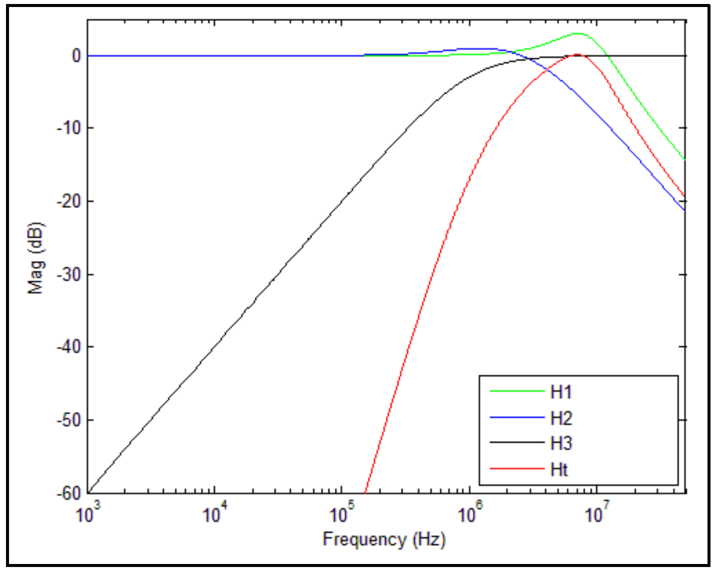
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

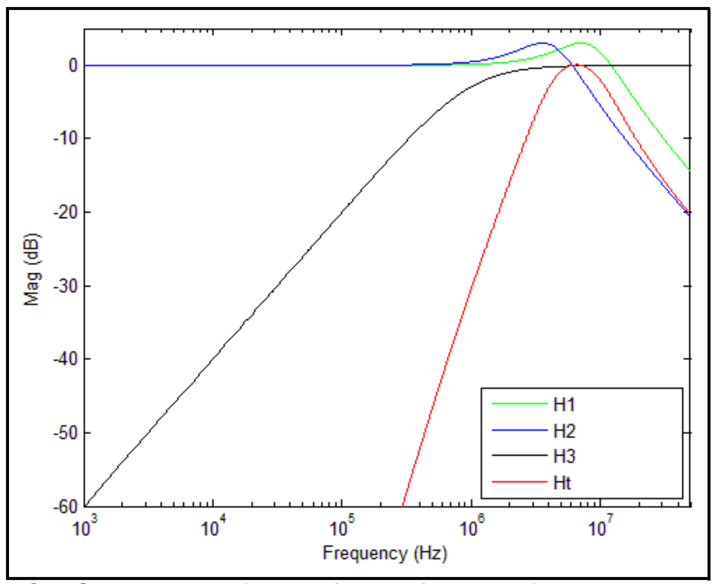


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.



PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS83PR226I-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS83PR226I-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 172mA = **595.98mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 595.98mW + 30mW = **625.98mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 38.05°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.626W * 38.05°C/W = 108.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board.

Table 7. Thermal Resistance θ_{JA} for 10 Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow	
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	38.05°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

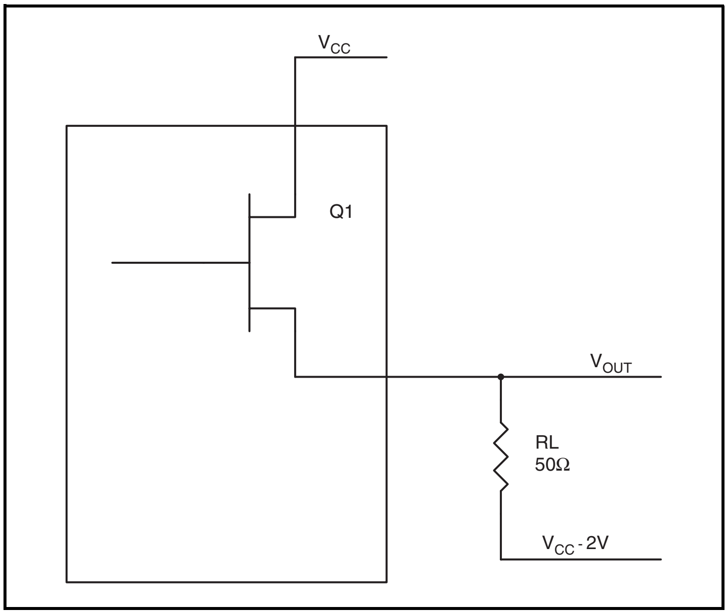


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.9V}$
  $(V_{CC\_MAX} – V_{OH\_MAX})$ = **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CO\_MAX} – 1.7V}$
  $(V_{CC\_MAX} – V_{OL\_MAX})$ = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX})$ =
[(2V – 0.9V)/50Ω] * 0.9V = **19.8mW**

Pd_L = $[(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX})$ =
[(2V – 1.7V)/50Ω] * 1.7V = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 10 Lead VFQFN

θ_{JA} vs. Air Flow	
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	38.05°C/W

Transistor Count

The transistor count for ICS83PSR226I-01 is: 6613

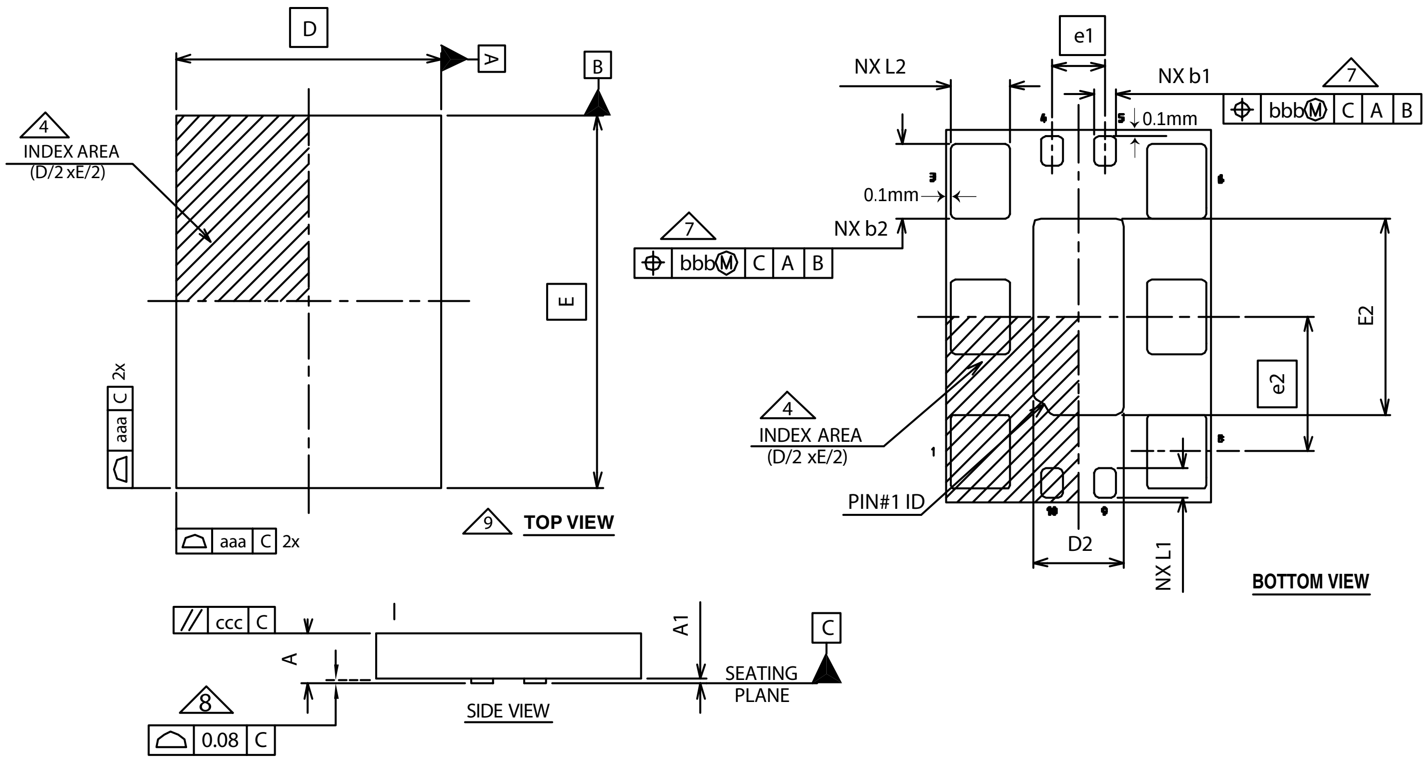
Package Dimensions

Table 9. Package Dimensions for 10-Lead VFQFN

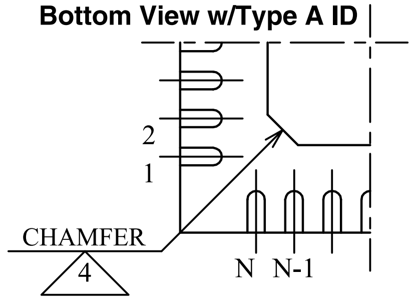
VNJR-1 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		10	
A	0.80	0.90	1.00
A1	0	0.02	0.05
b1	0.35	0.40	0.45
b2	1.35	1.40	1.45
D		5.00 Basic	
D2	1.55	1.70	1.80
E		7.00 Basic	
E2	3.55	3.70	3.80
e1		1.0	
e2		2.54	
L1	0.45	0.55	0.65
L2	1.0	1.10	1.20
N	10		
N_D	2		
N_E	3		
aaa	0.15		
bbb	0.10		
ccc	0.10		

Package Outline

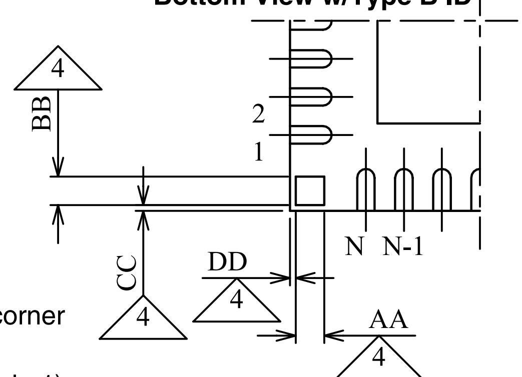
Package Outline - K Suffix for 10-Lead VFQFN



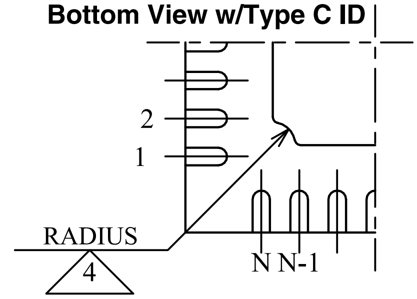
Bottom View w/Type A ID



Bottom View w/Type B ID



Bottom View w/Type C ID



There are 3 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type B: Dummy pad between pin 1 and N.
3. Type C: Mouse bite on the paddle (near pin 1)

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83PR226BKI-01LF	ICS3R226BI1L	“Lead-Free” 10 Lead VFQFN	Tray	-40°C to 85°C
83PR226BKI-01LFT	ICS3R226BI1L	“Lead-Free” 10 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		19	Package Dimensions - added 0.1mm dimension to small pad	7/31/08
B	T6A, T6B	5 - 6 10 11 16 20	AC Characteristics Tables - added PLL Lock Time spec. Added thermal note and updated PCIe notes. Added PLL Lock Time Diagram. Updated *Overdriving the XTAL Interface* section. Added PCIe Application Note. Updated Package Outline.	8/2/10
B	T6A, T6B	5 - 6	AC Characteristics Tables - added NOTE 5 to PLL Lock Time.	8/10/10

We've Got Your Timing Solution

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056