

STANDARD CAPACITANCE TVS ARRAY

APPLICATIONS

- ✓ Cellular Phones
- ✓ MP3 Players
- ✓ Personal Digital Assistant (PDA)
- ✓ Notebooks
- ✓ Digital Cameras

IEC COMPATIBILITY (EN61000-4)

- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns

FEATURES

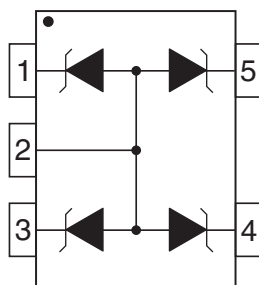
- ✓ 100 Watts Peak Pulse Power per Line ($t_p=8/20\mu s$)
- ✓ Available in 2 Voltages: 5V & 12V
- ✓ Up to Four (4) Lines of Protection
- ✓ ESD Protection > 25 kilovolts
- ✓ Low Clamping Voltage

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SC-70-4L Package
- ✓ Weight 14 milligrams (Approximate)
- ✓ Flammability rating UL 94V-0
- ✓ 8mm Tape and Reel Per EIA Standard 481
- ✓ Marking: Marking Code & Pin One Defined By DOT on Package



PIN CONFIGURATIONS

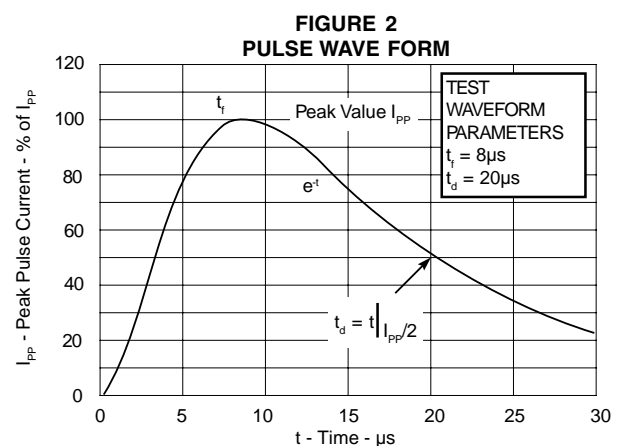
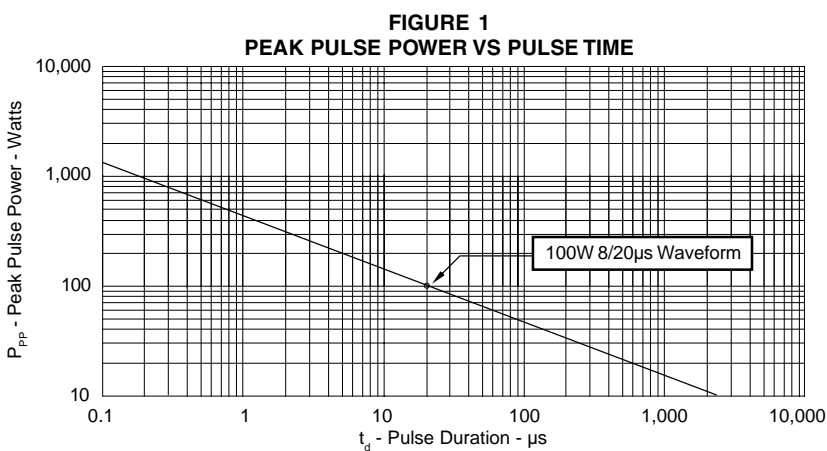


DEVICE CHARACTERISTICS

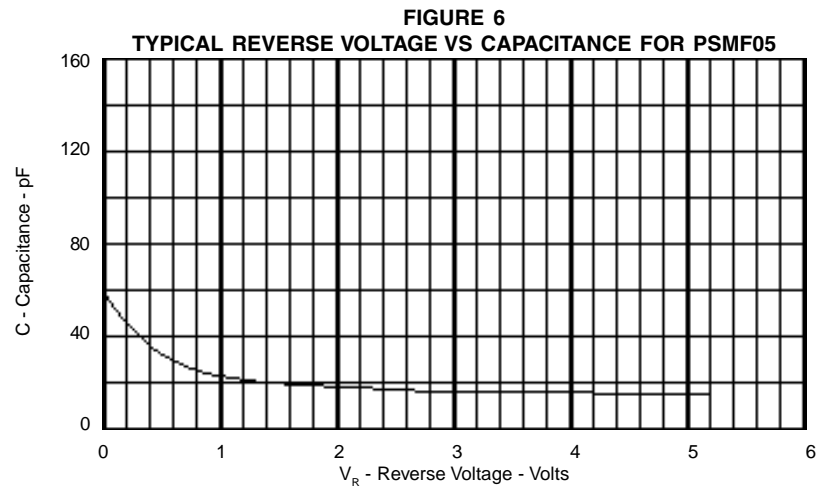
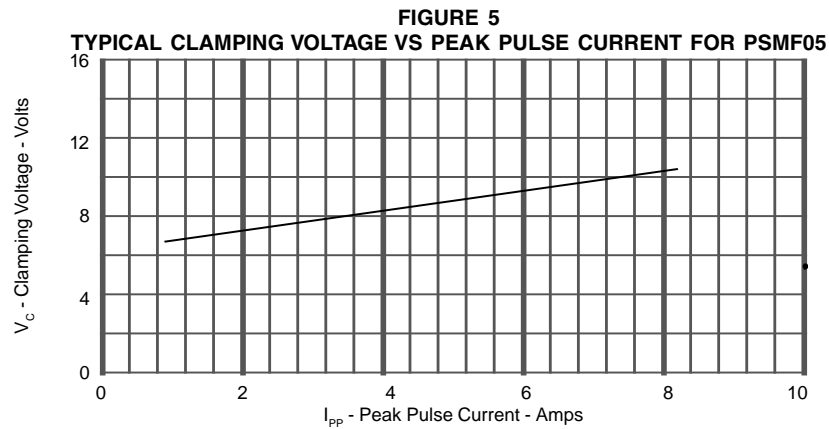
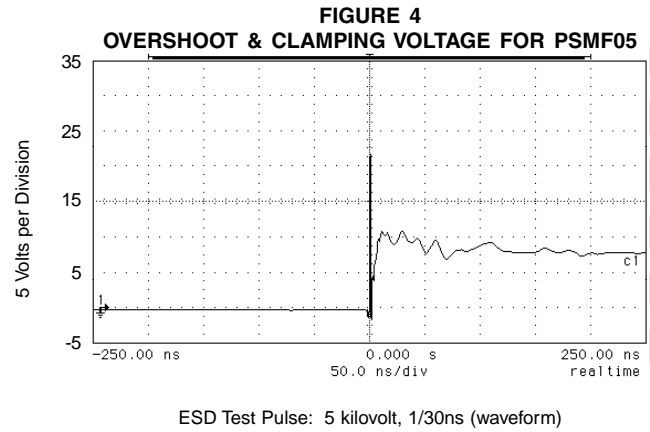
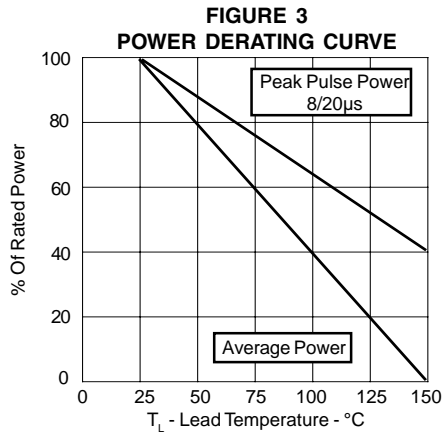
MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$) - See Figure 1	P_{PP}	100	Watts
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C
Forward Voltage @ 1A, 8/20 μs	V_{FP}	1.5	Volts

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified							
PART NUMBER	DEVICE MARKING CODE	RATED STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE (See Note 1)	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	MAXIMUM LEAKAGE CURRENT	MAXIMUM CAPACITANCE
		V_{WM} VOLTS	@ 1mA $V_{(BR)}$ VOLTS	@ $I_p = 1A$ V_C VOLTS	@ 8/20 μs V_C @ I_{PP}	@ V_{WM} I_D μA	@ 0V, 1 MHz C_J pF
PSMF05	05	5.0	6.0	9.5	12.0V @ 9.0A	10	60
PSMF12	12	12.0	13.3	15.0	22.0V @ 5.0A	1	30

Note 1: Test between pins 1 to 2, 3 to 2, 4 to 2 and 5 to 2.



GRAPHS



APPLICATION NOTE

The PSMF Series are TVS arrays designed to protect I/O or data lines from the damaging effects of ESD or EFT. This product provides unidirectional protection, with a surge capability of 200 Watts P_{PP} per line for an 8/20 μ s waveform and ESD protection > 25 kilovolts.

UNIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 1)

The PSMF Series provides up to four (4) lines of protection in a common-mode configuration as depicted in Figure 1. Circuit connectivity is as follows:

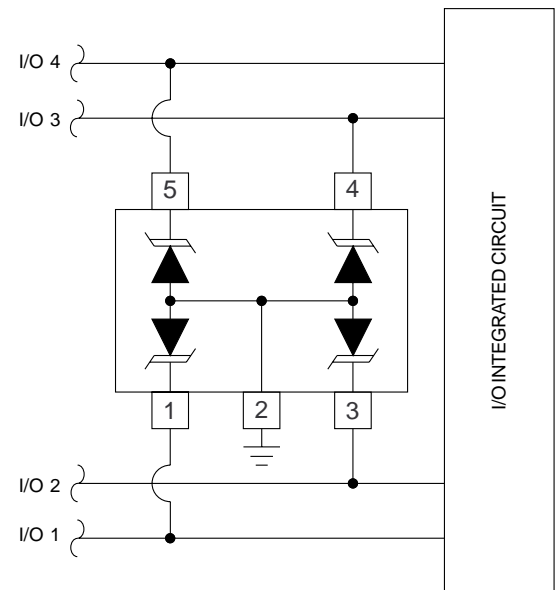
- ✓ I/O 1 is connected to Pin 1.
- ✓ I/O 2 is connected to Pin 3.
- ✓ I/O 3 is connected to Pin 4.
- ✓ I/O 4 is connected to Pin 5.
- ✓ Pin 2 is connected to ground.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

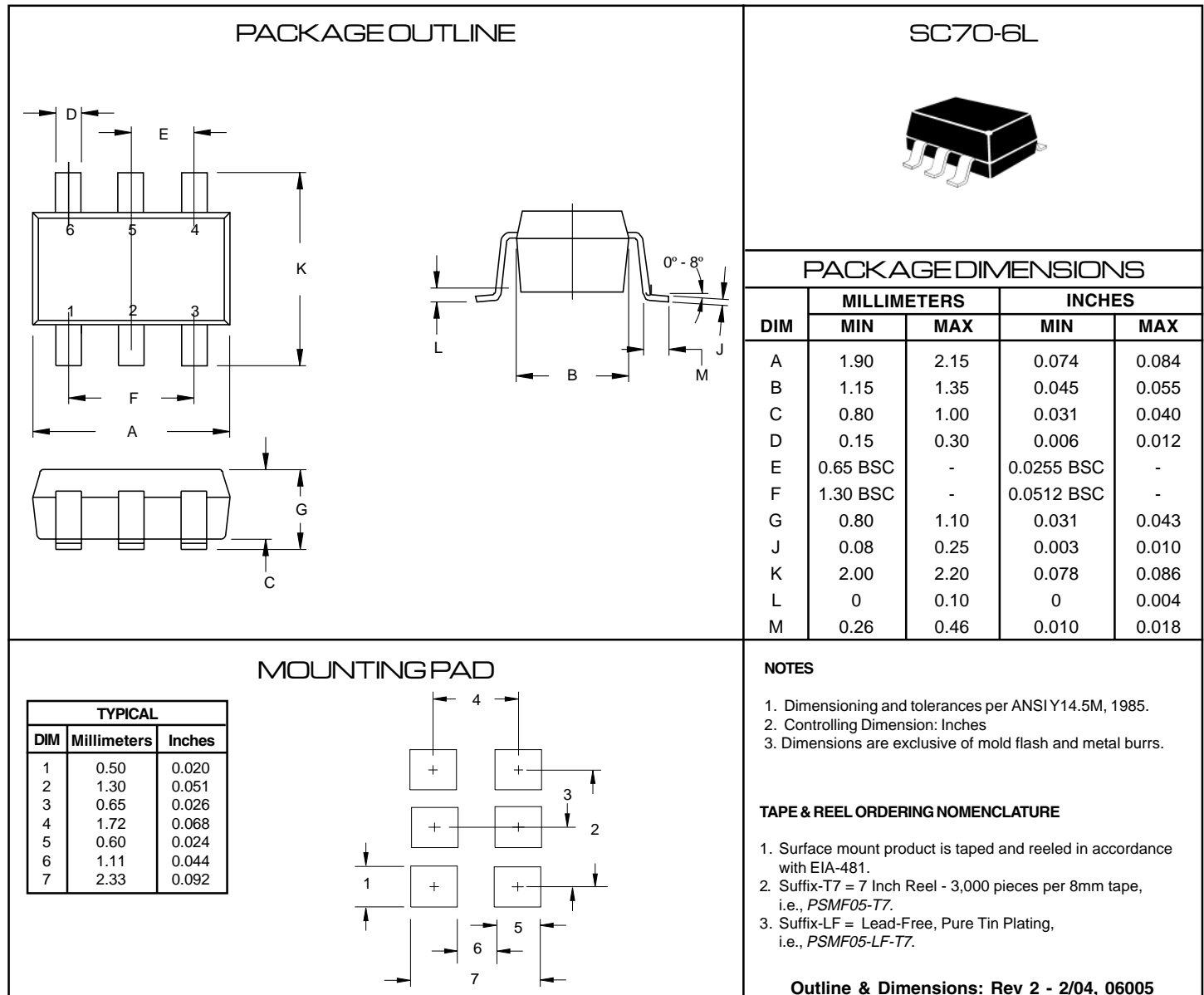
Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 1 - Unidirectional Configuration
Common-Mode I/O Port Protection



PACKAGE OUTLINE & DIMENSIONS



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