



STD70N02L STD70N02L-1

N-channel 25V - 0.0068Ω - 60A - DPAK - IPAK
STripFET™ III Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D
STD70N02L	25V	<0.008Ω	60A
STD70N02L-1	25V	<0.008Ω	60A

- R_{DS(ON)} * Qg industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

Application

- Switching applications

Description

This series of products utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

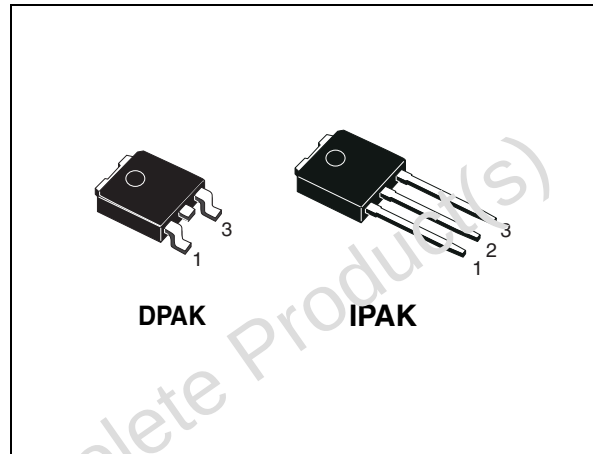


Figure 1. Internal schematic diagram

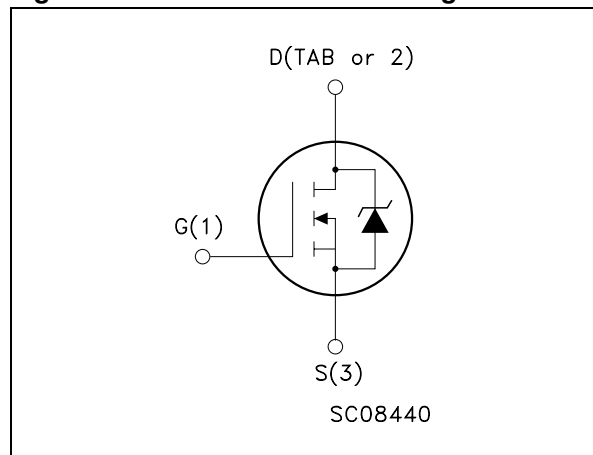


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD70N02L-1	D70N02L	IPAK	Tube
STD70N02L	D70N02L	DPAK	Tape & reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{\text{spike}}^{(1)}$	Drain-source voltage rating	30	V
V_{DS}	Drain-source voltage ($V_{\text{GS}} = 0$)	25	V
V_{DGR}	Drain-gate voltage ($R_{\text{GS}} = 20\text{k}\Omega$)	25	V
V_{GS}	Gate-source voltage	± 20	V
$I_{\text{D}}^{(2)}$	Drain current (continuous) at $T_{\text{C}} = 25^{\circ}\text{C}$	60	A
I_{D}	Drain current (continuous) at $T_{\text{C}} = 100^{\circ}\text{C}$	42	A
$I_{\text{DM}}^{(3)}$	Drain current (pulsed)	240	A
P_{TOT}	Total dissipation at $T_{\text{C}} = 25^{\circ}\text{C}$	60	W
	Derating factor	0.4	W/ $^{\circ}\text{C}$
$E_{\text{AS}}^{(4)}$	Single pulse avalanche energy	280	mJ
T_{j} T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^{\circ}\text{C}$

1. Guaranteed when external $R_{\text{g}}=4.7\Omega$ and $T_{\text{f}}<T_{\text{fmax}}$

2. Value limited by wire bonding

3. Pulse width limited by safe operating area

4. Starting $T_{\text{j}}=25^{\circ}\text{C}$, $I_{\text{d}} = 60\text{A}$, $V_{\text{DD}} = 15\text{V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{\text{thj-case}}$	Thermal resistance junction-case Max	2.5	$^{\circ}\text{C/W}$
$R_{\text{thj-amb}}$	Thermal resistance junction-amb Max	100	$^{\circ}\text{C/W}$
T_{l}	Maximum lead temperature for soldering purpose	275	$^{\circ}\text{C}$

2 Electrical characteristics

(T_{case} = 25°C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 25mA, V _{GS} = 0	25			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 20V, V _{DS} = 20V, T _c = 125°C			1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250μA	1	1.8		V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 30A V _{GS} = 5V, I _D = 15A		0.0068 0.090	0.008 0.014	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15V, I _D = 30A		27		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 16V, f = 1MHz, V _{GS} = 0		1400 400 55		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 10V, I _D = 60A V _{GS} = 10V (see Figure 8)		24 5 3.4	32	nC nC nC
R _G	Gate input resistance	f = 1MHz Gate DC Bias = 0 test signal level = 20mV open drain	0.5	1.5	3	Ω
Q _{OSS} ⁽²⁾	Output charge	V _{DS} = 16V, V _{GS} = 0V		9.4		nC

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%

2. Q_{OSS} = C_{OSS} * D Vin, C_{OSS} = C_{gd} + C_{gd}. (see [Appendix A](#))

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=10V$, $I_D=30A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 18)		10		ns
t_r	Rise time			130		ns
$t_{d(off)}$	Turn-off delay time			27		ns
t_f	Fall time			16	21.6	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				50	A
I_{SDM}	Source-drain current (pulsed)				200	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD}=30A$, $V_{GS}=0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD}=60A$, $di/dt = 100A/\mu s$ $V_{DD}=20V$, $T_j=150^\circ C$ (see Figure 21)		36		ns
Q_{rr}	Reverse recovery charge			36		nC
I_{RRM}	Reverse recovery current			2		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

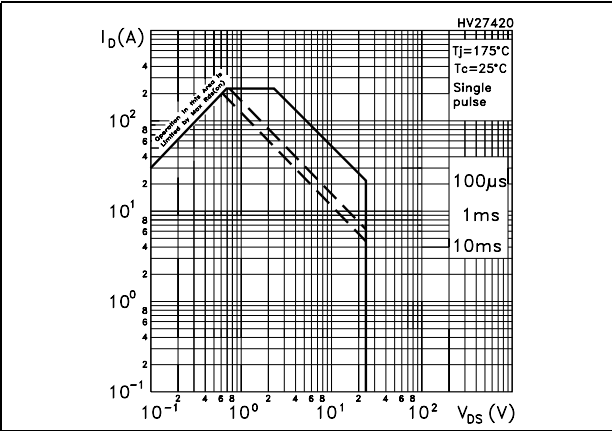


Figure 3. Thermal impedance

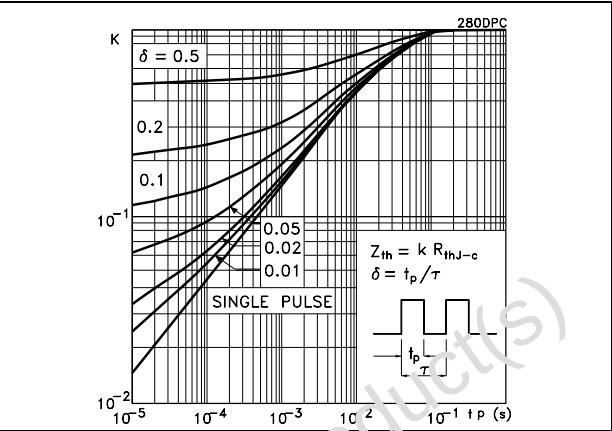


Figure 4. Output characteristics

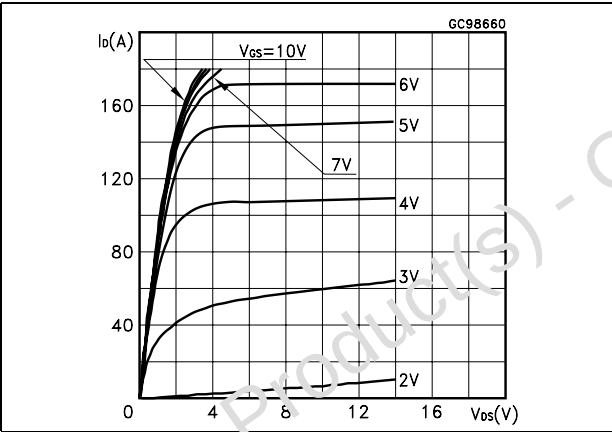


Figure 5. Transfer characteristics

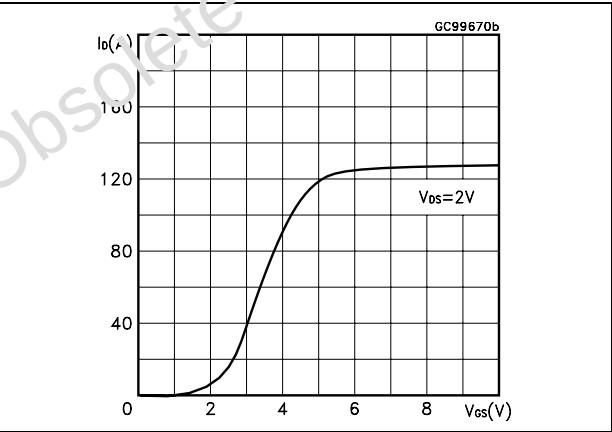


Figure 6. Transconductance

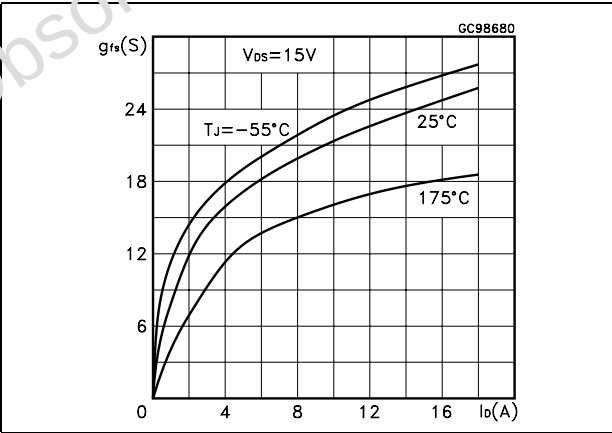


Figure 7. Static drain-source on resistance

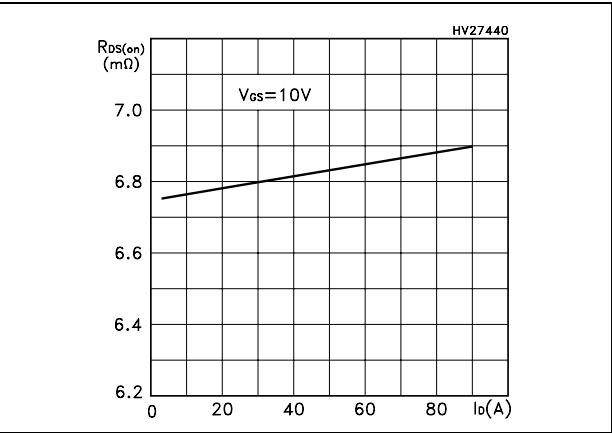


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

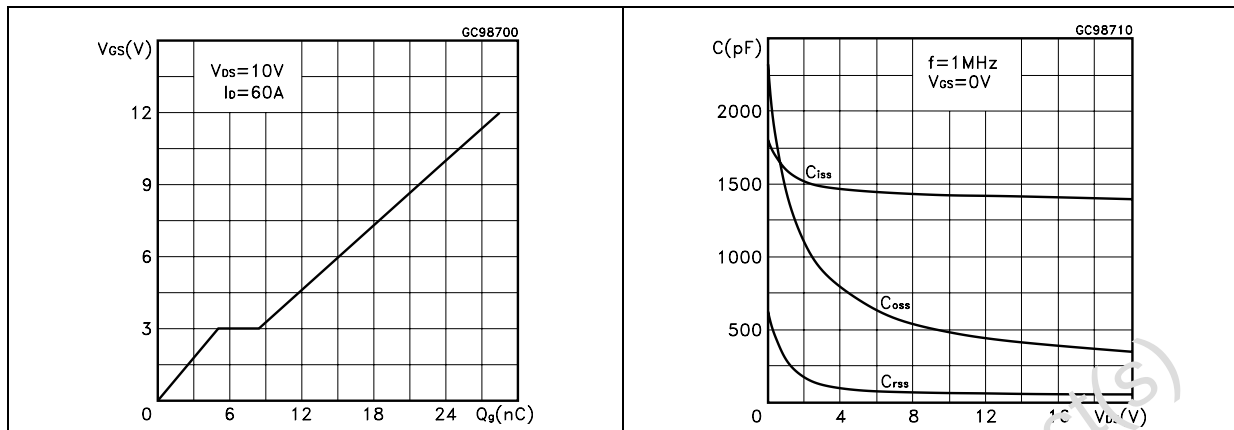


Figure 10. Normalized gate threshold voltage vs temperature

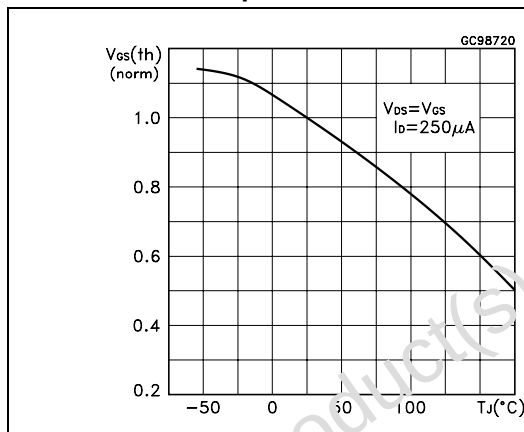


Figure 11. Normalized on resistance vs temperature

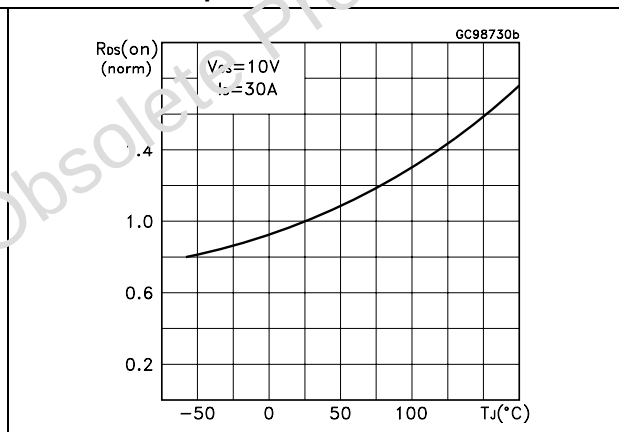


Figure 12. Source-drain diode forward characteristics

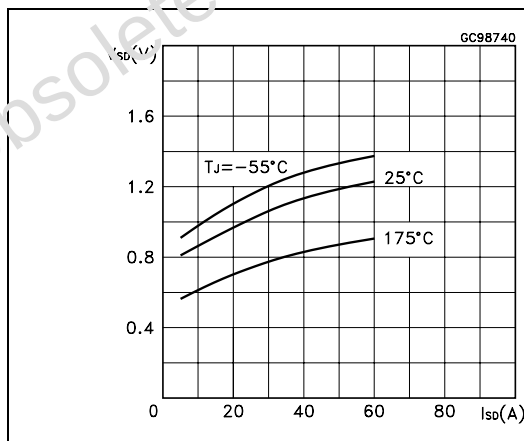
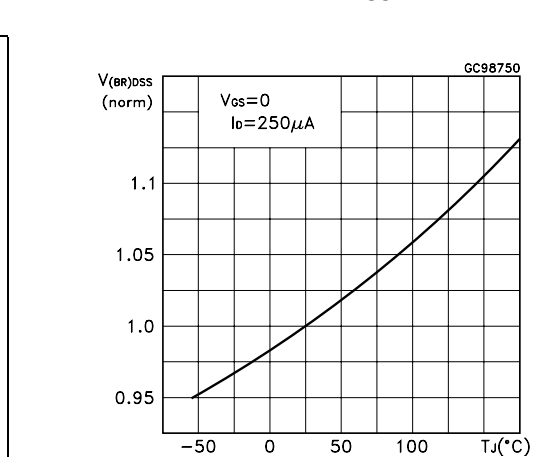
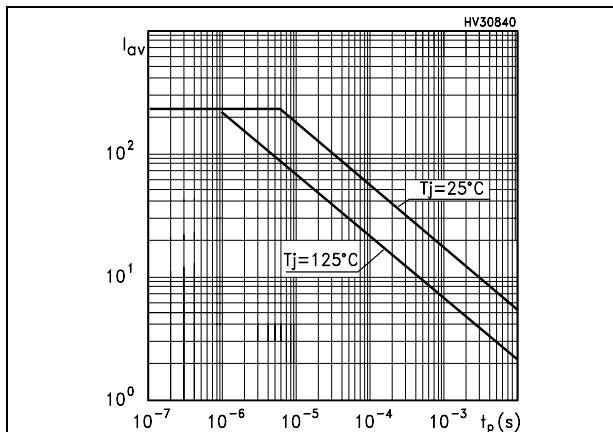
Figure 13. Normalized B_{VDS} vs temperature

Figure 14. Allowable I_{AV} vs time in avalanche

The previous curve gives the single pulse safe operating area for unclamped inductive loads, under the following conditions:

$$P_{D(AVE)} = 0.5 \cdot (1.3 \cdot B_{VDSS} \cdot I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} \cdot t_{AV}$$

Where:

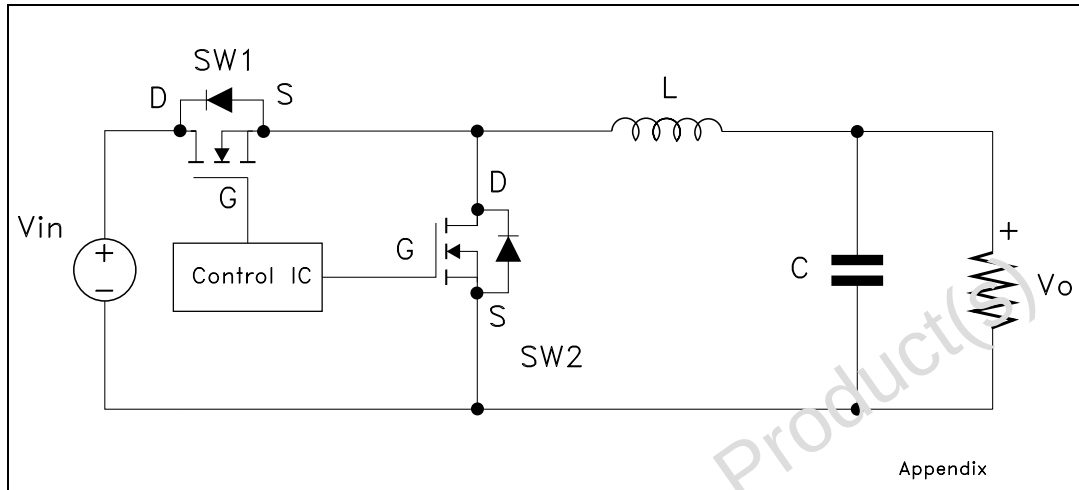
I_{AV} is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalanche (single pulse)

t_{AV} is the time in avalanche

Appendix A Buck convert

Figure 15. Synchronous buck converter



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

Very low $R_{DS(on)}$ to reduce conduction losses

Small Q_{gls} to reduce the gate charge losses

Small C_{oss} to reduce losses due to output capacitance

Small Q_{rr} to reduce losses on SW1 during its turn-on

The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon.

The high side (SW1) device requires:

Small R_G and L_G to allow higher gate current peak and to limit the voltage feedback on the gate

Small Q_g to have a faster commutation and to reduce gate charge losses

Low $R_{DS(on)}$ to reduce the conduction losses

Table 8. Power losses

		High side switch (SW1)	Low side switch (SW2)
$P_{\text{conduction}}$		$R_{\text{DS(on)}} \cdot I_L^2 \cdot \delta$	$R_{\text{DS(on)}} \cdot I_L^2 \cdot (1 - \delta)$
$P_{\text{switching}}$		$V_{\text{in}} \cdot (Q_{\text{gsth}}(\text{SW1}) + Q_{\text{gd}}(\text{SW1})) \cdot f \cdot \frac{I_L}{I_g}$	Zero voltage switching
P_{diode}	recovery	Not applicable	$V_{\text{in}} \cdot Q_{\text{rr}}(\text{SW2}) \cdot f$
	conduction	Not applicable	$V_f(\text{SW2}) \cdot I_L \cdot t_{\text{deadtime}} \cdot f$
$P_{\text{gate(Qg)}}$		$Q_g(\text{SW1}) \cdot V_{\text{gg}} \cdot f$	$Q_{\text{gls}}(\text{SW2}) \cdot V_{\text{gg}} \cdot f$
P_{Qoss}		$\frac{V_{\text{in}} \cdot Q_{\text{oss}}(\text{SW1}) \cdot f}{2}$	$\frac{V_{\text{in}} \cdot Q_{\text{oss}}(\text{SW2}) \cdot f}{2}$

Table 9. Power losses parameters

Paramter	Meaning
d	Duty-cycle
Q_{gsth}	Root threshold gate charge
Q_{gls}	Third quadrant gate charge
$P_{\text{conduction}}$	On state losses
$P_{\text{switching}}$	On-off transition losses
P_{diode}	Conduction and reverse recovery diode losses
P_{gate}	Gate driver losses
P_{Qoss}	Output capacitance losses

3 Test circuits

Figure 16. Switching times test circuit for resistive load

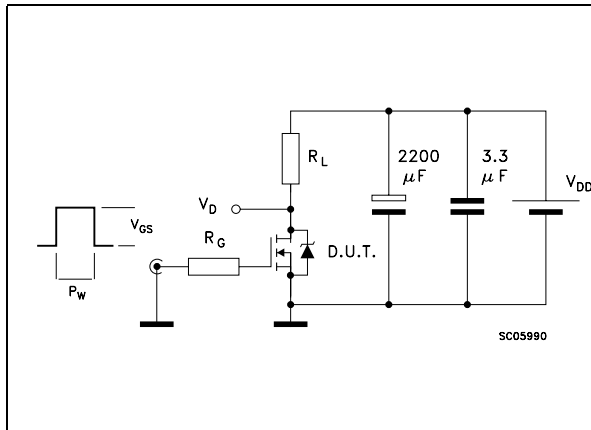


Figure 17. Gate charge test circuit

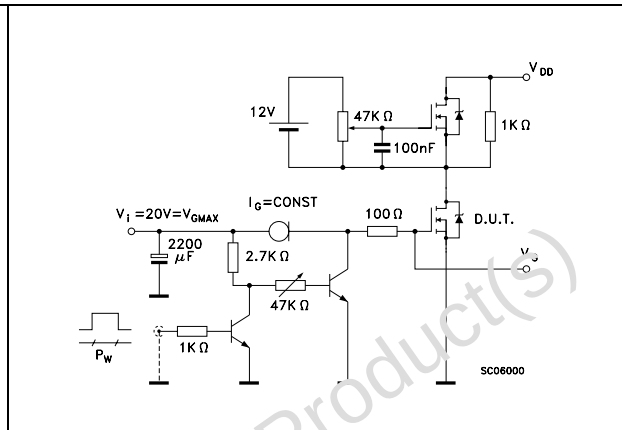


Figure 18. Test circuit for inductive load switching and diode recovery times

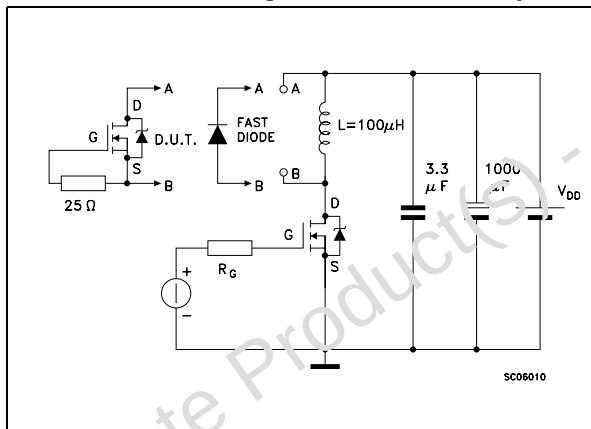


Figure 19. Unclamped inductive load test circuit

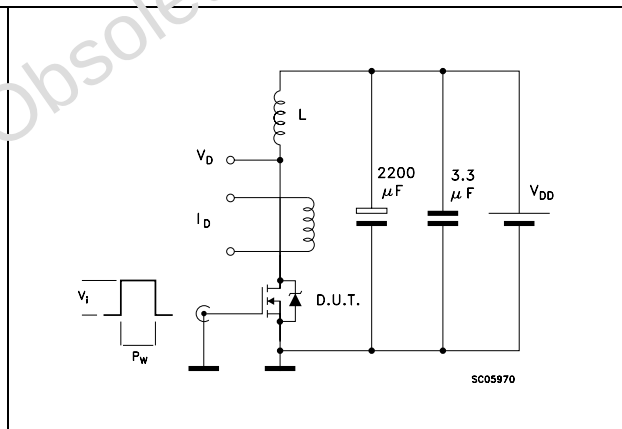


Figure 20. Unclamped inductive waveform

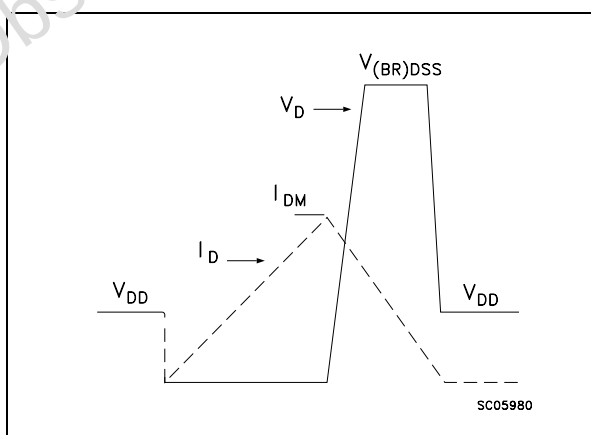
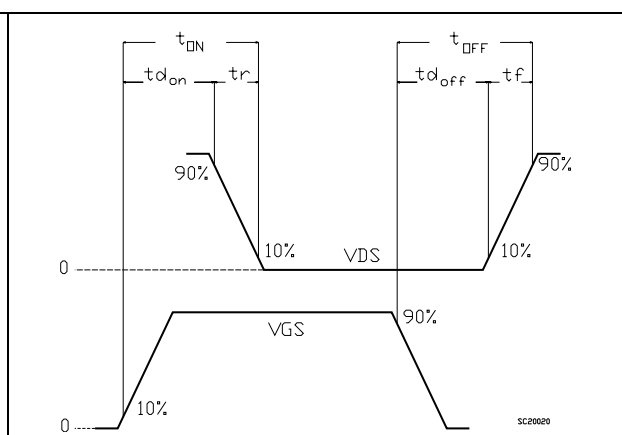


Figure 21. Switching time waveform



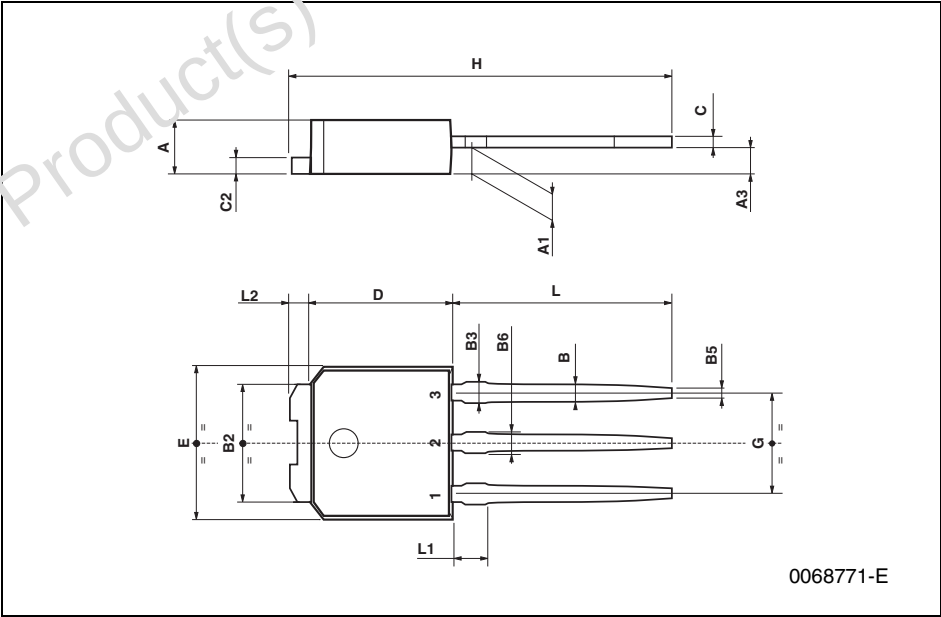
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

Obsolete Product(s) - Obsolete Product(s)

TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

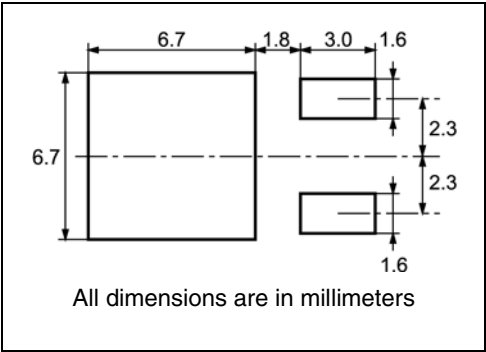


DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.201	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.369		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

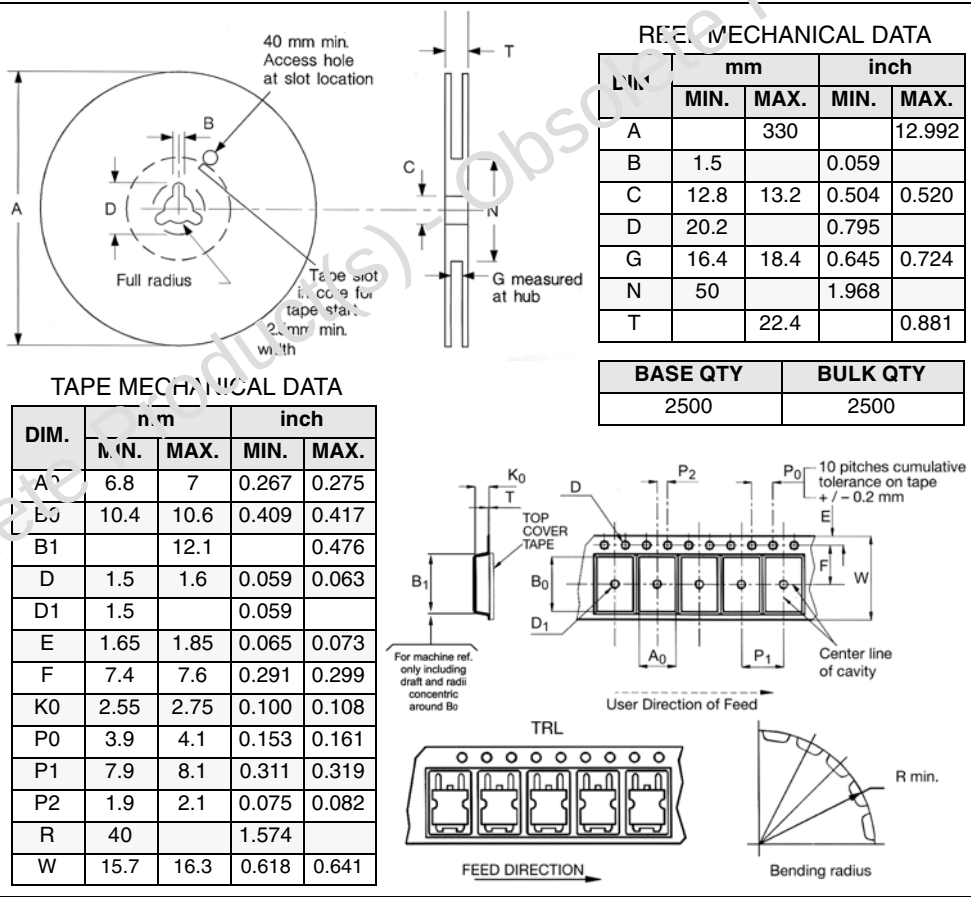
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5 Package mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Aug-2005	1	First release
02-Dec-2005	2	Modified Appendix A
07-Apr-2006	3	New template
03-May-2006	4	New value in Table 4 , new curve (see Figure 14)
25-Oct-2007	5	Updated BV _{dss} value

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