

PROTECTION PRODUCTS

Description

The SLV series of transient voltage suppressors are designed to protect low voltage, state-of-the-art CMOS semiconductors from transients caused by electrostatic discharge (ESD), cable discharge events (CDE), lightning and other induced voltage surges.

The devices are constructed using Semtech's proprietary EPD process technology. The EPD process provides low standoff voltages with significant reductions in leakage currents and capacitance over silicon-avalanche diode processes. The SLVU2.8-8 features integrated low capacitance compensation diodes that reduce the maximum capacitance to 8pF per line. This, combined with low leakage current, means signal integrity is preserved in high-speed applications such as 10/100/1000 Ethernet.

The SLVU2.8-8 is in an SO-8 package and may be used to protect four high-speed line pairs. The layout of the device minimizes trace inductance and reduces voltage overshoot associated with ESD events. The low clamping voltage of the SLVU2.8-8 minimizes the stress on the protected IC.

The SLV series TVS diodes will meet the surge requirements of IEC 61000-4-2 (ESD), IEC61000-4-5 (Lightning), and ETSI ETS 300 386.

Features

- ◆ 600 Watts peak pulse power ($t_p = 8/20\mu s$)
- ◆ Transient protection for high speed data lines to **IEC 61000-4-2 (ESD) 15kV (air), 8kV (contact)**
IEC 61000-4-4 (EFT) 40A ($t_p = 5/50ns$)
IEC 61000-4-5 (Lightning) 24A ($t_p = 8/20\mu s$)
- ◆ Protects four line pairs (eight lines)
- ◆ Comprehensive pin out for easy board layout
- ◆ Low capacitance
- ◆ High peak pulse current (30A, 8/20 μs)
- ◆ Low leakage current
- ◆ Low operating and clamping voltages
- ◆ Solid-state EPD TVS process technology

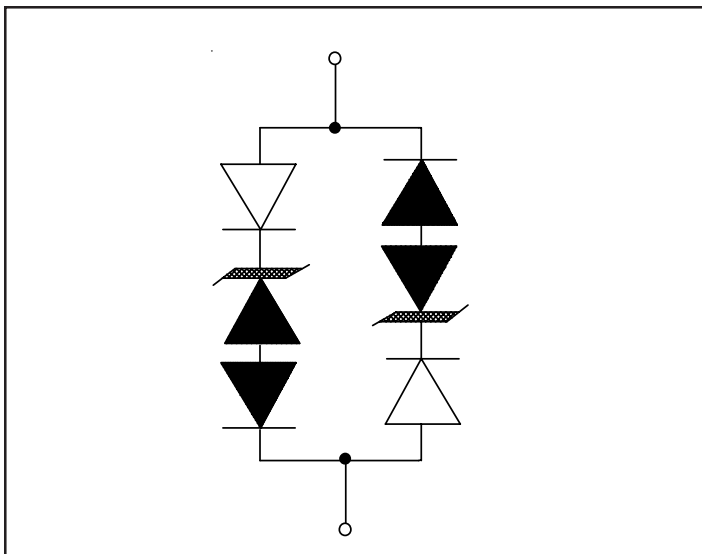
Mechanical Characteristics

- ◆ JEDEC SO-8 package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Part number, date code, logo
- ◆ Packaging : Tape and Reel per EIA 481

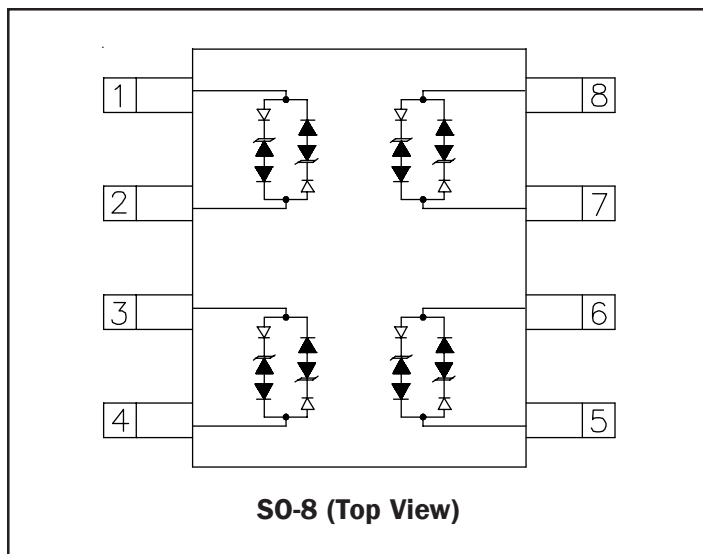
Applications

- ◆ 10/100/1000 Ethernet
- ◆ WAN/LAN Equipment
- ◆ Switching Systems
- ◆ DSLAMs
- ◆ Desktops, Servers, & Notebooks
- ◆ Instrumentation
- ◆ Base Stations
- ◆ Analog Inputs

Circuit Diagram (Each Line)



Schematic & PIN Configuration



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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{pk}	600	Watts
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{pp}	30	A
ESD Per IEC 61000-4-2 (Air) ESD Per IEC 61000-4-2 (Contact)	ESD	30 25	kV
Operating Temperature	T_j	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

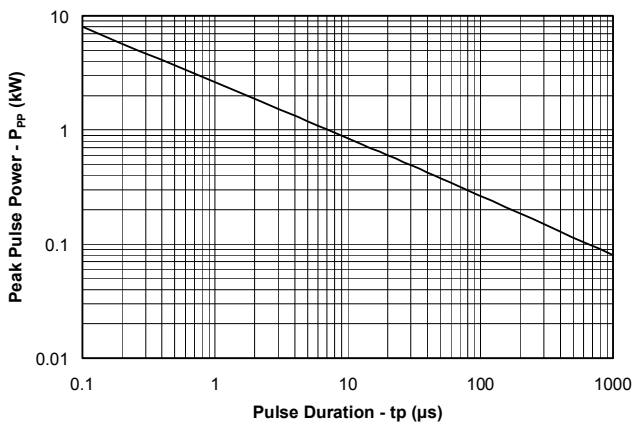
Electrical Characteristics (T=25°C)

SLVU2.8-8						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				2.8	V
Punch-Through Voltage	V_{PT}	$I_{PT} = 2\mu A$	3.0			V
Snap-Back Voltage	V_{SB}	$I_{SB} = 50mA$	2.8			V
Reverse Leakage Current	I_R	$V_{RWM} = 2.8V$, $T=25^\circ C$ (Each Line)		.100	1	μA
Clamping Voltage	V_C	$I_{pp} = 1A$, $t_p = 8/20\mu s$ (Each Line)			4.6	V
Clamping Voltage	V_C	$I_{pp} = 24A$, $t_p = 8/20\mu s$ (Each Line)			15	V
Clamping Voltage	V_C	$I_{pp} = 30A$, $t_p = 8/20\mu s$ (Each Line)			17	V
Maximum Peak Pulse Current	I_{pp}	$t_p = 8/20\mu s$			30	A
Junction Capacitance	C_j	$V_R = 0V$, $f = 1MHz$ (Each Line)			8	pF

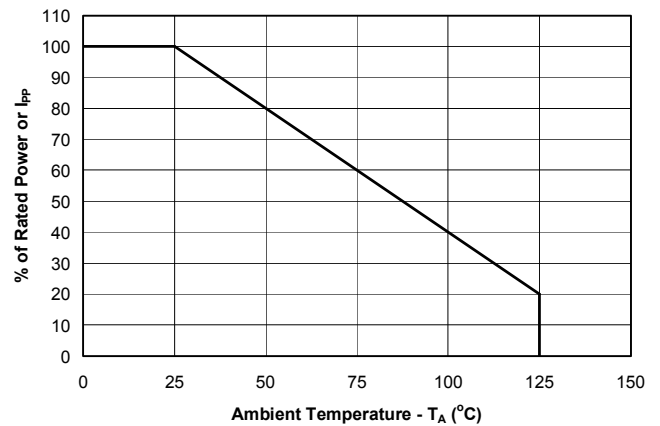
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Typical Characteristics

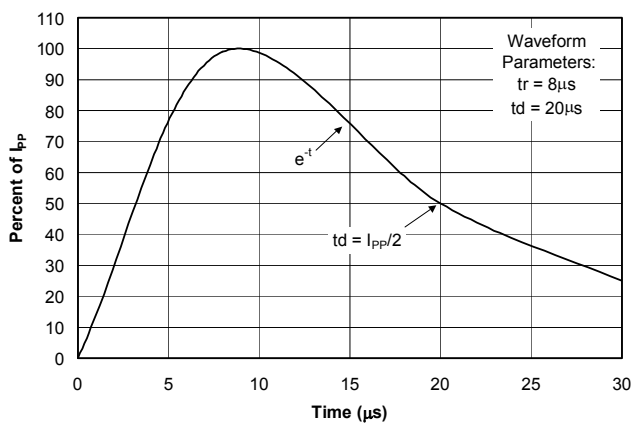
Non-Repetitive Peak Pulse Power vs. Pulse Time



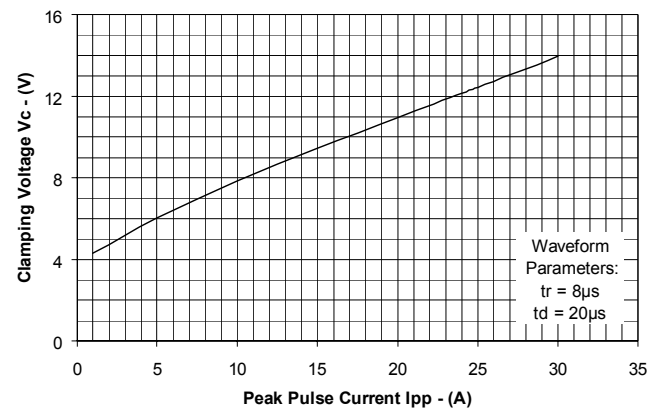
Power Derating Curve



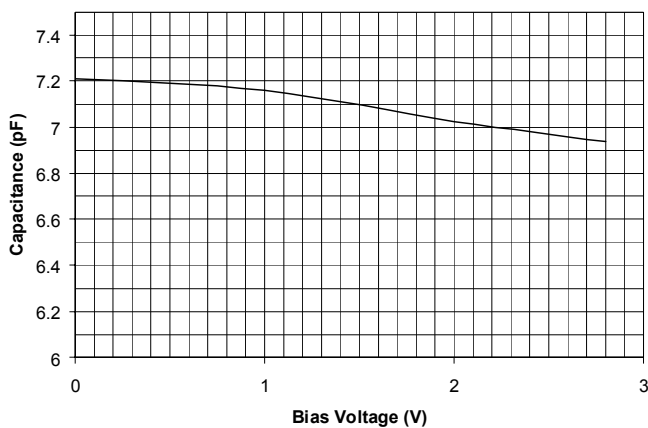
Pulse Waveform



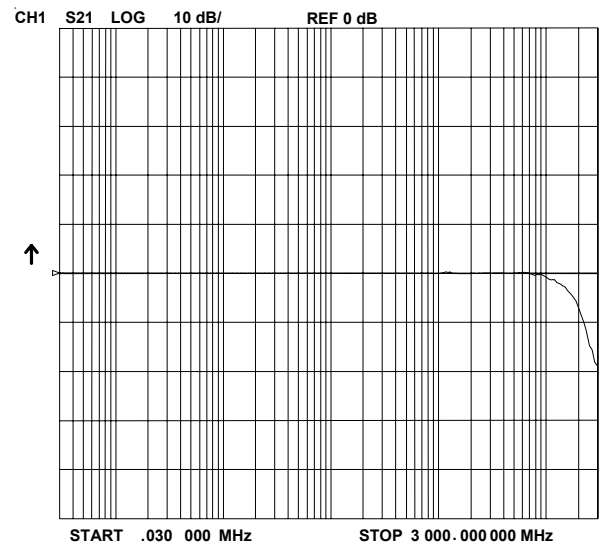
Clamping Voltage vs. Peak Pulse Current



Capacitance vs. Reverse Voltage



Insertion Loss S21



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Applications Information

Device Connection for Protection of Eight Data Lines

Electronic equipment is susceptible to transient disturbances from a variety of sources including: ESD to an open connector or interface, direct or nearby lightning strikes to cables and wires, and charged cables “hot plugged” into I/O ports. The SLVU2.8-8 is designed to protect sensitive components from damage and latch-up which may result from such transient events. The SLVU2.8-8 can be configured to protect four high-speed line pairs differentially, or four lines to ground (common mode). The device is connected as follows:

1. Differential Protection of four line pairs:

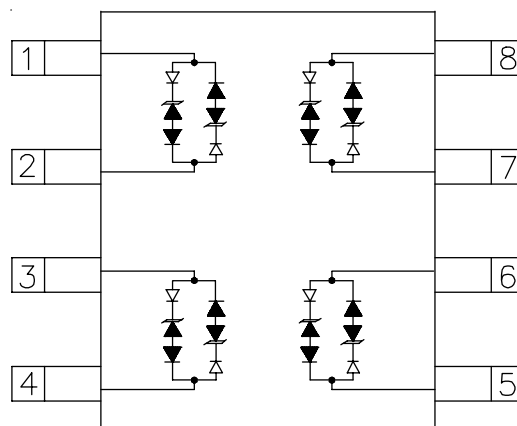
Line pairs are connected at pins 1 and 2, 3 and 4, 5 and 6, and 7 and 8.

Circuit Board Layout Recommendations for Suppression of ESD.

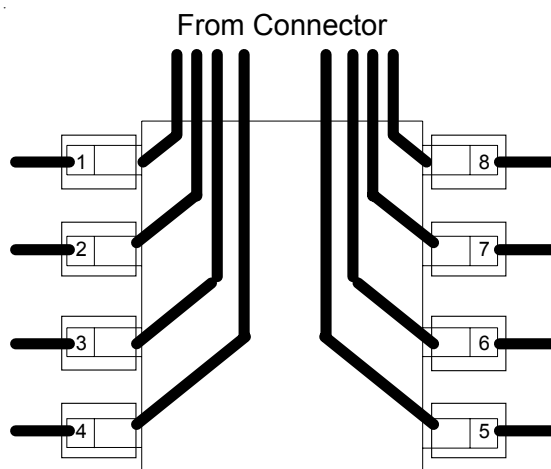
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

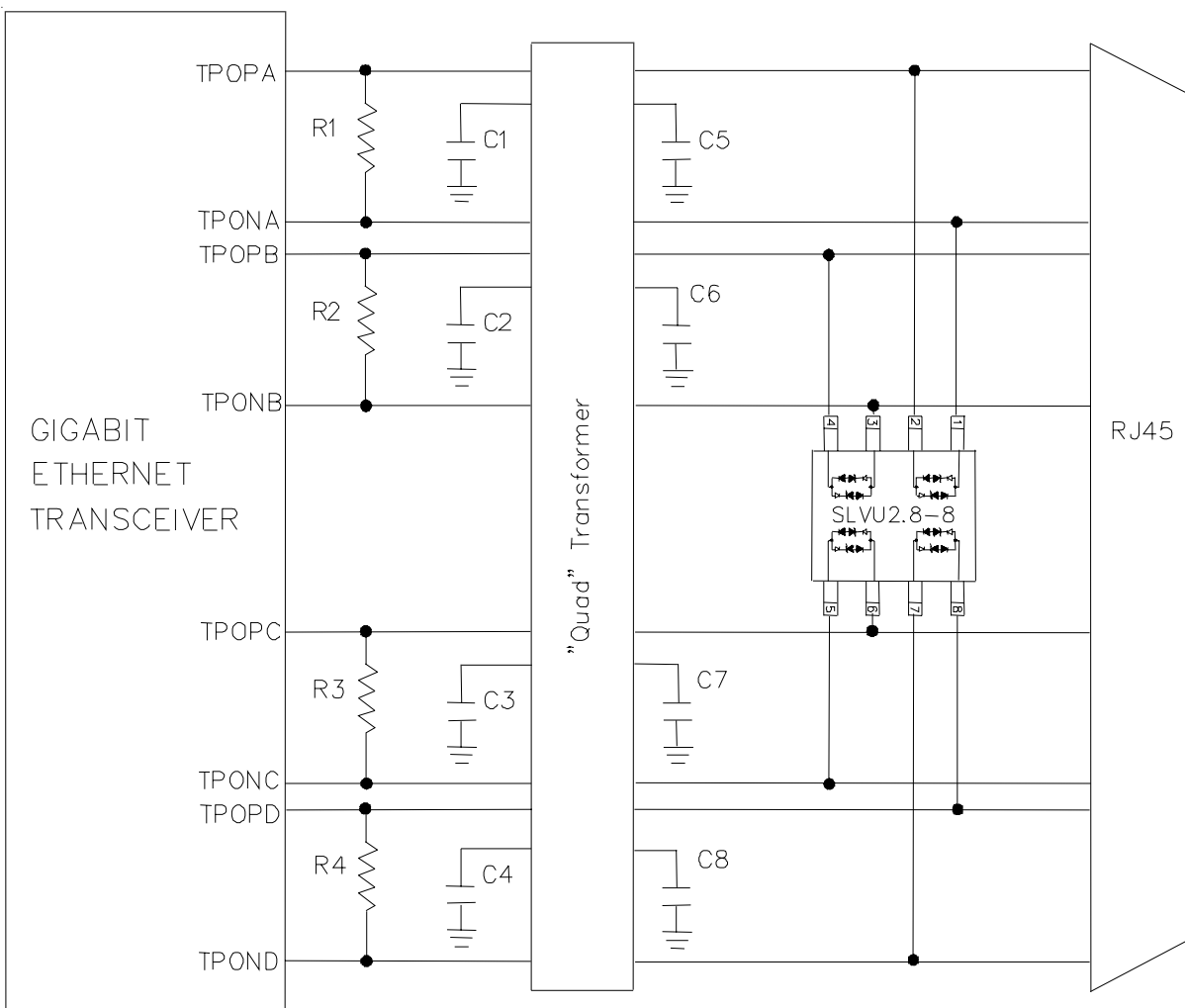
- Place the device near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

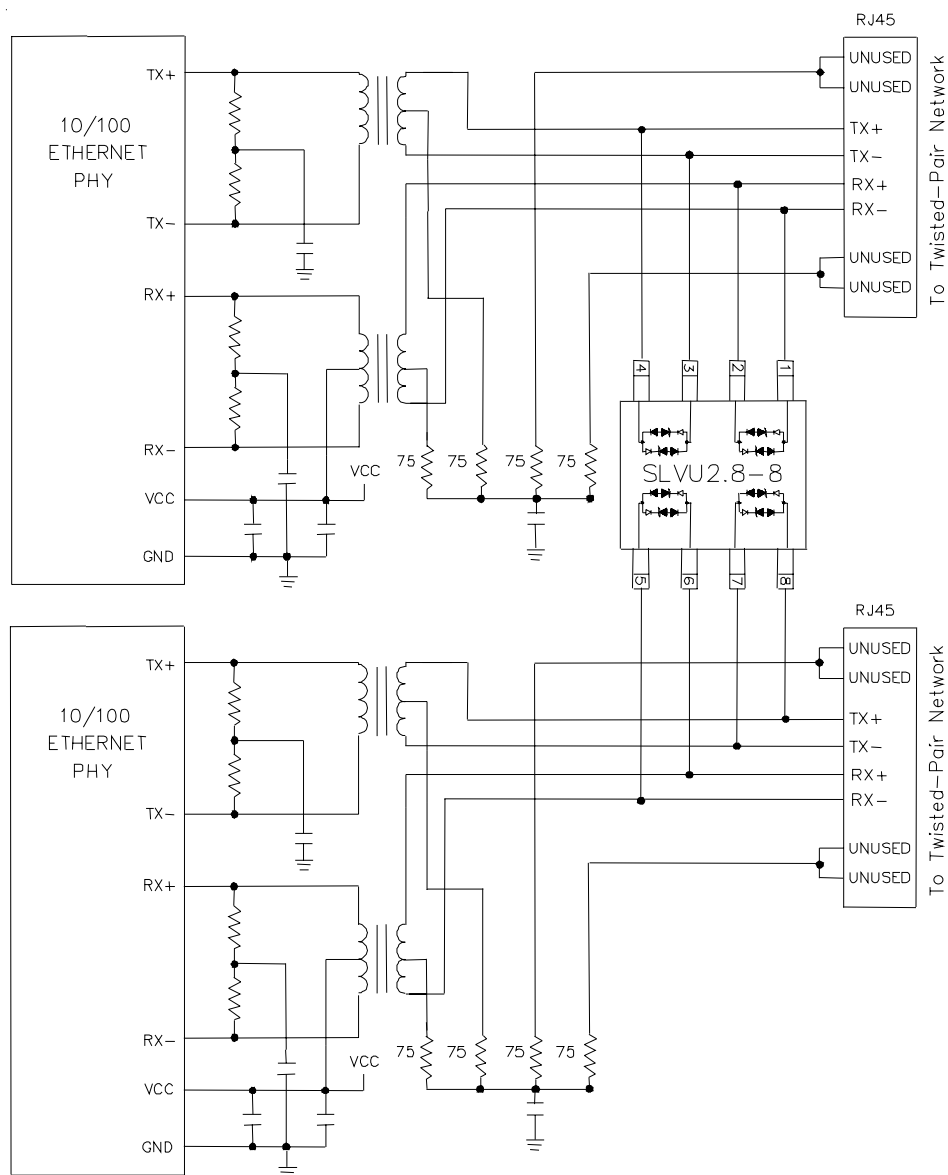
SLVU2.8-8 Circuit Diagram



Differential Protection of Four Line Pairs



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Typical Applications

Gigabit Ethernet Protection Circuit

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Typical Applications


One SLVU2.8-8 Protecting Two 10/100 Ethernet Port

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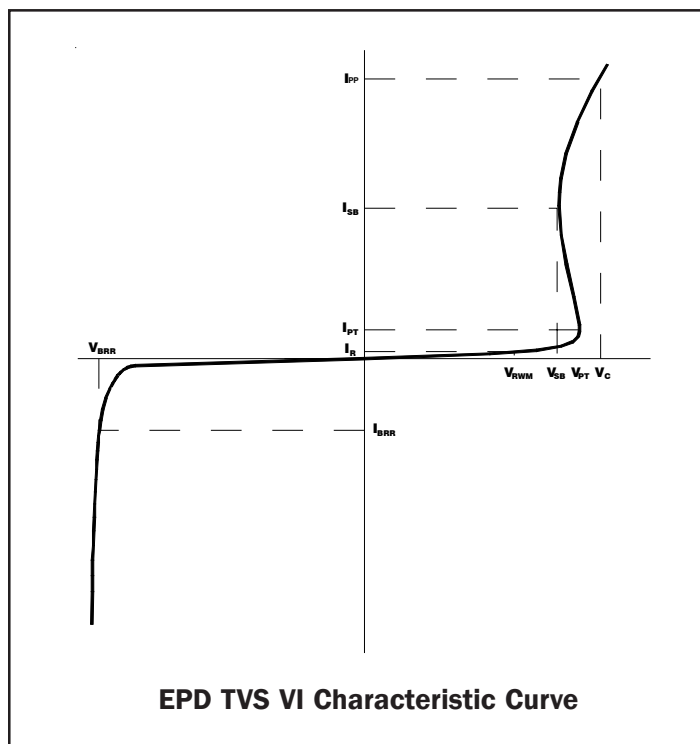
Applications Information (*continued*)

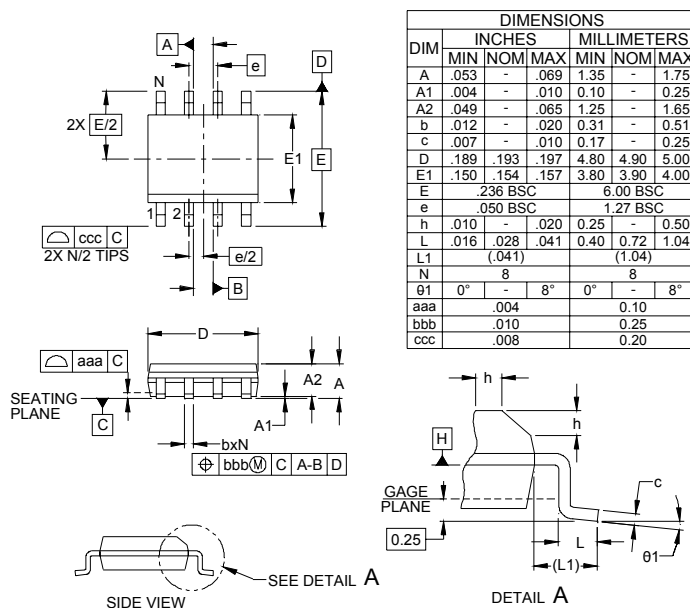
EPD TVS™ Characteristics

The SLVU2.8-8 is constructed using Semtech's proprietary EPD technology. The structure of the EPD TVS is vastly different from the traditional pn-junction devices. At voltages below 5V, high leakage current and junction capacitance render conventional avalanche technology impractical for most applications. However, by utilizing the EPD technology, the SLVU2.8-8 can effectively operate at 2.8V while maintaining excellent electrical characteristics.

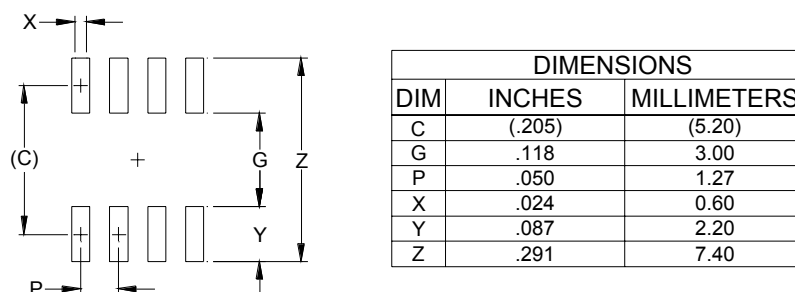
The EPD TVS employs a complex npnp structure in contrast to the pn structure normally found in traditional silicon-avalanche TVS diodes. The EPD mechanism is achieved by engineering the center region of the device such that the reverse biased junction does not avalanche, but will “punch-through” to a conducting state. This structure results in a device with superior dc electrical parameters at low voltages while maintaining the capability to absorb high transient currents.

The IV characteristic curve of the EPD device is shown in Figure 1. The device represents a high impedance to the circuit up to the working voltage (V_{RWM}). During a transient event, the device will begin to conduct as it is biased in the reverse direction. When the punch-through voltage (V_{PT}) is exceeded, the device enters a low impedance state, diverting the transient current away from the protected circuit. When the device is conducting current, it will exhibit a slight “snap-back” or negative resistance characteristic due to its structure. This must be considered when connecting the device to a power supply rail. To return to a non-conducting state, the current through the device must fall below the snap-back current (approximately $< 50\text{mA}$).

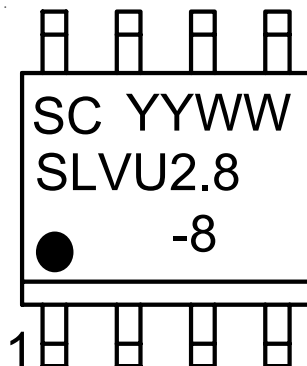


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Outline Drawing - S0-8

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - S0-8

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

PROTECTION PRODUCTS
Marking

Top View

Note:

(1) yyww = Date Code

Ordering Information

Part Number	Working Voltage	Qty/Pkg	Reel Size
SLVU2.8-8.TB	2.8V	500/Reel	7 Inch
SLVU2.8-8.TBT ⁽¹⁾	2.8V	500/Reel	7 Inch
SLVU2.8-8	2.8V	98/Tube	N/A
SLVU2.8-8.T ⁽¹⁾	2.8V	98/Tube	N/A

Note:

(1) Lead-Free Product

Contact Information

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