FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-31101-1E

ASSP for Graphics Control

Graphics Display Controller

MB86290A

■ DESCRIPTION

The MB86290A is a graphics display controller for drawing and displaying graphics on a car navigation system or amusement unit.

The MB86290A can process high-quality, true three-dimensional graphics at high speed using advanced features such as distortion control and hidden surface removal during expression of various levels of transparency and drawing in three-dimensional space. It can also process two-dimensional graphics with a smooth touch, for example, by drawing smooth lines and drawing polygons by connecting arbitrarily specified vertices.

■ FEATURES

- Operating frequency: 100 MHz (External clock of 14.32 MHz Max)
- Host interface: Enables direct connection to a CPU (Hitachi SH3/4 or NEC V832).
- Drawing features:
  - Drawing at a peak rate of 800 Mpixels per second (at an internal operating frequency of 100 MHz)
  - 2D drawing functions: Point, line, triangle, polygon, BLT, and pattern drawing
  - 3D drawing functions: Point, line, and triangle drawing, and hidden surface removal by Z-buffering
  - Special effects: Anti-aliasing, bold/dashed-line processing, alpha blending, Gouraud shading, texture mapping (bilinear filtering, perspective correct), and tiling

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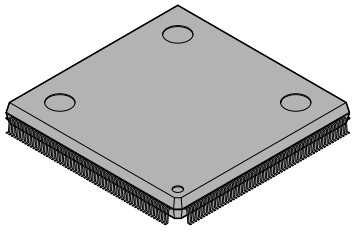
■ PACKAGE

240-pin, Plastic QFP



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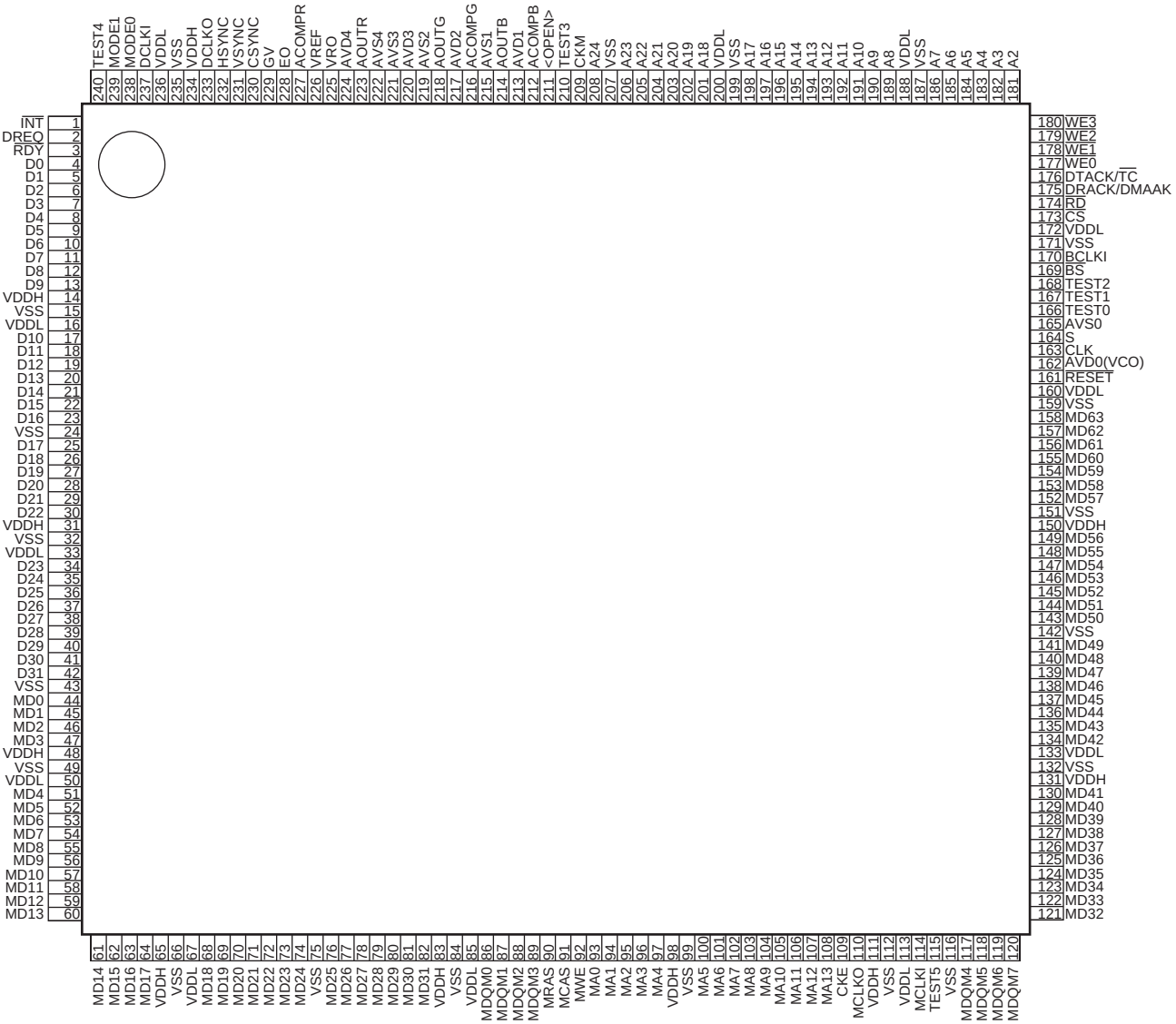
- Display features :
  - Maximum display resolution supported: 1024 x 768 pixels
  - Color display either with a color palette of 8 bits per pixel or directly using 5-bit RGB colors of 16 bits per pixel
  - Overlaying four layers of screen, of which two lower layers can be divided into the left and right parts
  - Supporting two 64x64-pixel hardware cursors
  - Three-channel D/A converter integrated to output analog RGB signals
  - Capable of superimposing using an external synchronization mode
- Memory interface :
  - Using SDRAM as graphics memory at an operating clock speed of 100 MHz and data bus width of 64 bits. Capable of connecting up to 32 Mbytes (offering a throughput of 800 Mbps).
  - Power-supply voltage: Two power supplies at 2.5 V±0.2 V for internal circuits and 3.3 V±0.3 V for I/O parts
  - Package: Plastic QFP with 240 pins (with a lead pitch of 0.5 mm)
  - Power consumption: 1 W (at 100 MHz, V_{DDL} = 2.5 V ± 0.2 V)
  - Process technology: 0.25 µm CMOS

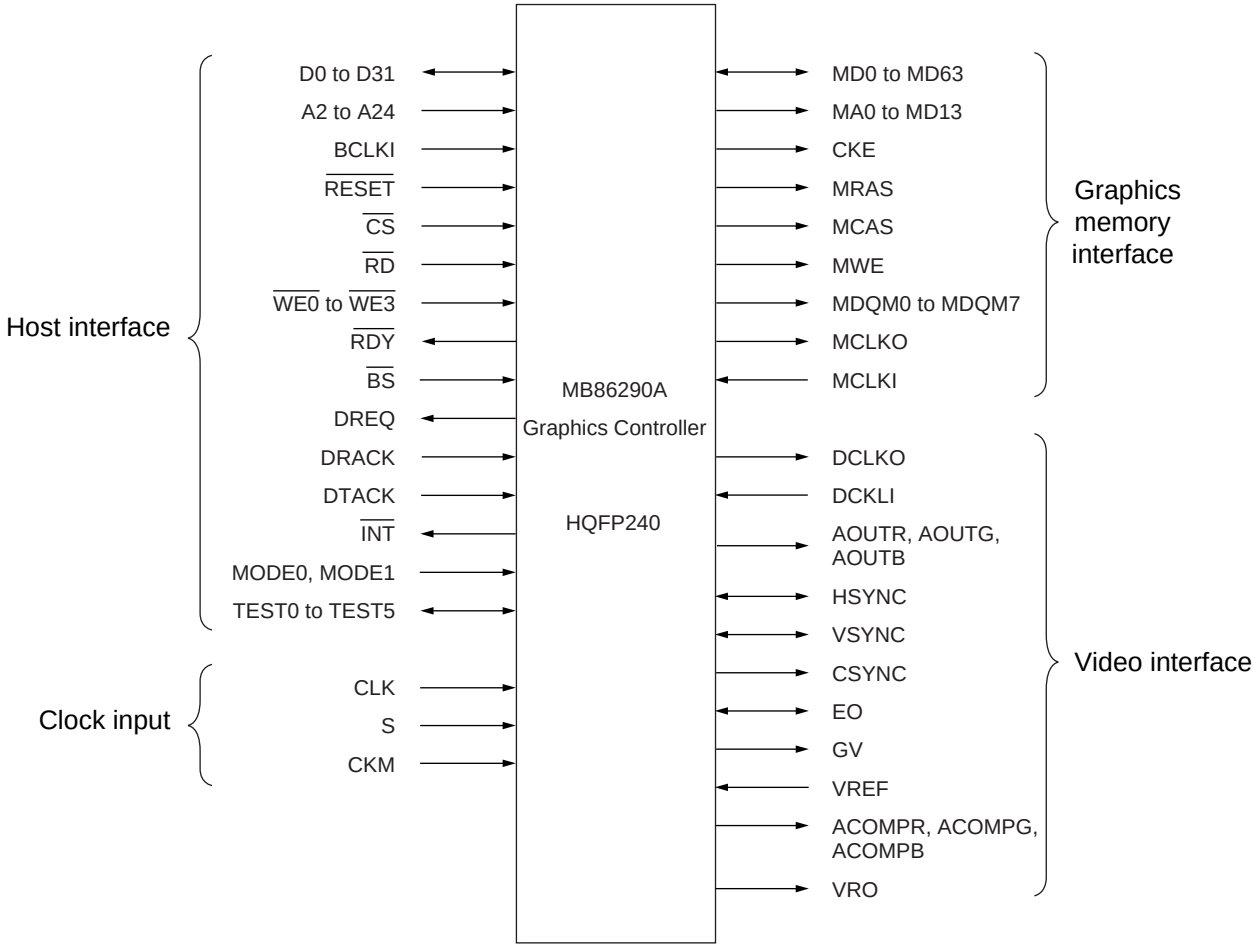
■ PIN ASSIGNMENT

(TOP VIEW)



VSS/AVS : Ground, VDDH : 3.3 V power supply, VDDL : 2.5 V power supply
AVD1 - AVD4 : 2.5 V analog power supply, AVD(VCO) : 2.5 V PLL power supply
Notes : • Leave pin 211 open without making any connection.
• AVD1 - AVD4, AVD(VCO), and /VDDL should be separated on the board.

■ PIN DESCRIPTION



• **Host Interface Pins**

Pin Name	Input/output	Function
MODE0, MODE1	Input	Host CPU mode select
$\overline{\text{RESET}}$	Input	Hardware reset
D0 to D31	Input/Output	Host CPU bus data
A2 to A24	Input	Host CPU bus address (Connect A24 to $\overline{\text{MWR}}$ in V832 mode.)
BCLKI	Input	Host CPU bus clock
$\overline{\text{BS}}$	Input	Bus cycle start signal
$\overline{\text{CS}}$	Input	Chip select signal
$\overline{\text{RD}}$	Input	Read strobe signal
$\overline{\text{WE0}}$	Input	D0 to D7 write strobe signal
$\overline{\text{WE1}}$	Input	D8 to D15 write strobe signal
$\overline{\text{WE2}}$	Input	D16 to D23 write strobe signal
$\overline{\text{WE3}}$	Input	D24 to D31 write strobe signal
$\overline{\text{RDY}}$	Output Tristate	Wait request signal (“0” for wait state with SH3; “1” for wait state with SH4 or V832)
DREQ	Output	DMA request signal (active low with both SH and V832)
DRACK/ DMAAK	Input	InputDMA request acknowledge signal (Connect this to DMAAK in V832 mode. Active high with both SH and V832.)
DTACK/$\overline{\text{TC}}$	Input	DMA transfer strobe signal (Connect this to $\overline{\text{TC}}$ in V832 mode. SH = active high, V832 = active low)
$\overline{\text{INT}}$	Output	Host CPU interrupt signal (SH = active low, V832 = active high)
TEST0 to TEST5	Input	Test signal

Note : The host interface can connect the MB86290A to the SH4 (SH7750) or SH3 (SH7709) manufactured by Hitachi Ltd. or to the V832 manufactured by NEC without any external circuit in between. (Using the SRAM interface allows the MB86290A to use another CPU.) The host CPU is set by the MODE pins as shown below.

MODE1 pin	MODE0 pin	CPU Type
L	L	SH3
L	H	SH4
H	L	V832
H	H	Reserved

Notes :
- The host interface transfers data signals at a fixed width of 32 bits.
- There are 23 lines for address signals handled in double words (32 bits) and 32 Mbytes of address space.
- The external bus can be used at an operating frequency of 100 MHz Max.
- The $\overline{\text{RDY}}$ signal at the low level sets the ready state in the SH4 or V832 mode; the signal at the low level sets the wait state in the SH3 mode. Note that the XRDY signal is a tristate output.
- The host interface supports DMA transfer using an external DMA controller.

- The host interface generates a host processor interrupt signal.
- The $\overline{\text{RESET}}$ pin requires low level input of at least 300 µs after setting “S” (PLL reset signal) to high level.
- Fix the TEST signal at high level.
- In the V832 mode, connect the following pins as specified :

Pin Name	V832 Signal Name
A24	$\overline{\text{MWR}}$
DTACK	$\overline{\text{TC}}$
DRACK	DMAAK

• **Video Interface Pins**

Pin Name	Input/output	Function
DCLKO	Output	Display dot clock signal output
DCLKI	Input	External synchronous dot clock signal input
AOUTR	Analog output	Analog video (R) signal output
AOUTG	Analog output	Analog video (G) signal output
AOUTB	Analog output	Analog video (B) signal output
HSYNC	Input/output*	Horizontal sync signal output Horizontal sync signal input in external synchronization mode
VSYNC	Input/output*	Vertical sync signal output Vertical sync signal input in external synchronization mode
CSYNC	Output	Composite sync signal output
EO	Input/output*	Even/odd-number field identification output Even/odd-number field identification input in external synchronization mode
GV	Output	Graphics/video select signal
VREF	Analog output	Reference voltage input pin
ACOMPR	Analog output	R-signal compensation pin
ACOMPG	Analog output	G-signal compensation pin
ACOMPB	Analog output	B-signal compensation pin
VRO	Analog output	Reference current setting pin

* : Input voltage level : 5 V tolerant

Notes :
- The video interface contains an 8-bit D/A converter to output analog RGB signals.
- Using an additional external circuit, the video interface can use CSYNC signals to generate composite video signals.
- The video interface can output analog RGB signals synchronized with external video signals. The mode for synchronization with the DCLKI signal can be selected as well as the mode for synchronization with a set dot clock as for normal display.
- The HSYNC and VSYNC signals must be pulled up outside the LSI as they enter the input state upon reset.
- Terminate the AOUTR, AOUTG, and AOUTB pins with a resistance of 75 Ω.
- Input 1.1 V to the VREF pin. Between this pin and analog ground, insert a bypass capacitor (one with a superior high-frequency characteristic such as a laminated ceramic capacitor) .
- Connect the ACOMPR, ACOMPG, and ACOMPB pins to the 0.1µF ceramic capacitor ahead of the analog power supply.
- Connect the VRO pin to the analog ground with a 2.7 kΩ resistor.
- The input voltage levels of the HSYNC, VSYNC, and EO signals are 5 V tolerant. Do not input 5 V to these pins with the power supply off. (See ■ ABSOLUTE MAXIMUM RATINGS.)
- For noninterlaced display in external synchronization mode, input “0” to the EO pin, for example, using a pull-down resistor.
- The GV signal serves to switch between graphics and video for chroma keying. The pin outputs a low level signal to select video.

• **Graphics Memory Interface Pins**

Pin Name	Input/output	Function
MD0 to MD63	Input/output	Graphics memory bus data
MA0 to MA13	Output	Graphics memory bus data
CKE	Output	Clock enable
MRAS	Output	Row address strobe
MCAS	Output	Column address strobe
MWE	Output	Write enable
MDQM0 to MDQM7	Output	Data mask
MCLKO	Output	Graphics memory clock output
MCLKI	Input	Graphics memory clock input

Notes :
- The graphics memory interface connects the MB86290A to the external memory used for graphical image data. The interface can directly accept 64 Mbit SDRAM (with a 16-bit or 32-bit data bus) without any external circuit.
- The data signal can be selected between 64 bits and 32 bits. To use the 32-bit signal, leave the MD32 to MD63 and MDQM4 to MDQM7 pins open.
- Connect the MCLKI pin to the MCLKO pin.

• **Clock Input Pins**

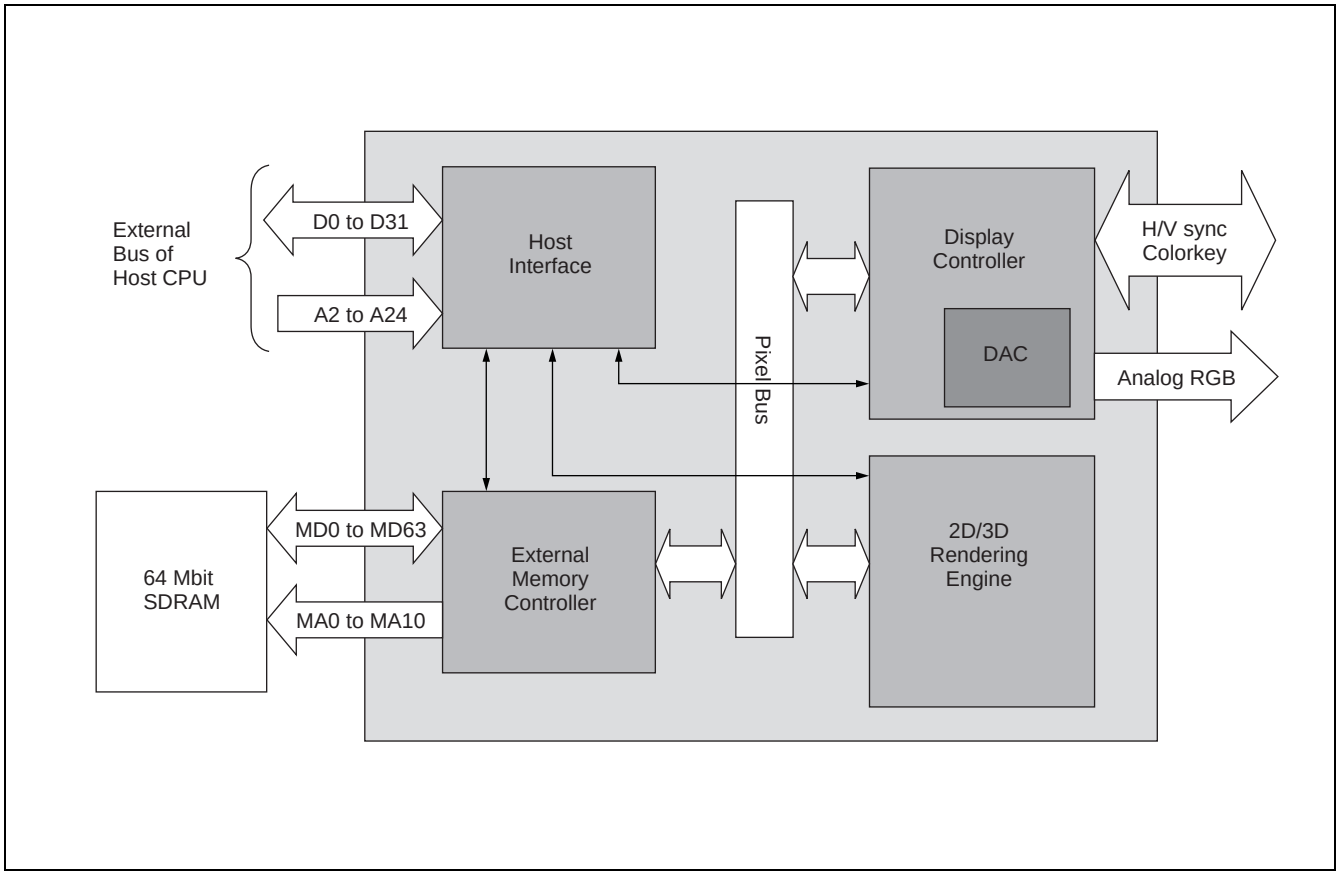
Pin Name	Input/output	Function
CLK	Input	Clock input signal
S	Input	PLL reset signal
CKM	Input	Clock mode signal

Notes :
- The clock input block inputs the clock signal that serves as the basis for the reference clock for the internal operating clock and display dot clock. Usually input 4 Fsc (= 14.31818 MHz) . The internal PLL generates the internal operating clock signal of 100.22726 MHz and the display reference clock signal of 200.45452 MHz.
- The internal operating clock signal to be used can be selected between the clock signal (CLK input multiplied by 7) generated by the internal PLL and the bus clock BCLKI input to the host CPU interface. Select the BCLKI input to use the host CPU bus at 100 MHz.

CKM	Clock Mode
L	Select internal PLL output.
H	Select host CPU bus clock (BCLKI) .

Note : Immediately after turning the power supply on, input a pulse whose low level period is 500 ns or more to the S pin before setting it to high level. After the S signal goes high, input the $\overline{\text{RESET}}$ signal at low level for 300 μs or more.

■ BLOCK DIAGRAM



■ FUNCTION BLOCKS

• Host Interface

This block allows the MB86290A to be connected to the SH3 or SH4 microprocessor manufactured by Hitachi Ltd. without any external circuit in between. The block provides an interface to transfer display list and texture pattern data directly from main memory to the CREMSON graphics memory or internal register using the external DMA controller.

• External Memory Controller

This block controls the external synchronous DRAM connected as graphics memory. The 64-bit or 32-bit data bus is selected and the maximum operating frequency is 100 MHz.

• Display Controller

This block contains a three-channel D/A converter supporting XGA (1024x768 pixels) display and outputs analog RGB signals. The block enables superimposing using the external synchronization mode. It can divide the screen into the left and right parts to display different contents and to scroll them separately. It can also display animations smoothly using double buffering. In addition, it can overlay up to four screens, where the image color blending function can be used to display maps through the console screen as a transparency.

• 2D/3D Rendering Engine

This block draws images in two or three dimensions.

- 2D drawing
  The block provides the anti-aliasing and alpha blending functions to display high-quality images even on a low-resolution LCD.

- 3D drawing
  The block provides true 3D drawing functions such as perspective texture mapping and Gouraud shading.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power-supply voltage	V_{DDL}*1	− 0.5	+ 3.0	V
	V_{DDH}	− 0.5	+ 4.0	V
Input voltage	V_I		V_{DDH} + 0.5 (< 4.0)	V
	V_{IV}*2	− 0.5	V_{DDH} + 4.0 (< 6.0)	
Output current	I_O	− 13	+ 13	mA
Power pin current	I_{POW}	—	60	mA
Ambient operating temperature	T_A	0	70	°C
		− 40*3	+ 85*3	
Ambient storage temperature	Tstg	− 55	+ 125	°C

*1 : The analog and PLL power supplies are included.

*2 : The HSYNC, VSYNC, and EO signals are input.

*3 : Model supporting a wider range of temperatures

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power-supply voltage	V_{DDL}*1	2.3	2.5	2.7	V
	V_{DDL}*2	2.6*6			
	V_{DDH}	3.0	3.3	3.6	
		3.5*6			
Input voltage (High level)	V_{IH}	2.0	—	V_{DDH} + 0.3	V
	V_{IHV}*3	2.0	—	5.5	
Input voltage (Low level)	V_{IL}	− 0.3	—	+ 0.8	V
	V_{ILV}*3	− 0.3	—	+ 0.8	
VREF pin input voltage	V_{REF}	1.05	1.10	1.15	V
VRO pin external resistor	R_{VRO}	—	2.7	—	kΩ
AOUT pin external resistor*4	R_{AOUT}	—	75	—	Ω
ACOMP pin external capacitor*5	C_{ACOMP}	—	0.1	—	μF
Ambient operating temperature	T_A	− 40	—	+ 85	°C
				+ 70*6	

*1 : The analog and PLL power supplies are included.

*2 : The HSYNC, VSYNC, and EO signals are input.

*3 : AOUTR, AOUTG, and AOUTB pins

*4 : AOUTR, AOUTG, AOUTB pins

*5 : ACOMPR, ACOMPG, ACOMPB pins

*6 : Using BCLKI at 90 MHz or more

Notes :
- The VDDL and VDDH power supplies can be turned on or off in either order. Note, however, that the VDDH voltage must not be applied alone continuously for several seconds.
- Do not input the HSYNC, VSYNC or signal with the power-supply voltage not applied. (See “Input voltage” in “■ ABSOLUTE MAXIMUM RATINGS”.)
- After turning the power on, input a pulse remaining at low level for at least 500 ns to the S pin. Then, set the S pin to high level and input the $\overline{\text{RESET}}$ signal held at low level for at least 300 μs.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DDL} = 2.5 V ± 0.2 V, V_{DDH} = 3.3 V ± 0.3, V_{SS} = 0.0 V, T_A = 0 °C to +70 °C)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Output voltage (High level) *1		V_{OH}	V_{DDH} – 0.2	—	V_{DDH}	V
Output voltage (Low level) *2		V_{OL}	0.0	—	0.2	V
Output current (High level)		I_{OH1}*3	– 2.0	—	—	mA
		I_{OH2}*4	– 4.0	—	—	
		I_{OH3}*5	– 8.0	—	—	
Output current (Low level)		I_{OL1}*3	2.0	—	—	mA
		I_{OL2}*4	4.0	—	—	
		I_{OL3}*5	8.0	—	—	
AOUT voltage*6	Full scale	I_{AOUT}	9.90	10.42	10.94	mA
	Zero scale		0	2	20	µA
AOUT voltage*7		V_{AOUT}	– 0.1	—	+ 1.1	V
Input leakage current		I_L	—	—	± 5	µA
Pin capacitance		C	—	—	16	pF

*1 : Value when –100 µA current flows into output pins.

*2 : Value when 100 µA current flows into output pins.

*3 : Output characteristics of the MD0 to MD63, MDQM0 to MDQM7 pins

*4 : Output characteristics of the signals (excluding analog signals) other than those in *3 and *5

*5 : MCLKO pin output characteristics

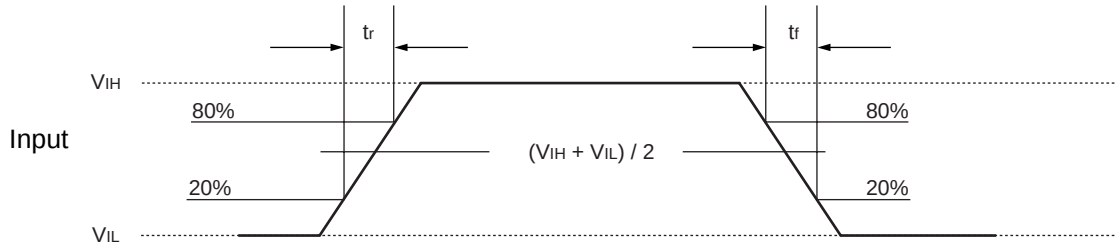
*6 : AOUTR, AOUTG, and AOUTB pin output current. Conditions V_{REF} = 1.10 V, R_{VRO} = 2.7 kΩ
(The full-scale output current calculation expression is (V_{REF} / R_{VRO}) × 25.575)

*7 : AOUTR, AOUTG and AOUTB pins

2. AC Characteristics

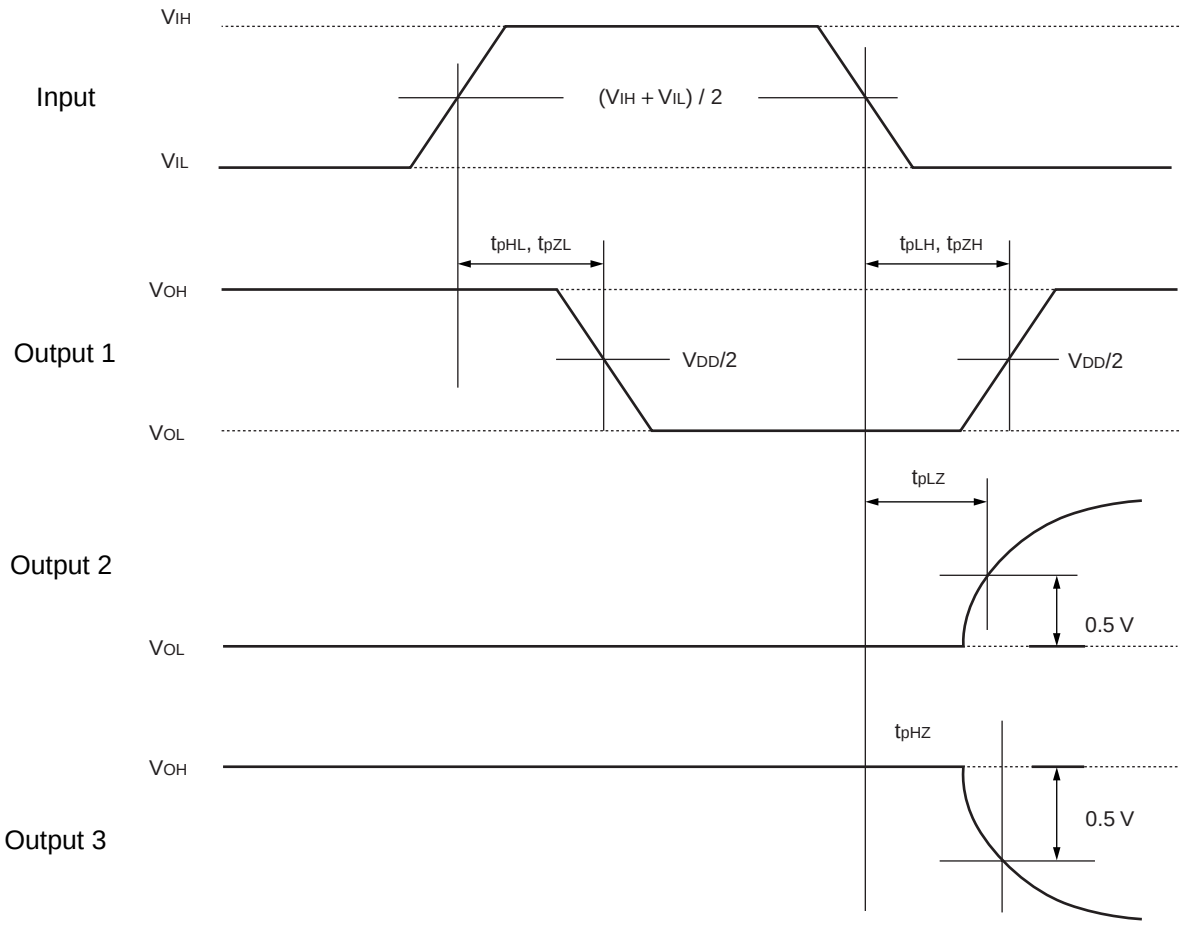
(V_{IH} = 2.0 V, V_{IL} = 0.8 V)

• Input measurement conditions



• t_r, t_f ≤ 5 ns
• Input measurement standard : (V_{IH} + V_{IL}) / 2

• Output measurement conditions



• Output measurement standard : t_{pLZ} : V_{OL} + 0.5 V
t_{pHZ} : V_{OH} – 0.5 V
Else : V_{DD}/2

(1) Host Interface

• Clock

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
BCLKI frequency	f_{BCLKI}	—	—	100	MHz
BCLKI H period	t_{HBCLKI}	—	3.5	—	ns
BCLKI L period	t_{LBCLKI}	—	3.5	—	ns

• Host interface signals

(Recommended operating conditions A, External load of 20 pF)

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Address setup time	t_{ADS}	—	3.0	—	ns
Address hold time	t_{ADH}	—	1.0	—	ns
$\overline{BS}$ setup time	t_{BSS}	—	3.5	—	ns
			3.0*3		
$\overline{BS}$ hold time	t_{BSH}	—	0.0	—	ns
$\overline{CS}$ setup time	t_{CSS}	—	3.5	—	ns
			3.0*3		
$\overline{CS}$ hold time	t_{CSH}	—	0.0	—	ns
$\overline{RD}$ setup time	t_{RDS}	—	3.0	—	ns
$\overline{RD}$ hold time	t_{RDH}	—	1.0	—	ns
$\overline{WE}$ setup time	t_{WES}	—	3.0	—	ns
$\overline{WE}$ hold time	t_{WEH}	—	1.0	—	ns
Write data setup time	t_{WDS}	—	5.0	—	ns
			4.0*3		
Write data hold time	t_{WDH}	—	1.0	—	ns
DTACK setup time	t_{DAKS}	—	3.0	—	ns
DTACK hold time	t_{DAKH}	—	1.0	—	ns
DRACK setup time	t_{DRKS}	—	3.0	—	ns
DRACK hold time	t_{DRKH}	—	1.0	—	ns
Read data delay time (to $\overline{RD}$)	t_{RDDZ}	—	4.0	8.5	ns
			—	7.5*3	ns
Read data delay time	t_{RDD}	*1	4.0	9.5	ns
			—	6.0*3	ns
$\overline{RDY}$ delay time (to $\overline{CS}$) SH	t_{RDYDZ}	—	3.0	9.0	ns
			—	7.5*3	ns

(Continued)

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Parameter	Symbol	Condition	Value		Unit
			Min	Max	
$\overline{RDY}$ delay time (to $\overline{CS}$) V832	t_{RDYDZ}	—	3.0	13.0	ns
			—	10.5*3	ns
$\overline{RDY}$ delay time	t_{RDYD}	—	3.5	8.5	ns
			—	7.0*3	ns
DREQ delay time	t_{DRQD}	—	3.5	7.5	ns
			—	6.5*3	ns
MODE hold time	t_{MODH}	*2	—	20.0	ns

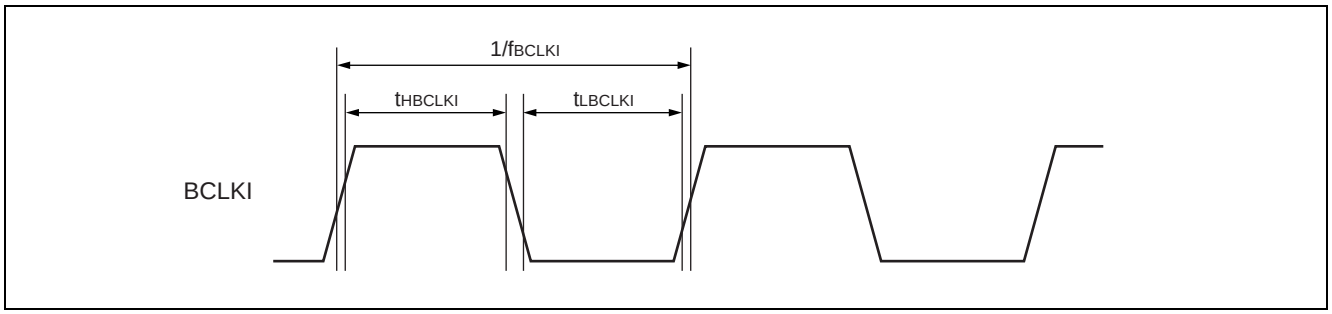
*1 : Read data is output one cycle before the CPU samples it.

*2 : Hold time for reset cancellation

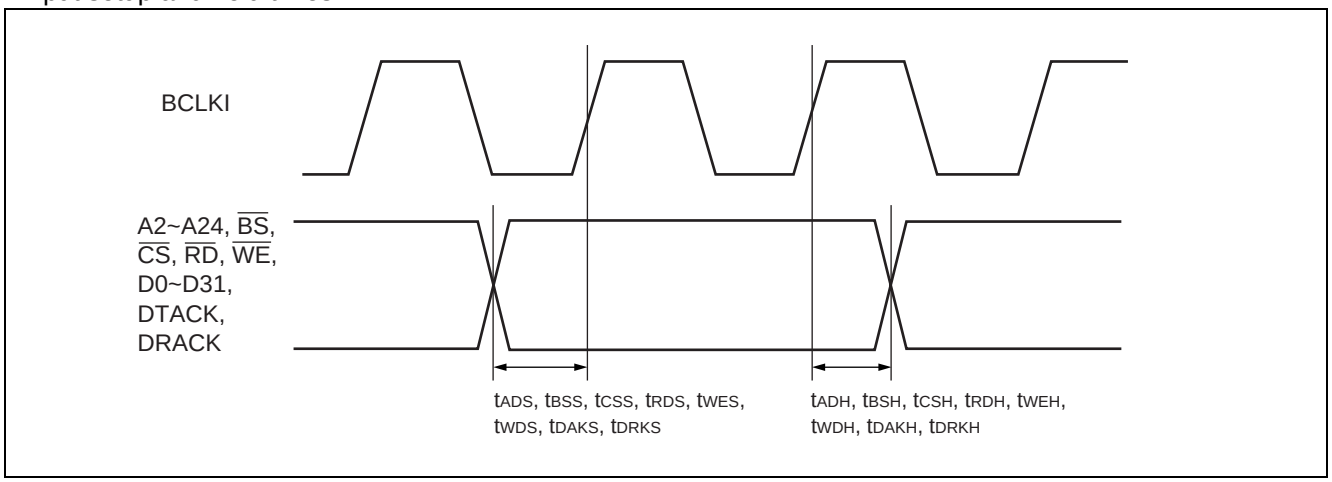
*3 : Using BCLKI at 90 MHz or more

Note: The $\overline{INT}$ signal is output in synchronization with the internal operating clock. As a host interface signal, it is an asynchronous signal.

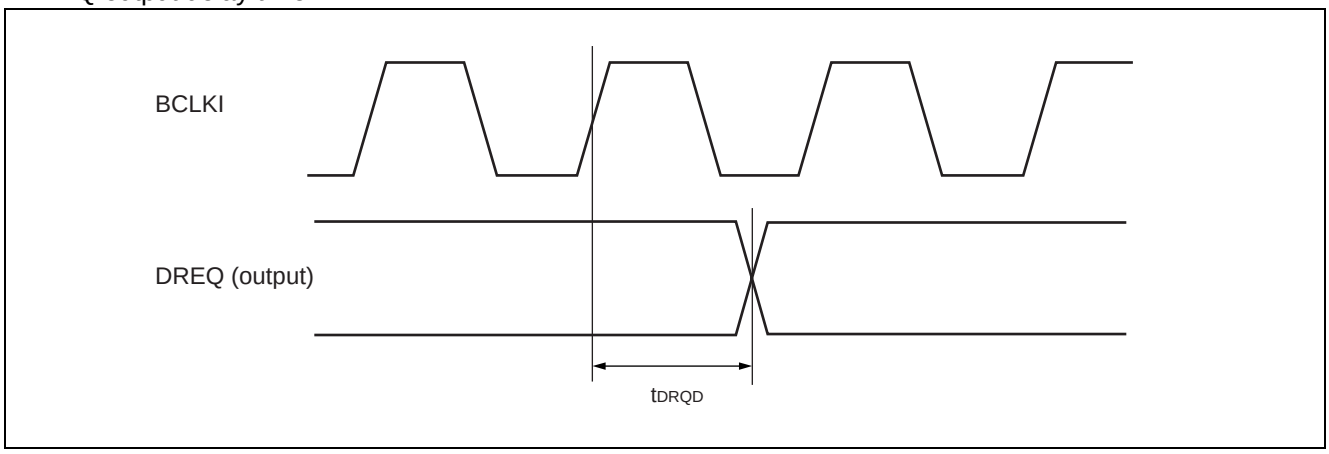
• Clock



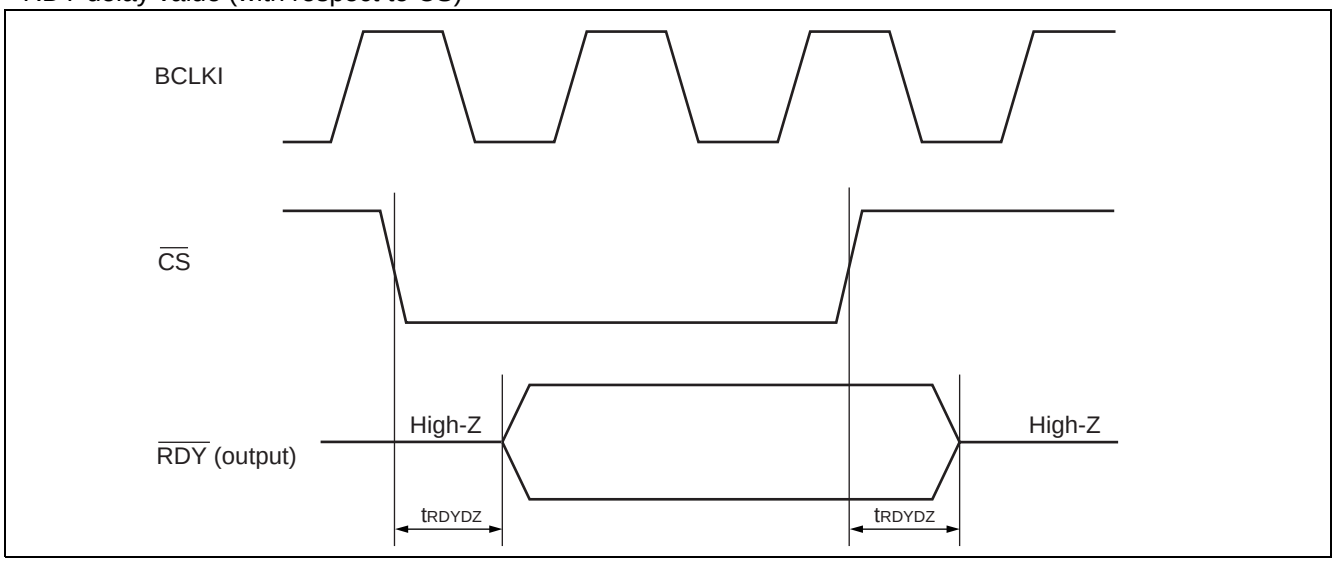
• Input setup and hold times



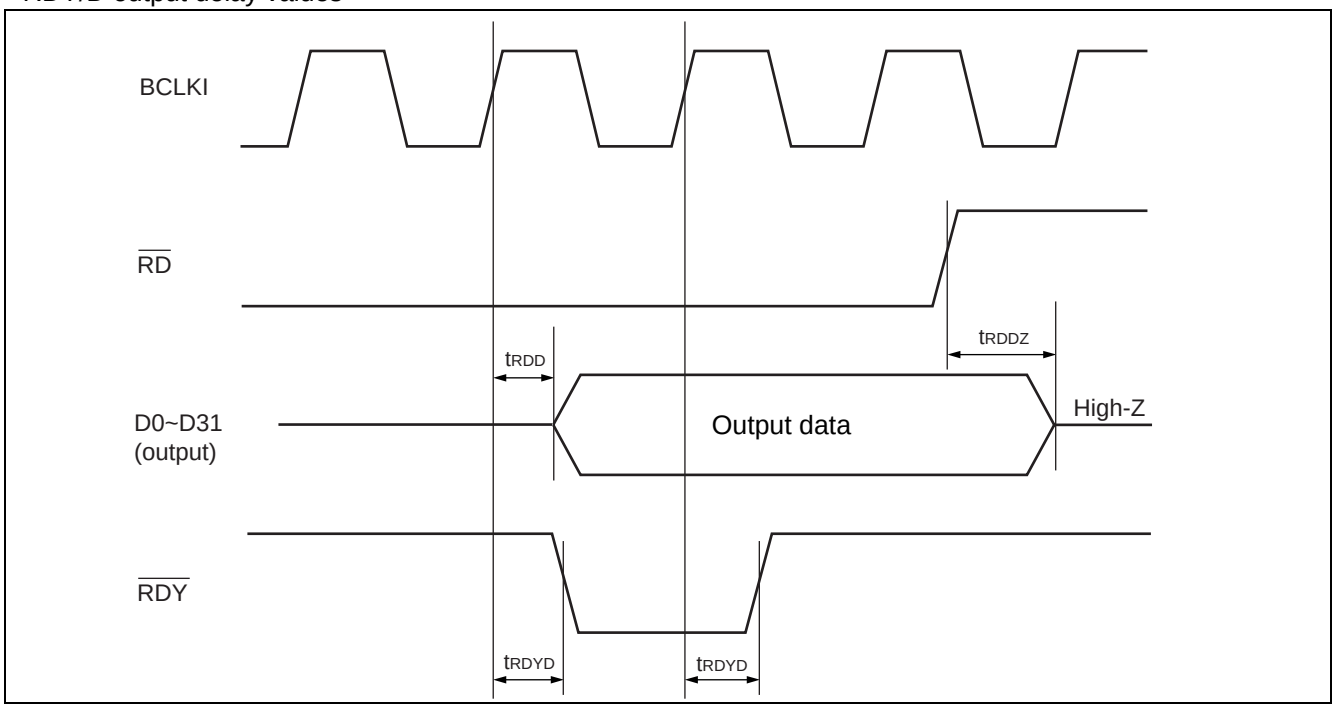
• DREQ output delay time



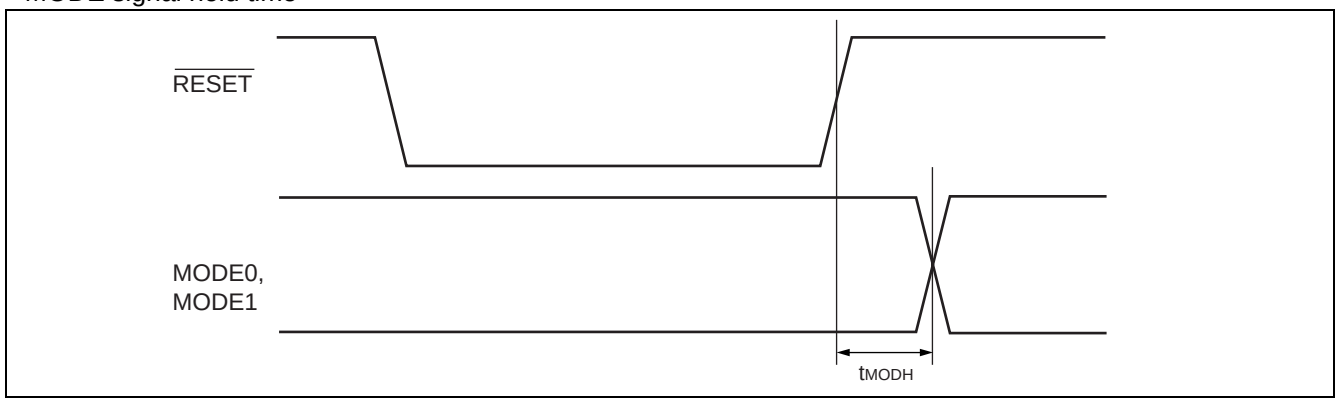
• $\overline{RDY}$ delay value (with respect to $\overline{CS}$)



• $\overline{RDY}$/D output delay values



• MODE signal hold time



(2) Video Interface

• Clock

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
CLK frequency	f_{CLK}	—	—	14.32	—	MHz
CLK H period	t_{HCLK}	—	25	—	—	ns
CLK L period	t_{LCLK}	—	25	—	—	ns
DCLKI frequency	f_{DCLKI}	—	—	—	67	MHz
DCLKI H period	t_{HDCLKI}	—	5	—	—	ns
DCLKI L period	t_{LDCLKI}	—	5	—	—	ns
DCLKO frequency	f_{DCLKO}	—	—	—	67	MHz

• Input signals

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
HSYNC input pulse width	$t_{WHSYNC0}$	*1	3	—	—	clock
	$t_{WHSYNC1}$	*2	3	—	—	clock
HSYNC input setup time	t_{SHSYNC}	*2	10	—	—	ns
HSYNC input hold time	t_{HHSYNC}	*2	10	—	—	ns
VSYNC input pulse width	$t_{WHSYNC1}$	—	1	—	—	HSYNC 1 cycle
EO input setup time	t_{SEO}	*3	10	—	—	ns
EO input hold time	t_{HEO}	*3	10	—	—	ns

*1 : Applied only in PLL synchronization mode (CKS = 0) . The reference clock is the internal PLL's output with Cycle = 1/ (14 f_{CLK}) .

*2 : Applied only in DCLKI synchronization mode (CKS = 1) . The reference clock is DCLKI.

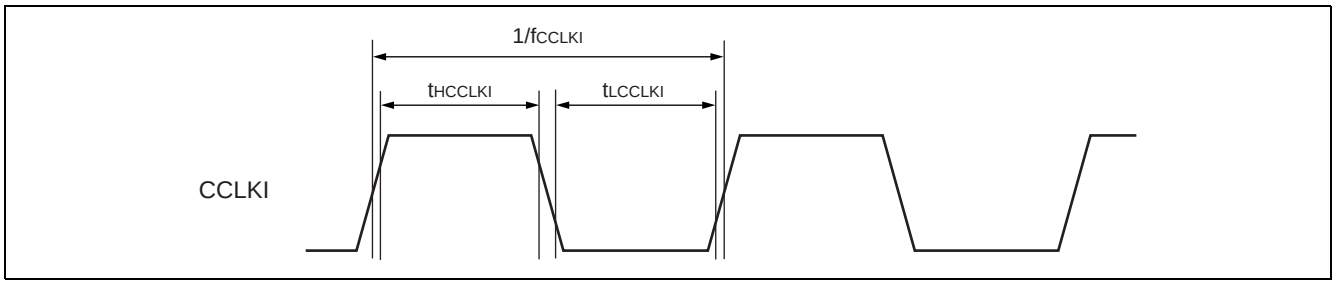
*3 : Based on the edge with VSYNC negated.

• Output signals

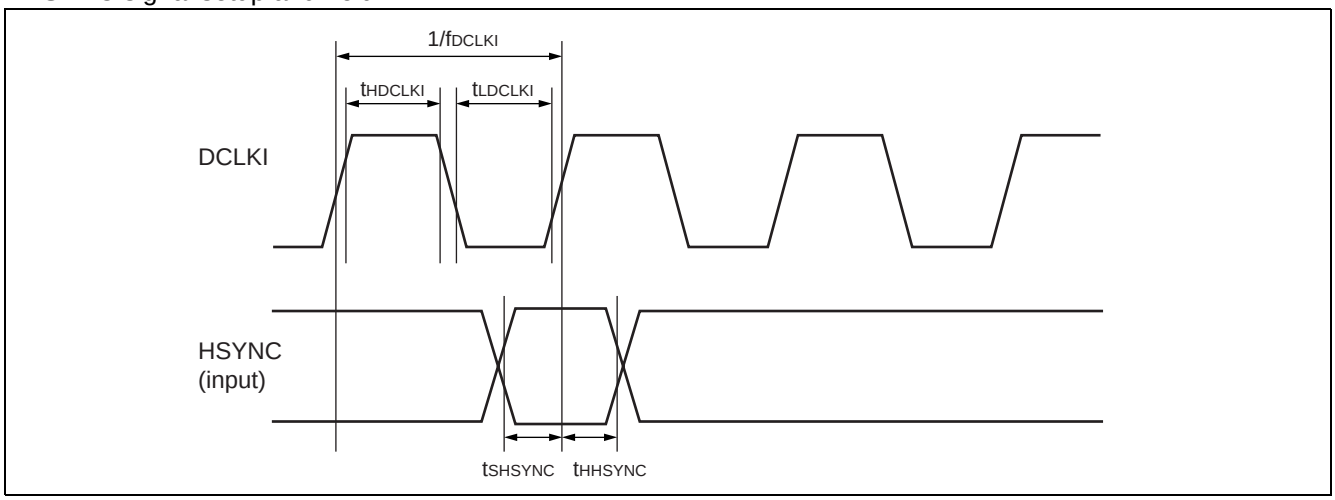
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
EO output delay time	t_{DEO}	*	—	—	10	ns
HSYNC output delay time	t_{DHSYNC}	—	—	—	10	ns
VSYNC output delay time	t_{DVSYNC}	—	—	—	10	ns
CSYNC output delay time	t_{DCSYNC}	—	—	—	10	ns
GV output delay time	t_{DGV}	—	—	—	10	ns

* : The EO output varies at the same time as VSYNC is asserted.

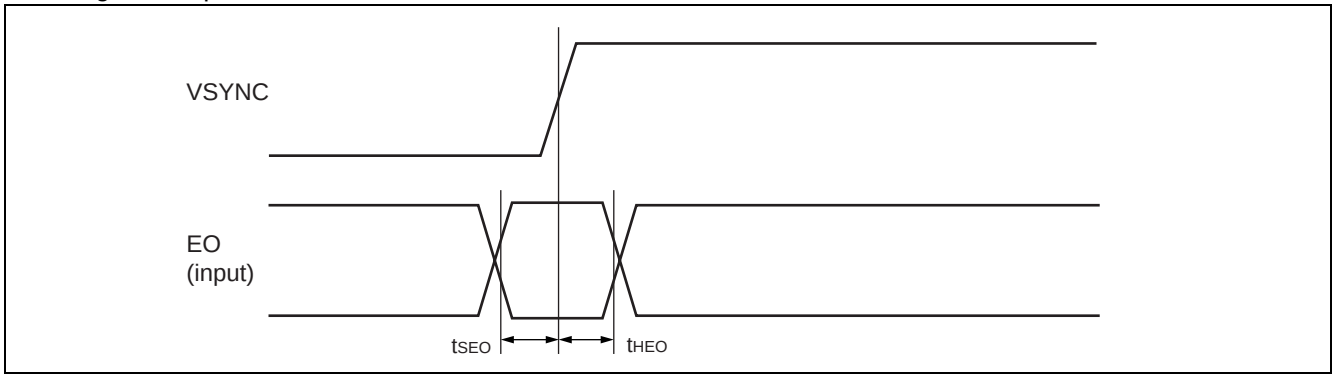
• Clock



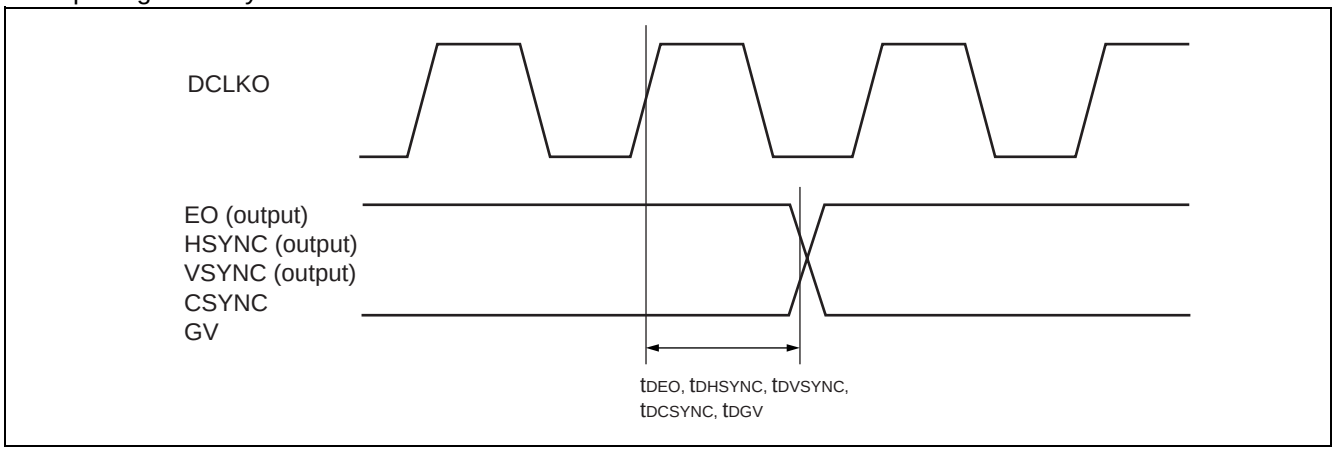
• HSYNC signal setup and hold



• EO signal setup and hold



• Output signal delay



(3) Graphics Memory Interface

• Clock

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
MCLKO frequency	f_{MCLKO}	—	—	—	100	MHz
MCLKO H period	t_{HMCLKO}	—	1	—	—	ns
MCLKO L period	t_{LMCLKO}	—	1	—	—	ns
MCLKI frequency	f_{MCLKI}	—	—	—	100	MHz
MCLKI H period	t_{HMCLKI}	—	1	—	—	ns
MCLKI L period	t_{LMCLKI}	—	1	—	—	ns
MCLKI delay to MCLKO	t_{OID}	—	1	—	4	ns

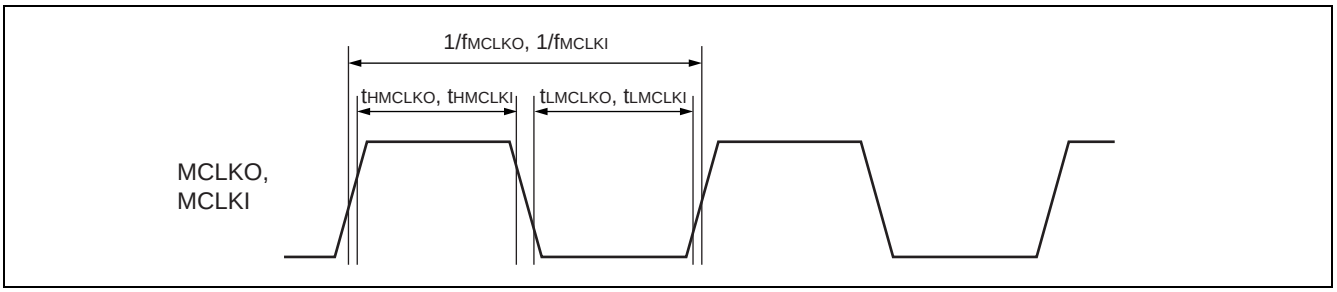
• I/O signals

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
MA, MRAS, MCAS, MWE, CKE Setup time	t_{MADS}	*1	3.5	—	—	ns
MA, MRAS, MCAS, MWE, CKE Hold time	t_{MADH}	*1	1	—	—	ns
MDQM data setup time	t_{MDQMDS}	*1	3.5	—	—	ns
MDQM data hold time	t_{MDQMDH}	*1	1	—	—	ns
MD output data setup time	t_{MDODS}	*1	3.5	—	—	ns
MD output data hold time	t_{MDODH}	*1	1	—	—	ns
MD input data setup time	t_{MDIDS}	*2	3	—	—	ns
MD input data hold time	t_{MDIDH}	*2	1	—	—	ns

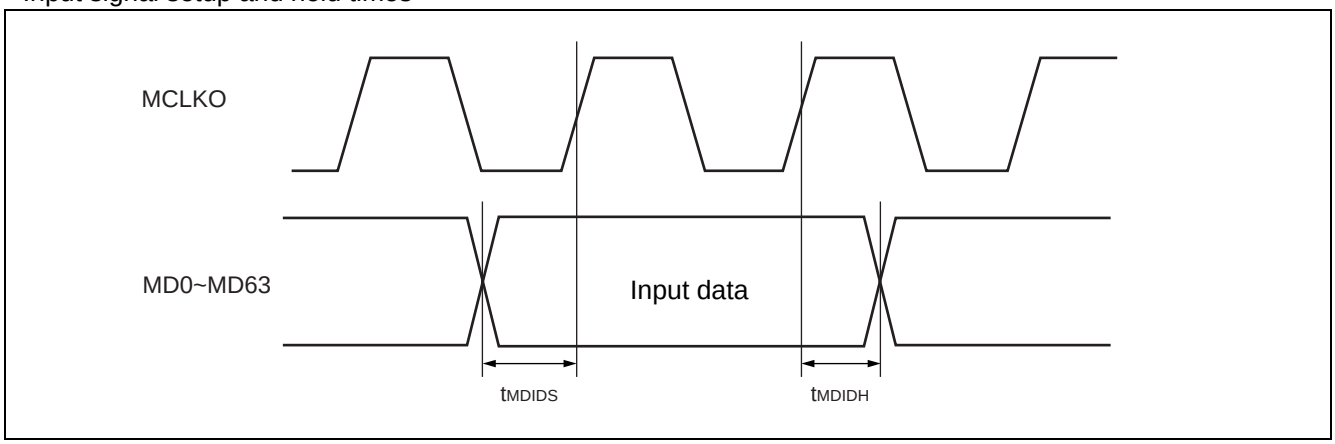
*1 : Setup/hold time with respect to MCLKO.

*2 : Setup/hold time with respect to MCLKI.

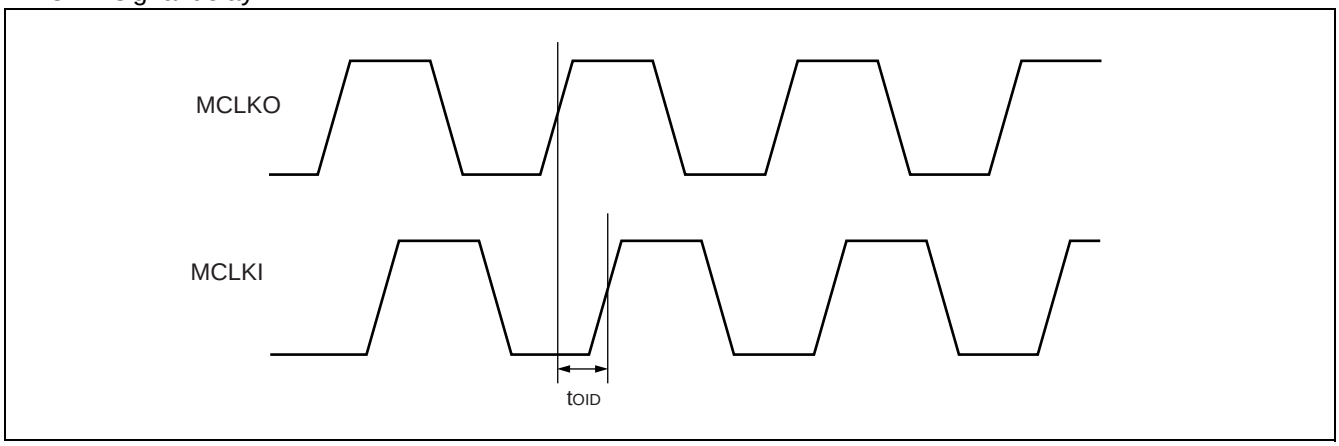
• Clock



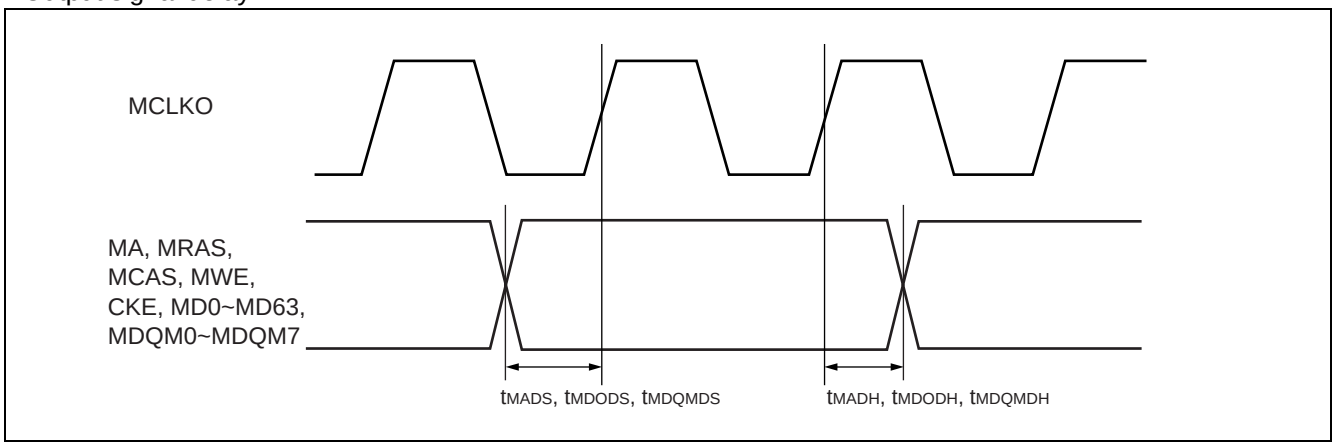
• Input signal setup and hold times



• MCLKI signal delay



• Output signal delay



(4) PLL Standards

Parameter	Value			Unit	Description
	Min	Typ	Max		
Input frequency (Typical)	—	14.31818	—	MHz	
Output frequency	—	—	200.45452	MHz	Multiplied by 14
Duty ratio	93.1	—	101.3	%	PLL output clock H/L pulse width ratio
Jitter	− 150	—	+ 180	ps	Cycle difference between two consecutive cycles

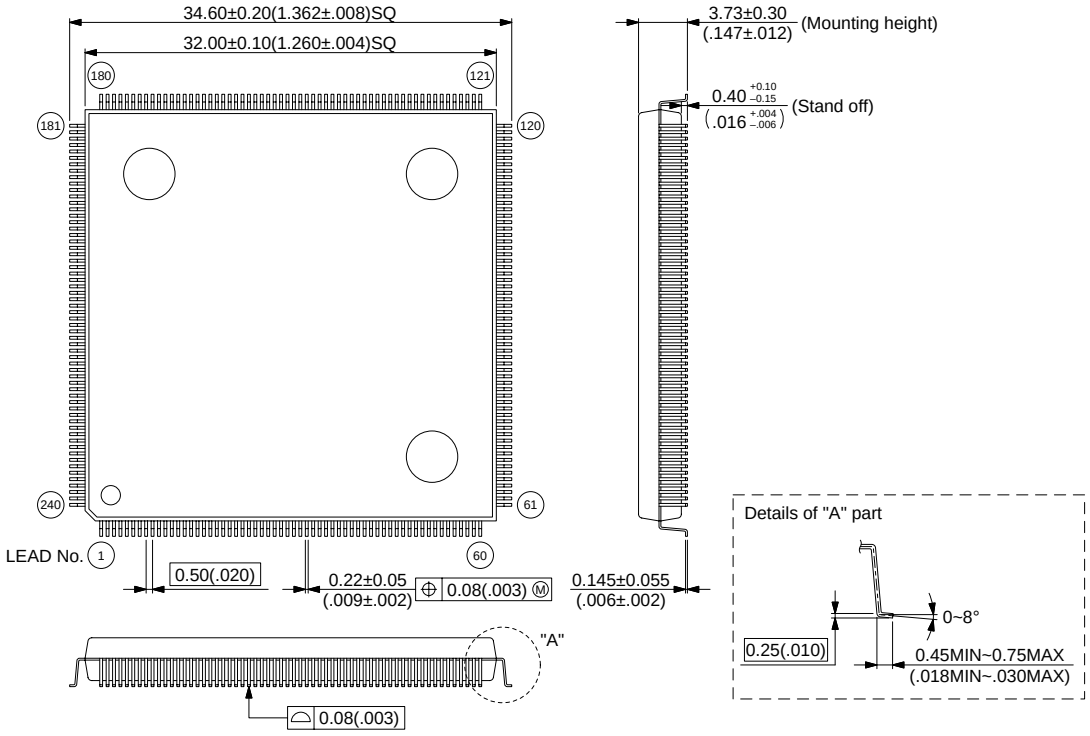
■ ORDERING INFORMATION

Part Number	Package	Remarks
MB86290APFVS	240-pin plastic QFP (FPT-240P-M03)	

■ PACKAGE DIMENSION

240-pin plastic QFP
(FPT-240P-M03)

*Pins width and pins thickness include plating thickness.



Dimensions in mm (inches)

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