



DESCRIPTION

The voltage-sensing input comparators are identical and can be used with threshold levels from zero volts to ($V_{IN} - 3V$). Each has approximately 25mv of hysteresis which is offset so the switching differential threshold is zero on the non-inverting input for rising levels and zero on the inverting input for falling signals. All other operating characteristics are as described in the SG1543 data sheet and application note.

FEATURES

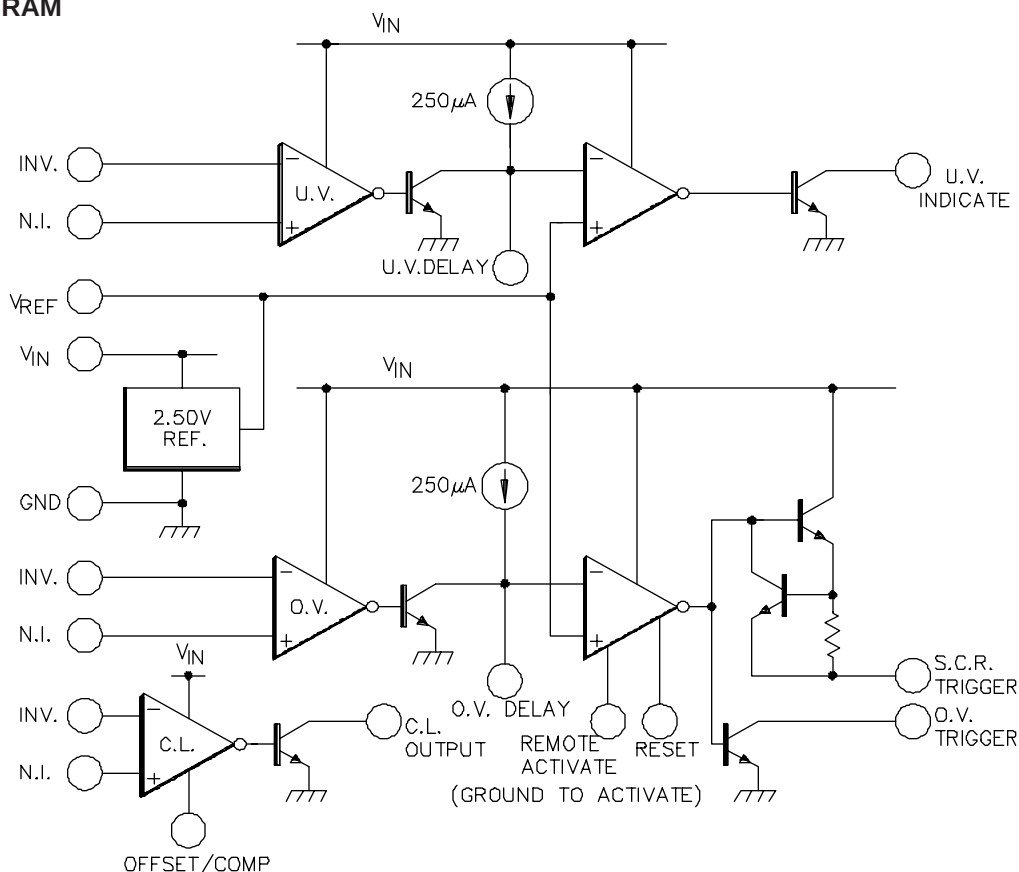
- Uncommitted comparator inputs for wide input flexibility
- Common-Mode range from zero to near supply voltage
- Reference voltage trimmed to 1% accuracy
- Over-voltage, under-voltage, and current sensing circuits all included
- SCR "Crowbar" drive of 300mA
- Programmable time delays
- Open-collector outputs and remote activation capability
- Total standby current less than 10mA

HIGH RELIABILITY FEATURES

- SG1544

- ◆ Available to MIL-STD-883 and DESC SMD
- ◆ LMI level "S" processing available

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (+V_{IN}) 40V
Sense Inputs +V_{IN}
SCR Trigger Current (Note 2) 300mA
Indicator Output Voltage 40V

Indicator Output Sink Current 50mA
Operating Junction Temperature
Hermetic (J Package) 150°C
Plasitc (N, DW Packages) 150°C
Storage Temperature Range -65°C to 150°C

Note 1. Values beyond which damage may occur.

Note 2. At higher input voltages, a dissipation limiting resistor, R_G, is required. See Figure 1.

THERMAL DATA

J Package:

Thermal Resistance-Junction to Case, θ_{JC} 25°C/W
Thermal Resistance-Junction to Ambient, θ_{JA} 70°C/W

N Package:

Thermal Resistance-Junction to Case, θ_{JC} 30°C/W
Thermal Resistance-Junction to Ambient, θ_{JA} 60°C/W

DW Package:

Thermal Resistance-Junction to Case, θ_{JC} 35°C/W
Thermal Resistance-Junction to Ambient, θ_{JA} 90°C/W

RoHS Peak Package Solder Reflow (40 sec. max. exp.)...260°C (+0, -5)

Note A. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.

Note B. The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Supply Voltage (+V_{IN}) 4.7V to 40V
Current Limit Common Mode
Input Voltage Range 0V to +V_{IN} -3V
Reference Load Current 0 to 10mA
Indicator Output Voltage 4.7V to 40V
Indicator Output Current 0 to 10mA

Delay Timing Capacitor (Note 4) 0 to 1μF
Operating Ambient Temperature Range

SG1544 -55°C to 125°C
SG2544 -25°C to 85°C
SG3544 0°C to 70°C

Note 3: Range over which the device is functional.

Note 4: Larger value capacitor may be used with peak current limiting. See Figure 1.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1544 with -55°C ≤ T_A ≤ 125°C, SG2544 with -25°C ≤ T_A ≤ 85°C, SG3544 with 0°C ≤ T_A ≤ 70°C, and +V_{IN} = 10V. Indicator outputs have 2kΩ pull-up resistors. All electrical ratings and specifications are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5V reference. Low duty cycle testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1544/2544			SG3544			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Section								
Input Voltage Range	T _J = 25°C to T _{MAX}	4.5		40	4.5		40	V
		4.7		40	4.7		40	V
Supply Current	+V _{IN} = 40V, Outputs open		7	10		7	10	mA
Reference Section								
Output Voltage	T _J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
		2.45		2.55	2.40		2.60	V
Line Regulation	+V _{IN} = 5 to 30V		1	5		1	5	mV
Load Regulation	I _{REF} = 0 to 10mA		1	10		1	10	mV
Short Circuit Current	V _{REF} = 0V	12	25	40	12	25	40	mA
Temperature Stability			.005			.005		%/°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	SG1544/2544			SG3544			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Comparator Section								
Input Threshold (Note 5)	T _j = 25°C	2.45 2.40	2.50	2.55 2.60	2.40 2.35	2.50	2.60 2.65	V V
Input Hysteresis			25			25		mV
Input Bias Current	Sense input = 0V		0.3	1.0		0.3	1.0	μA
Delay Saturation			0.2	0.5		0.2	0.5	V
Delay High Level			6	8		6	8	V
Delay Charging Current	V _D = 0V	200	250	300	200	250	300	μA
Indicate Saturation	I _L = 10mA		0.2	0.5		0.2	0.5	V
Indicate Leakage	V _{IND} = 40V		.01	1.0		0.1	1.0	μA
Propagation Delay	V _{O.V. N.I. IN} = 2.7V, V _{U.V. INV. IN} = 2.3V, T _j = 25°C							
	C _D = 0		400			400		ns
	C _D = 1μF		10			10		ms
SCR Trigger Section								
Peak Output Current	+V _{IN} = 5V, R _G = 0, V _O = 0	100	200	400	100	200	400	mA
Peak Output Voltage	+V _{IN} = 15V, I _O = 100mA	12	13		12	13		V
Output Off Voltage	+V _{IN} = 40V, R _L = 1KΩ		0	0.1		0	0.1	V
Remote Activate Current	REM. ACT. pin = Gnd		0.4	0.8		0.4	0.8	mA
Remote Activate Voltage	REM. ACT pin open		2	6		2	6	V
Reset Current	RESET pin = Gnd, REM. ACT. = Gnd		0.4	0.8		0.4	0.8	mA
Reset Voltage	RESET pin open, REM. ACT. = Gnd		2	6		2	6	V
Output Current Rise Time	R _L = 50Ω, T _j = 25°C, C _D = 0		400			400		mA/μs
Prop. Delay from REM. ACT. Pin	V _{REM. ACT.} = 0.4V		300			300		ns
Prop. Delay fom O.V. N.I. IN Pin	V _{O.V. N.I. INPUT} = 2.7V		500			500		ns
Current Limit Section								
Input Voltage Range		0		V _{IN} -3V	0		V _{IN} -3V	V
Input Bias Current	OFFSET/COMP pin open, V _{CM} = 0V		0.3	1.0		0.3	1.0	μA
Input Offset Voltage	OFFSET/COMP pin open, V _{CM} = 0V		0	10		0	15	mV
	10Ω from OFFSET/COMP pin to Gnd, T _j = 25°C	80	100	120	70	100	130	mV
CMRR	0 ≤ V _{CM} ≤ 12V, V _{IN} = 15V	60	70		60	70		dB
AVOL	OFFSET/COMP pin open, V _{CM} = 0V	72	80		72	80		dB
Output Saturation	I _L = 10mA		0.2	0.5		0.2	0.5	V
Output Leakage	V _{IND} = 40V		.01	1.0		.01	1.0	μA
Small Signal Bandwidth	A _V = 0dB, T _j = 25°C		5			5		MHz
Propagation Delay	V _{OVERDRIVE} = 100mV, T _j = 25°C		200			200		ns

Note 5. Input voltage rising on O.V. N.I. INPUT and falling on U.V. INV. INPUT.

APPLICATION INFORMATION

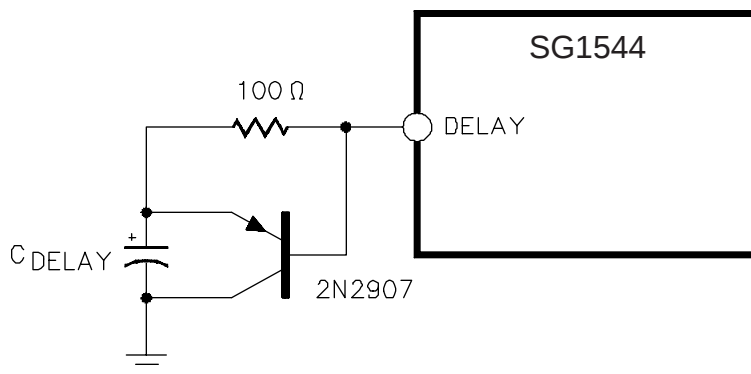


FIGURE 1 - SURGE LIMIT CIRCUIT FOR LARGE DELAY CAPACITORS

The 100 ohm resistor limits the peak discharge current into the SG1544 while the external PNP transistor provides a high peak-current discharge path for the delay capacitor.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
18-PIN CERAMIC DIP J - PACKAGE	SG1544J/883B SG1544JDESC SG1544J SG2544J SG3544J	-55°C to 125°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	SCR TRIGGER REMOTE ACTIVATE RESET O.V. INDICATE O.V. DELAY O.V. N.I. INPUT O.V. INV. INPUT U.V. N.I. INPUT U.V. INV. INPUT 1 2 3 4 5 6 7 8 9 18 17 16 15 14 13 12 11 10 +V_{IN} V_{REF} GROUND C.L. OUTPUT OFFSET / COMP C.L. N.I. INPUT C.L. INV. INPUT U.V. INDICATE U.V. DELAY
18-PIN PLASTIC DIP N - PACKAGE	SG2544N SG3544N	-25°C to 85°C 0°C to 70°C	SCR TRIGGER REMOTE ACTIVATE RESET O.V. INDICATE O.V. DELAY O.V. N.I. INPUT O.V. INV. INPUT U.V. N.I. INPUT U.V. INV. INPUT 1 2 3 4 5 6 7 8 9 18 17 16 15 14 13 12 11 10 +V_{IN} V_{REF} GROUND C.L. OUTPUT OFFSET / COMP C.L. N.I. INPUT C.L. INV. INPUT U.V. INDICATE U.V. DELAY
	N Package: RoHS / Pb-free 100% Matte Tin lead Finish		N Package: RoHS Compliant / Pb-free Transition DC: 0503
18-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2544DW SG3544DW	-25°C to 85°C 0°C to 70°C	SCR TRIGGER REMOTE ACTIVATE RESET O.V. INDICATE O.V. DELAY O.V. N.I. INPUT O.V. INV. INPUT U.V. N.I. INPUT U.V. INV. INPUT 1 2 3 4 5 6 7 8 9 18 17 16 15 14 13 12 11 10 +V_{IN} V_{REF} GROUND C.L. OUTPUT OFFSET / COMP C.L. N.I. INPUT C.L. INV. INPUT U.V. INDICATE U.V. DELAY
	DW Package: RoHS / Pb-free 100% Matte Tin lead Finish		DW Package: RoHS Compliant / Pb-free Transition DC: 0516

Note 1. Contact factory for JAN and DESC product availability.
2. All packages are viewed from the top.