LM193/LM293/LM393/LM2903 Low Power Low Offset Voltage Dual Comparators

Check for Samples: LM193-N, LM2903-N, LM293-N, LM393-N

FEATURES

- Wide Supply
  - Voltage Range: 2.0V to 36V
  - Single or Dual Supplies: ±1.0V to ±18V
- Very Low Supply Current Drain (0.4 mA) — Independent of Supply Voltage
- Low Input Biasing Current: 25 nA
- Low Input Offset Current: ±5 nA
- Maximum Offset voltage: ±3 mV
- Input Common-Mode Voltage Range Includes Ground
- Differential Input Voltage Range Equal to the Power Supply Voltage
- Low Output Saturation Voltage: 250 mV at 4 mA
- Output Voltage Compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Available in the 8-Bump (12 mil) DSBGA Package
- See AN-1112 (SNVA009) for DSBGA Considerations

ADVANTAGES

- High Precision Comparators
- Reduced V_{OS} Drift Over Temperature
- Eliminates Need for Dual Supplies
- Allows Sensing Near Ground
- Compatible with All Forms of Logic
- Power Drain Suitable for Battery Operation

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

The LM393 and LM2903 parts are available in TI's innovative thin DSBGA package with 8 (12 mil) large bumps.

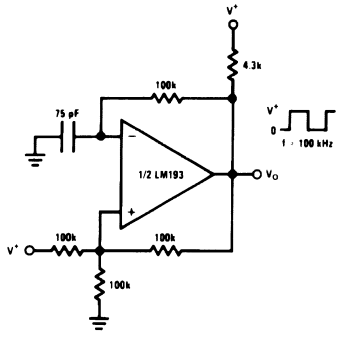

Figure 1. Squarewave Oscillator

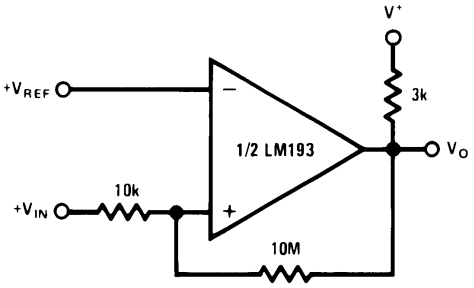

Figure 2. Non-Inverting Comparator with Hysteresis

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Schematic and Connection Diagrams

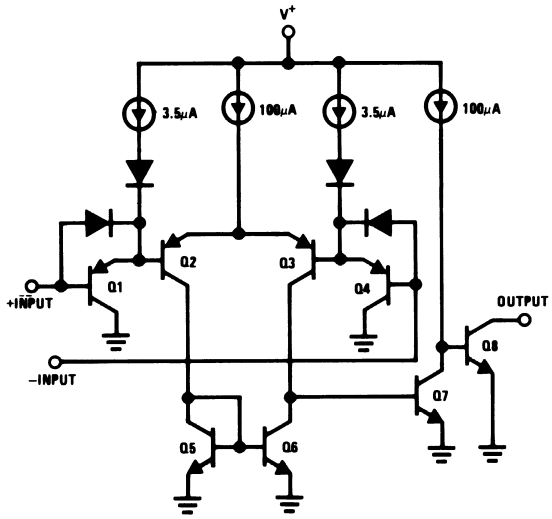

Figure 3. Schematic

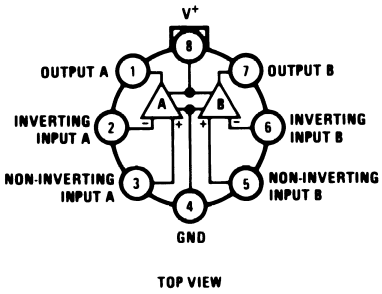

Figure 4. TO-99 Package

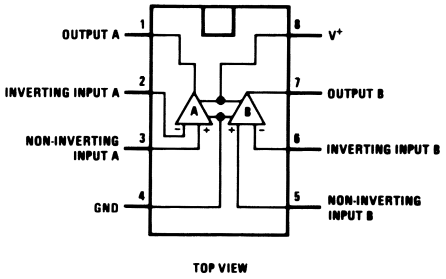

Figure 5. CDIP, PDIP, SOIC Packages

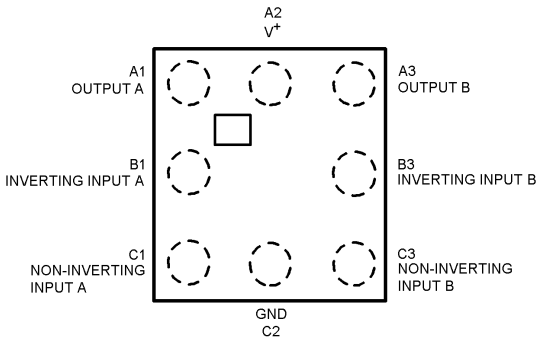

Figure 6. DSBGA Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2]

Supply Voltage, V^+	36V
Differential Input Voltage [3]	36V
Input Voltage	−0.3V to +36V
Input Current (V_{IN}<−0.3V) [4]	50 mA
Power Dissipation [5]	
PDIP	780 mW
TO-99	660 mW
SOIC Package	510 mW
DSBGA Package	568mW
Output Short-Circuit to Ground [6]	Continuous
Operating Temperature Range	
LM393	0°C to +70°C
LM293	−25°C to +85°C
LM193/LM193A	−55°C to +125°C
LM2903	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+260°C
Soldering Information	
CDIP, PDIP Package Soldering (10 seconds)	260°C
SOIC Package	215°C
Vapor Phase (60 seconds)	
Infrared (15 seconds)	220°C
See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.	
ESD rating (1.5 kΩ in series with 100 pF)	1300V

(1) Refer to RETS193AX for LM193AH military specifications and to RETS193X for LM193H military specifications.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).
(4) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V.
(5) For operating at high temperatures, the LM393 and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the “ON-OFF” characteristic of the outputs keeps the chip dissipation very small (P_D≤100 mW), provided the output transistors are allowed to saturate.
(6) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

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Electrical Characteristics

(V^+=5V, T_A = 25°C, unless otherwise stated)

Parameter	Test Conditions		LM193A			Units
			Min	Typ	Max	
Input Offset Voltage	(1)			1.0	2.0	mV
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, V_{CM} = 0V (2)			25	100	nA
Input Offset Current	$I_{IN}(+)-I_{IN}(-)$ V_{CM} = 0V			3.0	25	nA
Input Common Mode Voltage Range	V+ = 30V (3)		0		$V^+-1.5$	V
Supply Current	$R_L=\infty$	V^+=5V		0.4	1	mA
		V^+=36V		1	2.5	mA
Voltage Gain	$R_L \geq 15$ kΩ, V^+=15V V_O = 1V to 11V		50	200		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4V V_{RL}=5V, R_L=5.1 kΩ			300		ns
Response Time	V_{RL}=5V, R_L=5.1 kΩ (4)			1.3		µs
Output Sink Current	$V_{IN}(-)$=1V, $V_{IN}(+)$=0, $V_O \approx 1.5$V		6.0	16		mA
Saturation Voltage	$V_{IN}(-)$=1V, $V_{IN}(+)$=0, $I_{SINK} \leq 4$ mA			250	400	mV
Output Leakage Current	$V_{IN}(-)$=0, $V_{IN}(+)$=1V, V_O=5V			0.1		nA

(1) At output switch point, $V_O \approx 1.4$V, R_S=0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+-1.5$V), at 25°C.
(2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
(3) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+-1.5$V at 25°C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+.
(4) The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see Typical Performance Characteristics.

Electrical Characteristics

(V^+=5V, T_A = 25°C, unless otherwise stated)

Parameter	Test Conditions		LM193			LM293, LM393			LM2903			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(1)			1.0	5.0		1.0	5.0		2.0	7.0	mV
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, V_{CM} = 0V (2)			25	100		25	250		25	250	nA
Input Offset Current	$I_{IN}(+)-I_{IN}(-)$ V_{CM} = 0V			3.0	25		5.0	50		5.0	50	nA
Input Common Mode Voltage Range	V+ = 30V (3)		0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	$R_L=\infty$	V^+=5V		0.4	1		0.4	1		0.4	1.0	mA
		V^+=36V		1	2.5		1	2.5		1	2.5	mA
Voltage Gain	$R_L \geq 15$ kΩ, V^+=15V V_O = 1V to 11V		50	200		50	200		25	100		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4V V_{RL}=5V, R_L=5.1 kΩ			300			300			300		ns
Response Time	V_{RL}=5V, R_L=5.1 kΩ (4)			1.3			1.3			1.5		µs
Output Sink Current	$V_{IN}(-)$=1V, $V_{IN}(+)$=0, $V_O \leq 1.5$V		6.0	16		6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN}(-)$=1V, $V_{IN}(+)$=0, $I_{SINK} \leq 4$ mA			250	400		250	400		250	400	mV
Output Leakage Current	$V_{IN}(-)$=0, $V_{IN}(+)$=1V, V_O=5V			0.1			0.1			0.1		nA

(1) At output switch point, $V_O \approx 1.4$V, R_S=0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+-1.5$V), at 25°C.
(2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
(3) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+-1.5$V at 25°C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+.
(4) The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see Typical Performance Characteristics.

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Electrical Characteristics

(V+ = 5V) (1)

Parameter	Test Conditions	LM193A			Units
		Min	Typ	Max	
Input Offset Voltage	(2)			4.0	mV
Input Offset Current	$I_{IN(+)}-I_{IN(-)}$, V_{CM}=0V			100	nA
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range, V_{CM}=0V (3)			300	nA
Input Common Mode Voltage Range	V^+=30V (4)	0		$V^+-2.0$	V
Saturation Voltage	$V_{IN}(-)$=1V, $V_{IN}(+)$=0, $I_{SINK}\leq$4 mA			700	mV
Output Leakage Current	$V_{IN}(-)$=0, $V_{IN(+)}$=1V, V_O=30V			1.0	µA
Differential Input Voltage	Keep All V_{IN}'s≥0V (or V^-, if Used), (5)			36	V

(1) These specifications are limited to −55°C≤T_A≤+125°C, for the LM193/LM193A. With the LM293 all temperature specifications are limited to −25°C≤T_A≤+85°C and the LM393 temperature specifications are limited to 0°C≤T_A≤+70°C. The LM2903 is limited to −40°C≤T_A≤+85°C.
(2) At output switch point, V_O≈1.4V, R_S=0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+−1.5V), at 25°C.
(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
(4) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+−1.5V at 25°C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+.
(5) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

Electrical Characteristics

(V+ = 5V) (1)

Parameter	Test Conditions	LM193			LM293, LM393			LM2903			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(2)			9			9		9	15	mV
Input Offset Current	$I_{IN(+)}-I_{IN(-)}$, V_{CM}=0V			100			150		50	200	nA
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range, V_{CM}=0V (3)			300			400		200	500	nA
Input Common Mode Voltage Range	V^+=30V (4)	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	V
Saturation Voltage	$V_{IN}(-)$=1V, $V_{IN}(+)$=0, $I_{SINK}\leq$4 mA			700			700		400	700	mV
Output Leakage Current	$V_{IN}(-)$=0, $V_{IN(+)}$=1V, V_O=30V			1.0			1.0			1.0	µA
Differential Input Voltage	Keep All V_{IN}'s≥0V (or V^-, if Used), (5)			36			36			36	V

(1) These specifications are limited to −55°C≤T_A≤+125°C, for the LM193/LM193A. With the LM293 all temperature specifications are limited to −25°C≤T_A≤+85°C and the LM393 temperature specifications are limited to 0°C≤T_A≤+70°C. The LM2903 is limited to −40°C≤T_A≤+85°C.
(2) At output switch point, V_O≈1.4V, R_S=0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+−1.5V), at 25°C.
(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
(4) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+−1.5V at 25°C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+.
(5) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

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Typical Performance Characteristics

LM193/LM293/LM393, LM193A

Supply Current

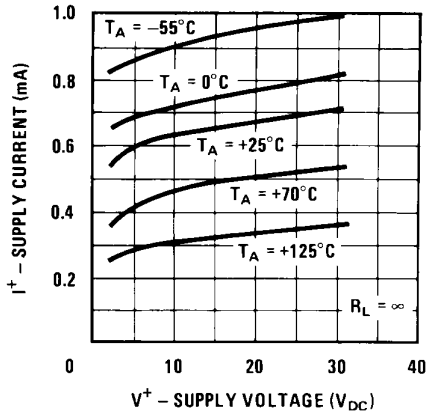

Figure 7.

Input Current

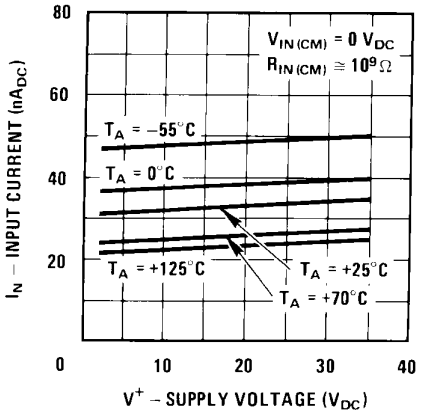

Figure 8.

Output Saturation Voltage

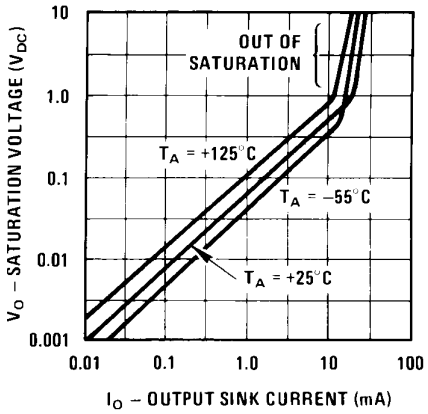

Figure 9.

Response Time for Various Input Overdrives—Negative Transition

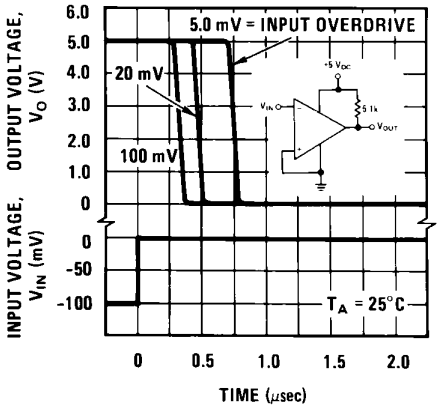

Figure 10.

Response Time for Various Input Overdrives—Positive Transition

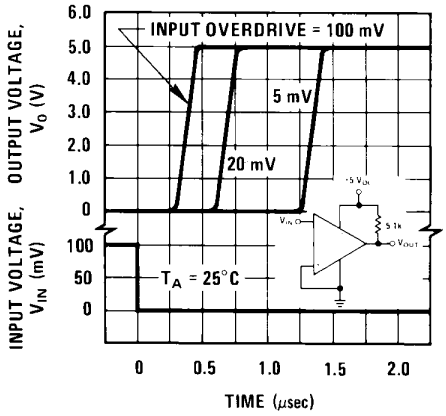

Figure 11.

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Typical Performance Characteristics

LM2903

Supply Current

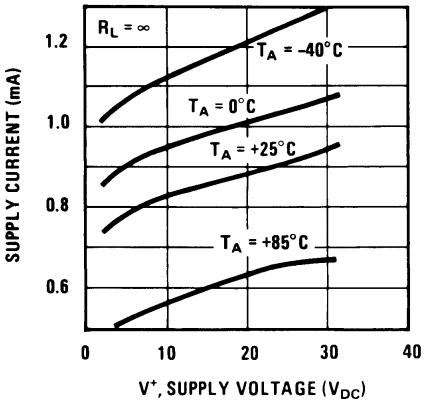

Figure 12.

Input Current

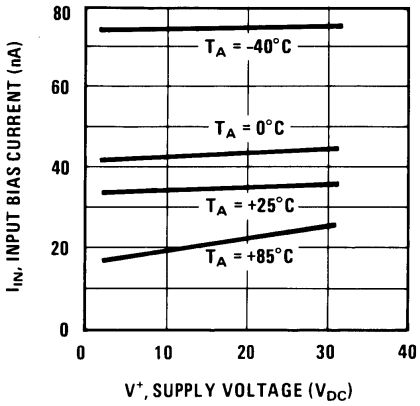

Figure 13.

Output Saturation Voltage

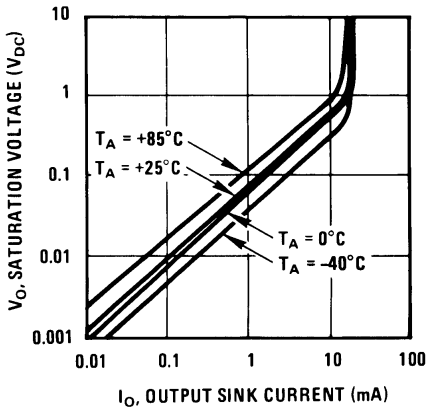

Figure 14.

Response Time for Various Input Overdrives—Negative Transition

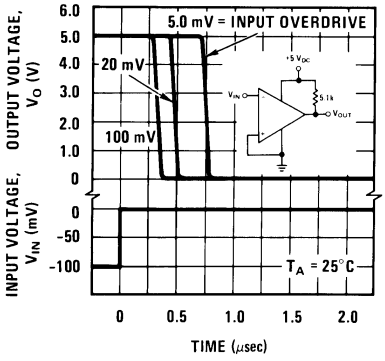

Figure 15.

Response Time for Various Input Overdrives—Positive Transition

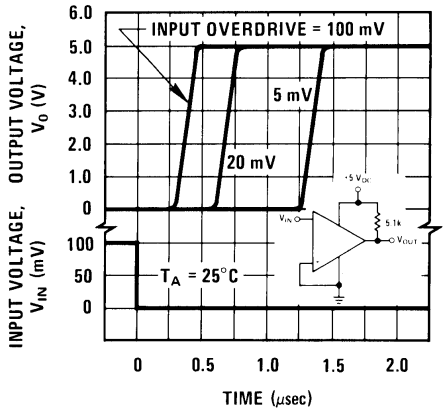

Figure 16.

APPLICATION HINTS

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All input pins of any unused comparators should be tied to the negative supply.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device(1). Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in Typical Applications.

The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications

(V^+=5.0 V_{DC})

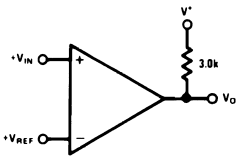

Figure 17. Basic Comparator

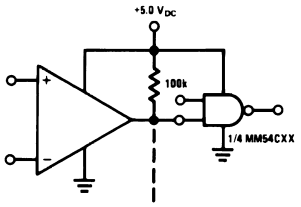

Figure 18. Driving CMOS

(1) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

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(V^+=5.0 V_{DC})

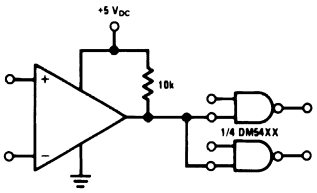


Figure 19. Driving TTL

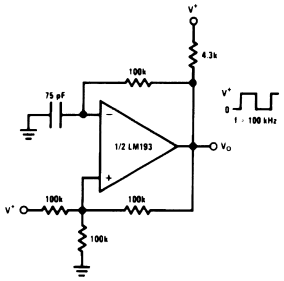


Figure 20. Squarewave Oscillator

* For large ratios of R1/R2,
D1 can be omitted.

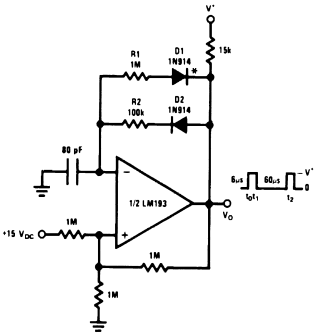


Figure 21. Pulse Generator

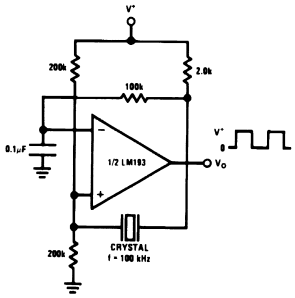
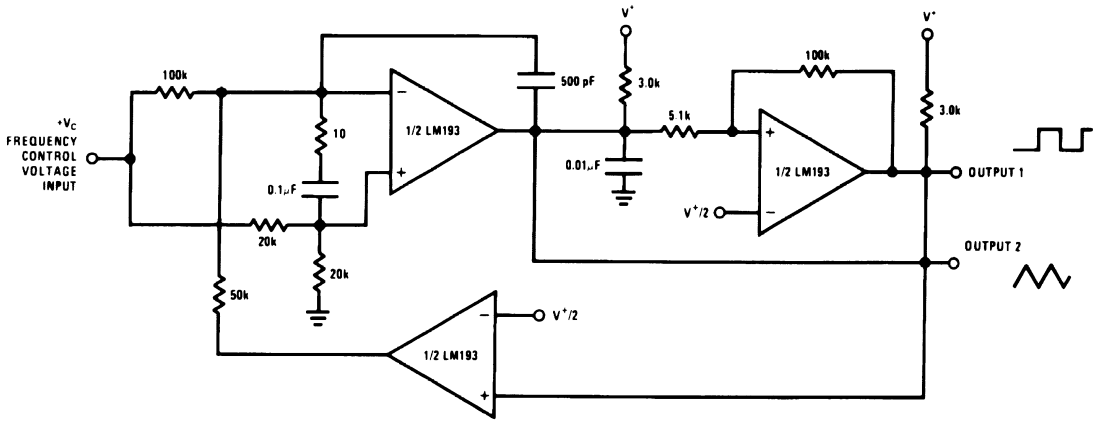


Figure 22. Crystal Controlled Oscillator



V* = +30 V_{DC}
+250 mV_{DC} ≤ V_C ≤ +50 V_{DC}
700Hz ≤ f_o ≤ 100kHz

Figure 23. Two-Decade High Frequency VCO

(V^+=5.0 V_{DC})

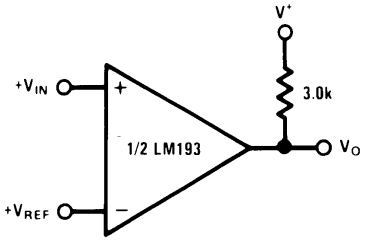


Figure 24. Basic Comparator

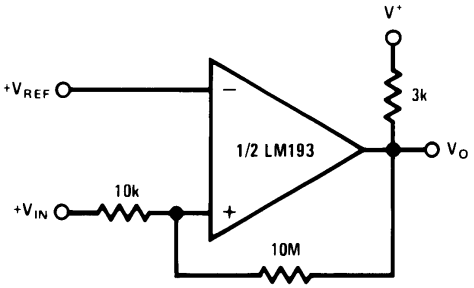


Figure 25. Non-Inverting Comparator with Hysteresis

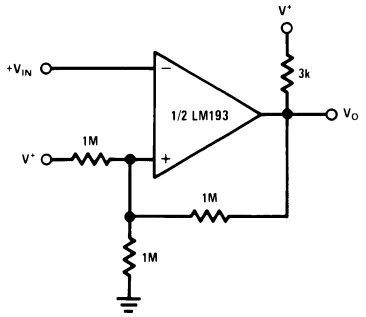


Figure 26. Inverting Comparator with Hysteresis

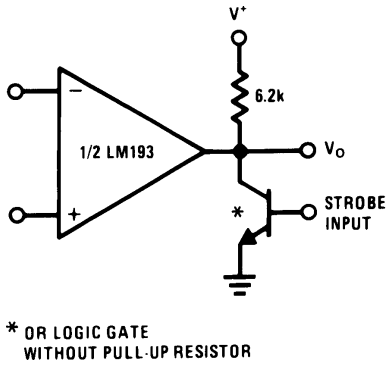


Figure 27. Output Strobing

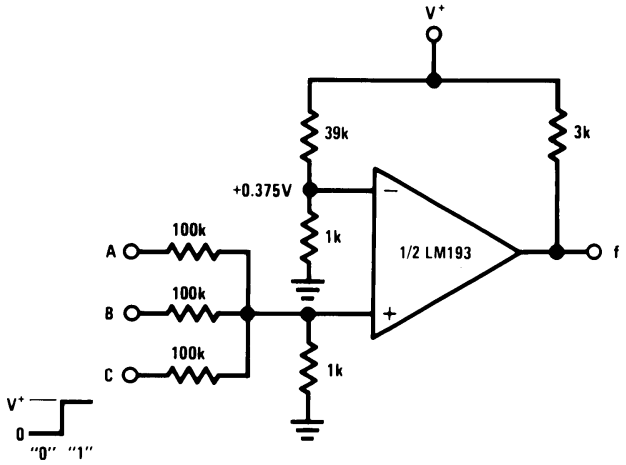


Figure 28. AND Gate

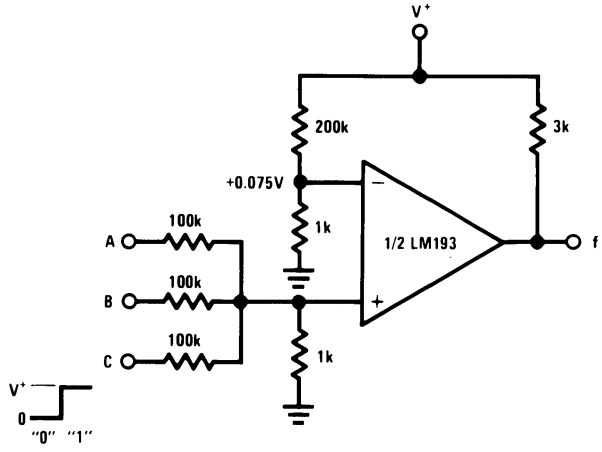


Figure 29. OR Gate

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(V^+=5.0 V_{DC})

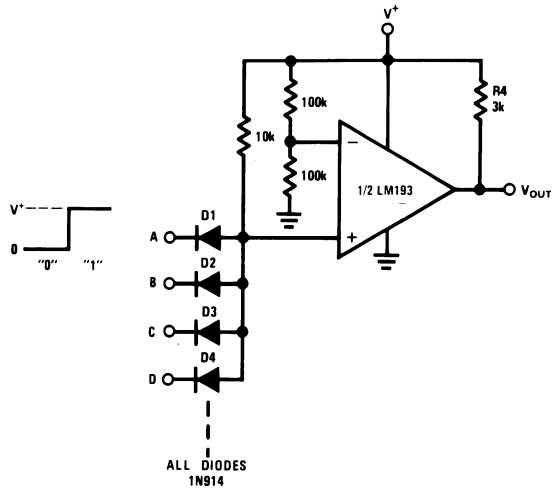

Figure 30. Large Fan-in AND Gate

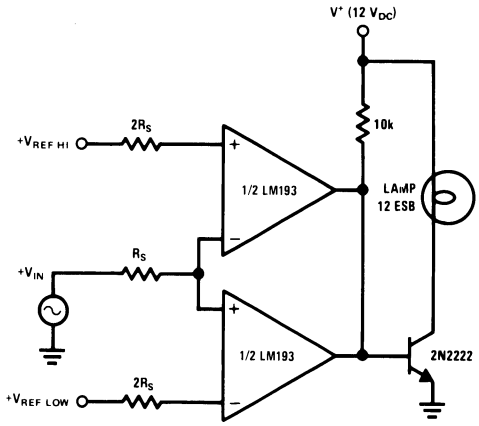

Figure 31. Limit Comparator

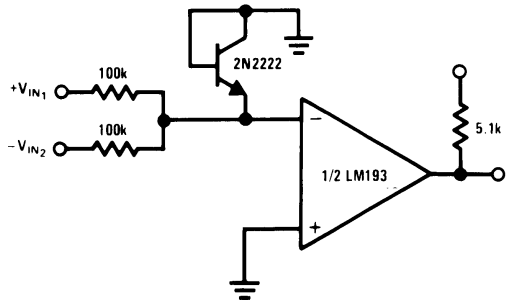

Figure 32. Comparing Input Voltages of Opposite Polarity

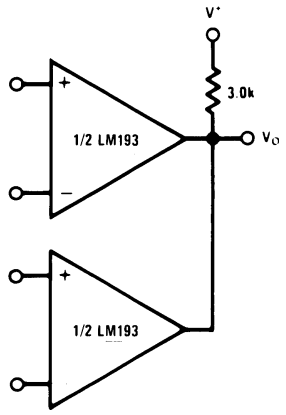

Figure 33. ORing the Outputs

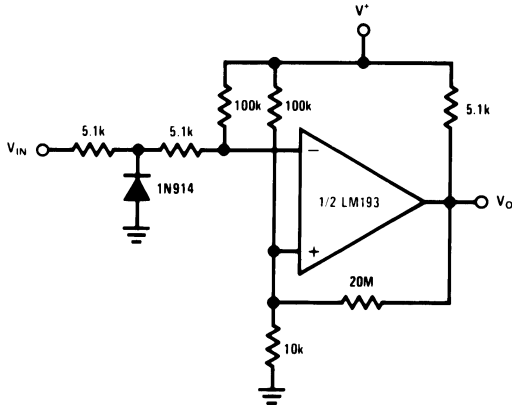

Figure 34. Zero Crossing Detector (Single Power Supply)

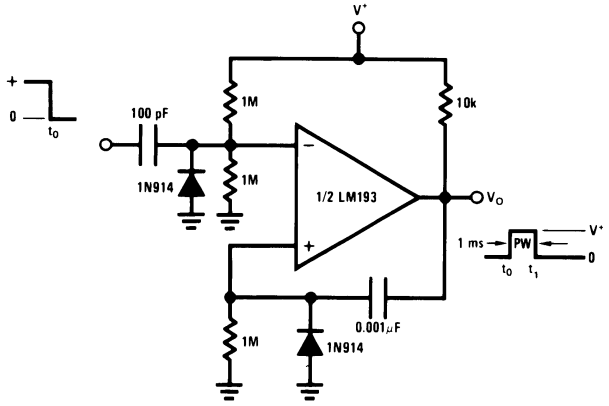

Figure 35. One-Shot Multivibrator

(V^+=5.0 V_{DC})

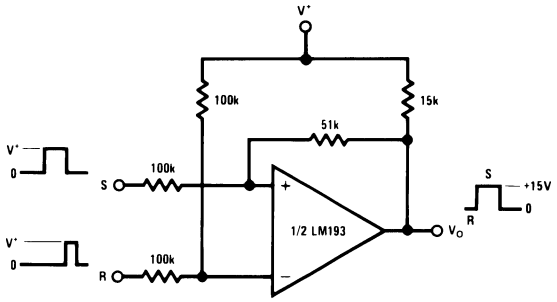

Figure 36. Bi-Stable Multivibrator

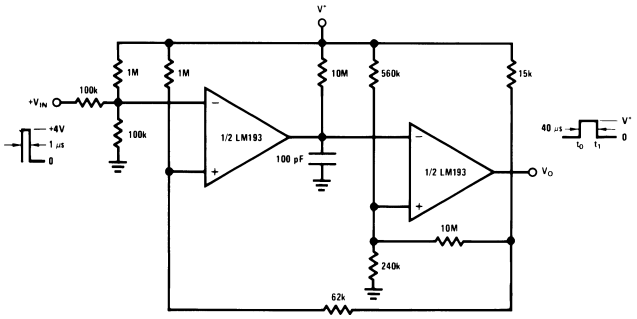

Figure 37. One-Shot Multivibrator with Input Lock Out

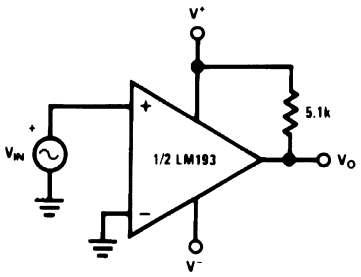

Figure 38. Zero Crossing Detector

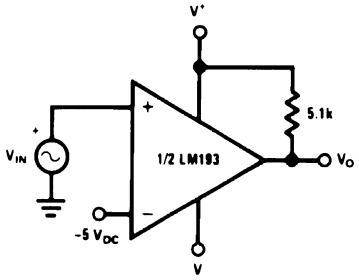

Figure 39. Comparator With a Negative Reference

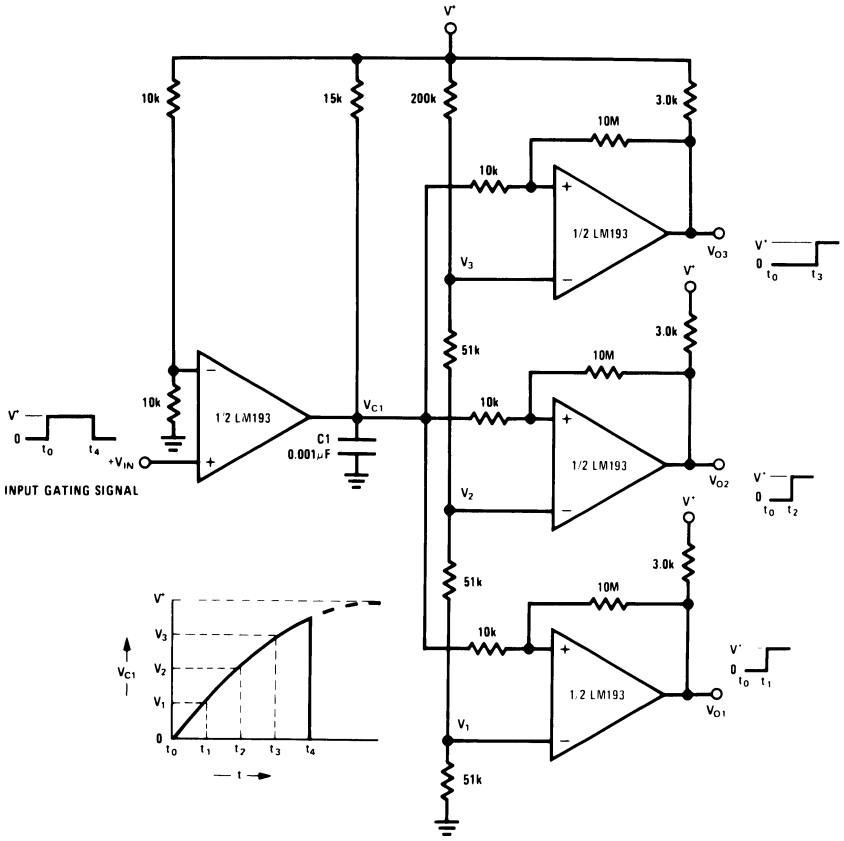

Figure 40. Time Delay Generator

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(V^+=5.0 V_{DC})

Split-Supply Applications

(V^+=+15 V_{DC} and V^-=−15 V_{DC})

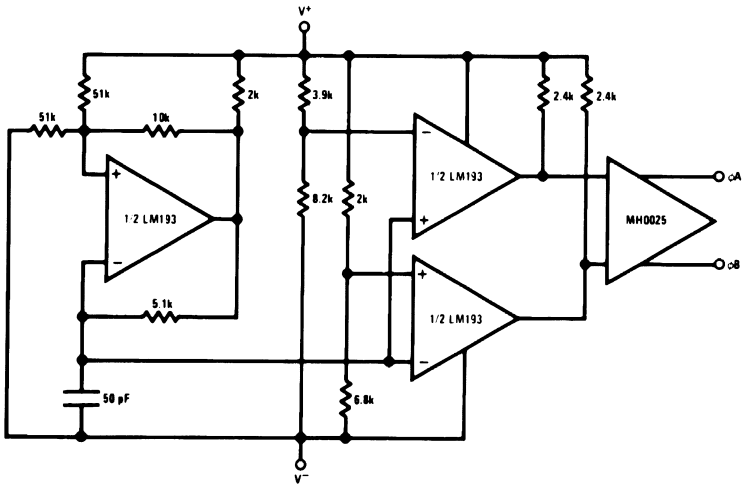

Figure 41. MOS Clock Driver

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	13

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM193AH	ACTIVE	TO-99	LMC	8	500	TBD	Call TI	Call TI	-55 to 125	LM193AH	Samples
LM193AH/NOPB	ACTIVE	TO-99	LMC	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM193AH	Samples
LM193H	ACTIVE	TO-99	LMC	8	500	TBD	Call TI	Call TI	-55 to 125	LM193H	Samples
LM193H/NOPB	ACTIVE	TO-99	LMC	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM193H	Samples
LM2903ITL/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C 03	Samples
LM2903ITLX/NOPB	ACTIVE	DSBGA	YZR	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C 03	Samples
LM2903M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LM 2903M	
LM2903M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 85	LM 2903M	Samples
LM2903MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LM 2903M	
LM2903MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 85	LM 2903M	Samples
LM2903N	LIFEBUY	PDIP	P	8	40	TBD	Call TI	Call TI	-40 to 85	LM 2903N	
LM2903N/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LM 2903N	Samples
LM293H	ACTIVE	TO-99	LMC	8	500	TBD	Call TI	Call TI	-25 to 85	LM293H	Samples
LM293H/NOPB	ACTIVE	TO-99	LMC	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	-25 to 85	LM293H	Samples
LM393M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM 393M	
LM393M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	0 to 70	LM 393M	Samples
LM393MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	LM 393M	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM393MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	0 to 70	LM 393M	Samples
LM393N	LIFEBUY	PDIP	P	8	40	TBD	Call TI	Call TI	0 to 70	LM 393N	
LM393N/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-1-NA-UNLIM	0 to 70	LM 393N	Samples
LM393TL/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	0 to 70	C 02	Samples
LM393TLX/NOPB	ACTIVE	DSBGA	YZR	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	0 to 70	C 02	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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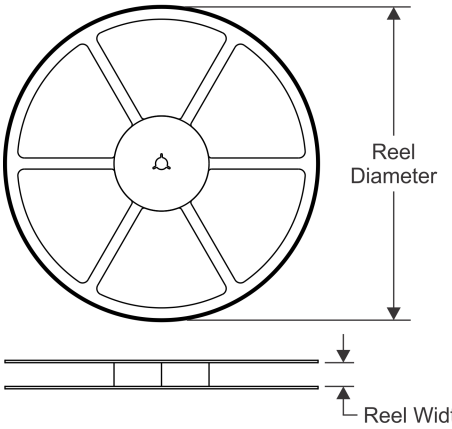
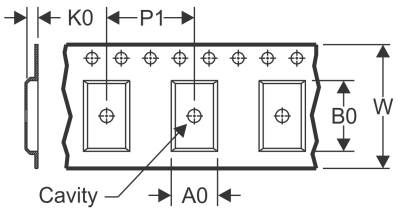
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

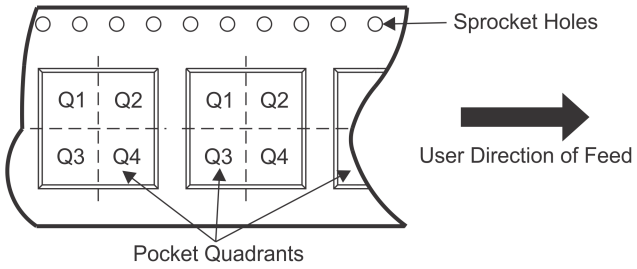


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

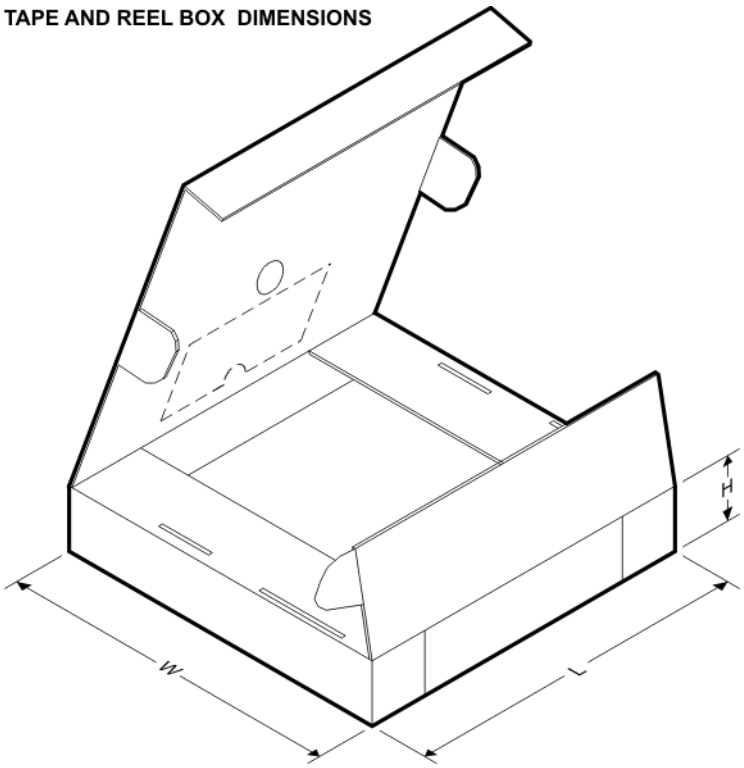
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2903ITL/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LM2903ITLX/NOPB	DSBGA	YZR	8	3000	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LM2903MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2903MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM393MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM393MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM393TL/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LM393TLX/NOPB	DSBGA	YZR	8	3000	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1

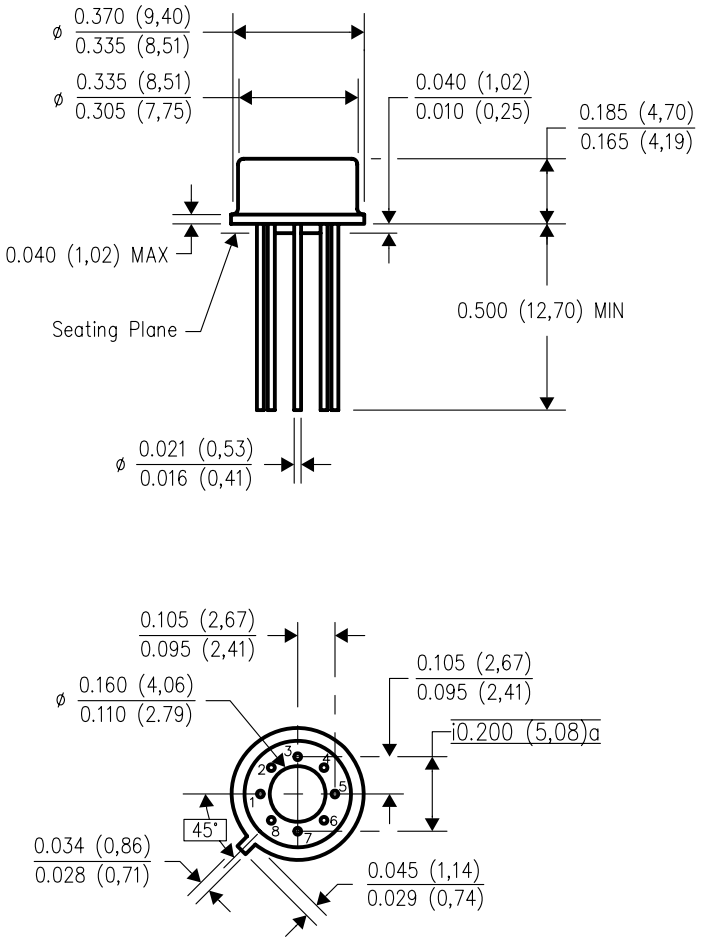
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2903ITL/NOPB	DSBGA	YZR	8	250	210.0	185.0	35.0
LM2903ITLX/NOPB	DSBGA	YZR	8	3000	210.0	185.0	35.0
LM2903MX	SOIC	D	8	2500	367.0	367.0	35.0
LM2903MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM393MX	SOIC	D	8	2500	367.0	367.0	35.0
LM393MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM393TL/NOPB	DSBGA	YZR	8	250	210.0	185.0	35.0
LM393TLX/NOPB	DSBGA	YZR	8	3000	210.0	185.0	35.0

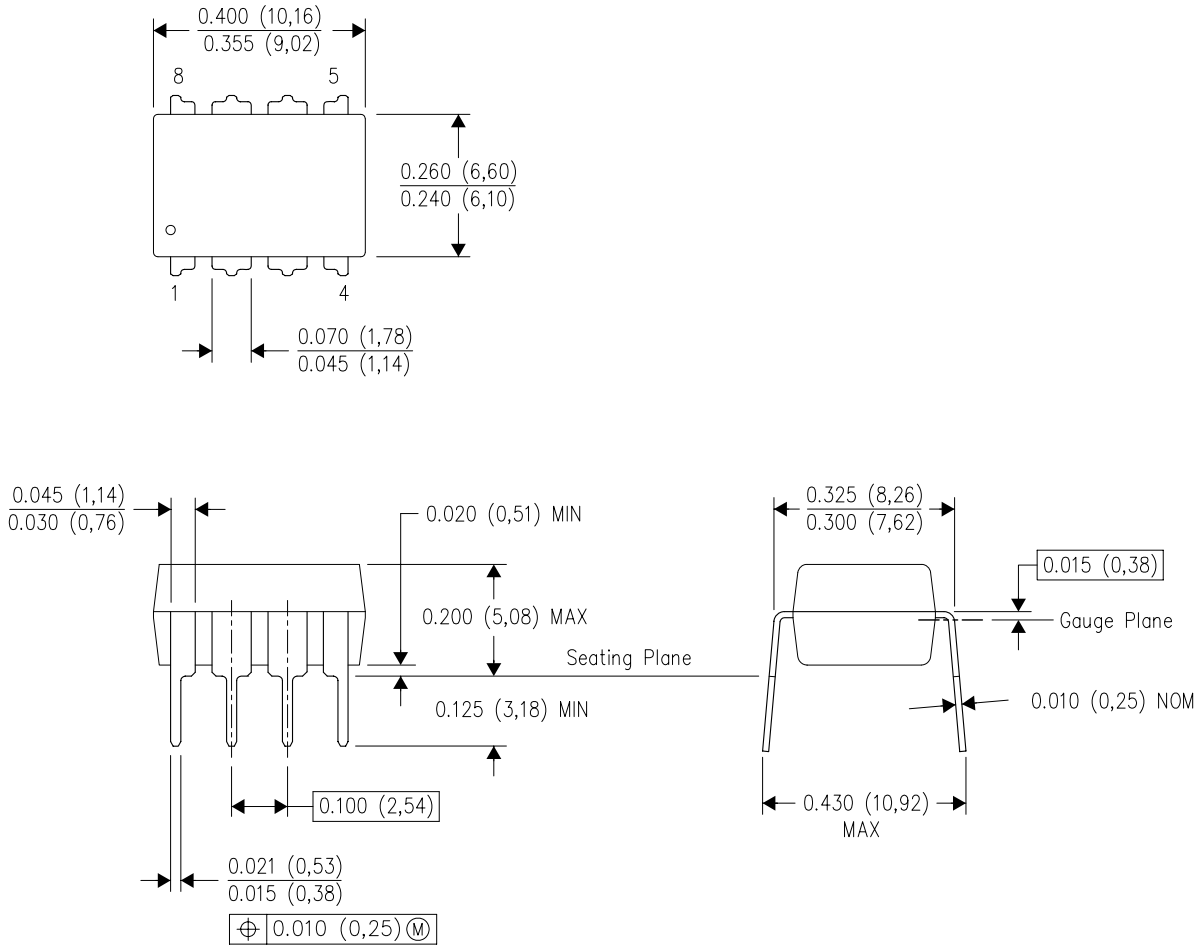
LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

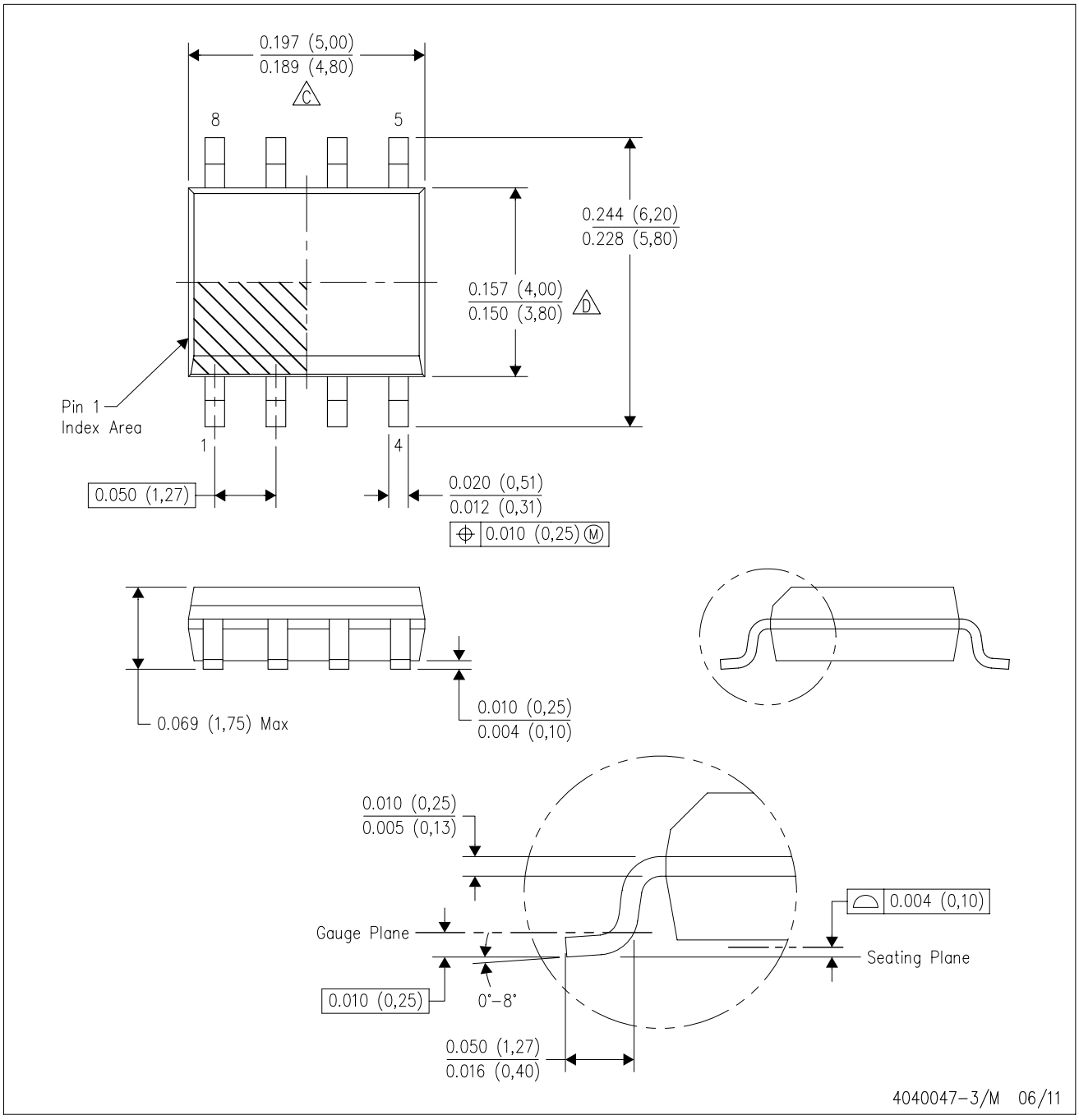
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–002/TO–99.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



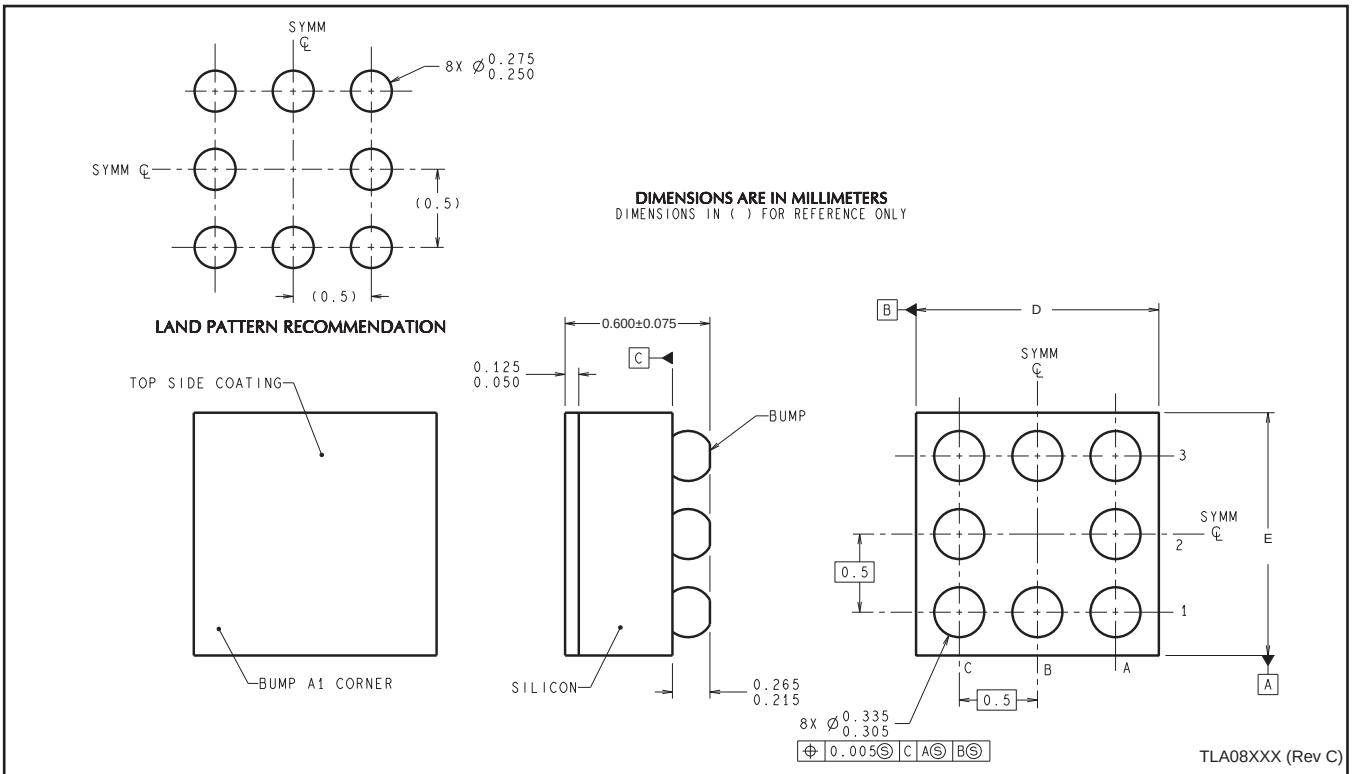
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

YZR0008



D: Max = 1.54 mm, Min = 1.479 mm

E: Max = 1.54 mm, Min = 1.479 mm

4215045/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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