INTEGRATED CIRCUITS
UNITRODE

UC1860
UC2860
UC3860

Resonant Mode Power Supply Controller

FEATURES

- 3MHz VFO Linear over 100:1 Range
- 5MHz Error Amplifier with Controlled Output Swing
- Programmable One Shot Timer—Down to 100ns
- Precision 5V Reference
- Dual 2A Peak Totem Pole Outputs
- Programmable Output Sequence
- Programmable Under Voltage Lockout
- Very Low Start Up Current
- Programmable Fault Management & Restart Delay
- Uncommitted Comparator

DESCRIPTION

The UC1860 family of control ICs is a versatile system for resonant mode power supply control. This device easily implements frequency modulated fixed-on-time control schemes as well as a number of other power supply control schemes with its various dedicated and programmable features.

The UC1860 includes a precision voltage reference, a wide-bandwidth error amplifier, a variable frequency oscillator operable to beyond 3MHz, an oscillator-triggered one-shot, dual high-current totem-pole output drivers, and a programmable toggle flip-flop. The output mode is easily programmed for various sequences such as A, off, B, off; A & B, off; or A, B, off. The error amplifier contains precision output clamps that allow programming of minimum and maximum frequency.

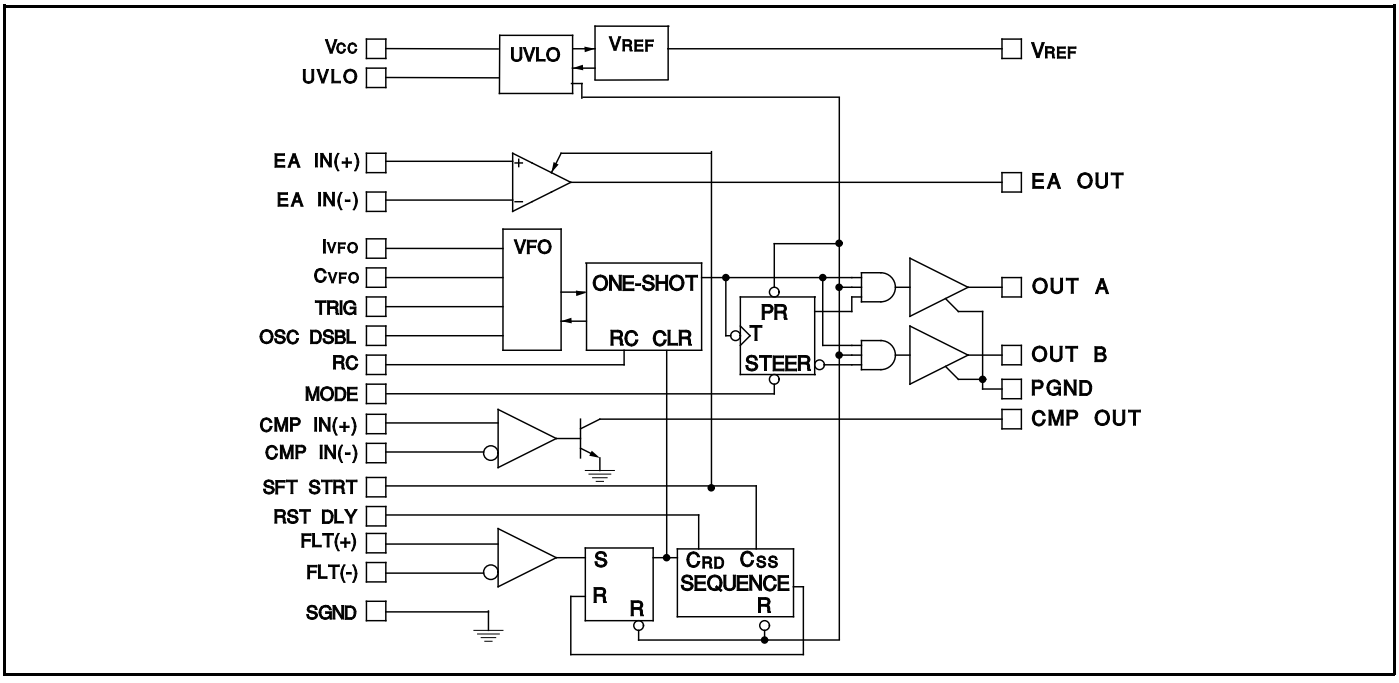
The device also contains an uncommitted comparator, a fast comparator for fault sensing, programmable soft start circuitry, and a programmable restart delay. Hic-up style response to faults is easily achieved. In addition, the UC1860 contains programmable under voltage lockout circuitry that forces the output stages low and minimizes supply current during start-up conditions.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 19) 20V
Output Current, Source or Sink (pins 17 & 20)
  DC 0.8A
  Pulse (0.5µs) 3.0A
Power Ground Voltage . . . . . ±0.2V
Inputs (pins 1, 2, 3, 4, 8, 9, 11, 12,
  13, 14, 21, 22, 23 & 24) . . . . . -0.4 to 6V
Error Amp Output Current, Source or Sink (pin 5) 2mA
I_{VFO} Current (pin 7) 2mA
Comparator Output Current (pin 15) 5mA
Comparator Output Voltage (pin 15) 15V
Soft Start or Restart Delay Sink Current (pins 22 & 23) . . . 5mA
Power Dissipation at T_A = 50°C (DIP) 1.25W
Power Dissipation at T_A = 50°C (PLCC) 1W
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

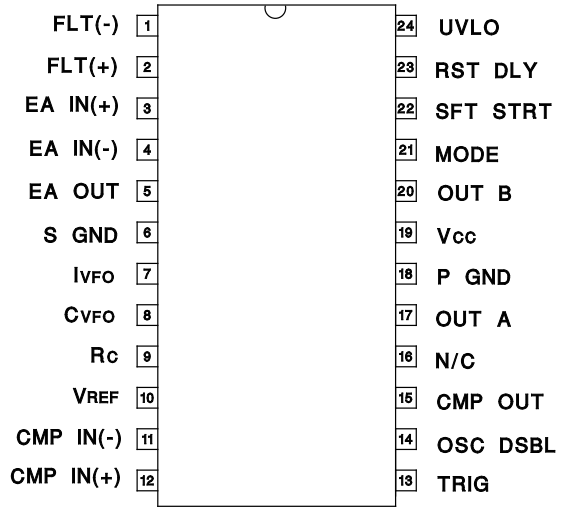
Note: All voltages are with respect to signal ground and all currents are positive into the specified terminal.
Pin numbers refer to the DIP.
Refer to Packaging Section of Databook for thermal limitations and considerations of packages.

BLOCK DIAGRAM

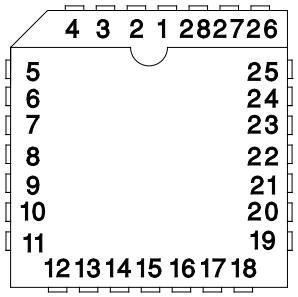


CONNECTION DIAGRAM

DIL - 24 (TOP VIEW)
J or N Package



PLCC-28, LCC-28
(TOP VIEW)
Q or L Package



PIN PACKAGE FUNCTION	
FUNCTION	PIN
S GND	1
I_{VFO}	2
C_{VFO}	3
RC	4
V_{REF}	5
CMP IN (-)	6
CMP IN (+)	7
TRIG	8
OSC DSBL	9
CMP OUT	10
N/C	11, 12
OUT A	13
PGND	14
N/C	15
V_{CC}	16
OUT B	17
N/C	18, 19
MODE	20
SFT STRT	21
RST DLY	22
UVLO	23
FLT (-)	24
FLT (+)	25
EA IN (+)	26
EA IN (-)	27
EA OUT	28

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, all specifications apply for -55°C ≤ T_A ≤ 125°C for the UC1860, -25°C ≤ T_A ≤ 85°C for the UC2860, 0 ≤ T_A ≤ 70°C for the UC3860, V_{CC} = 12V, C_{VFO} = 330pF, I_{VFO} = 0.5mA, C = 330pF, and R = 2.7k, T_A = T_J.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_A = 25°C, I_O = 0	4.95	5.00	5.05	V
	I_O = 0, Over Temp	4.93		5.07	V
Line Regulation	10 ≤ V_{CC} ≤ 20V		2	15	mV
Load Regulation	0≤ I_O ≤ 10mA		2	25	mV
Output Noise Voltage*	10Hz ≤ f ≤ 10kHz		50		μV_{RMS}
Short Circuit Current	V_{REF} = 0V	-150		-15	mA
Error Amplifier Section					
Input Offset Voltage	2.8 ≤ V_{CM} ≤ 4.5V		1	8	mV
Input Bias Current			50	500	nA
Open Loop Gain	dV_O = 1.5V	60	80		dB
PSRR	10 ≤ V_{CC} ≤ 20V	70	100		dB
Output Low (V_O-V_{IVFO})	-0.1 ≤ I_O ≤ 0.1mA	-8	0	8	mV
Output High (V_O-V_{IVFO})	-0.5 ≤ I_O ≤ 0.5mA	1.9	2	2.1	V
Unity Gain Bandwidth*	R_{IN} = 2k	4	5		MHz
Oscillator Section					
Nominal Frequency*		1.0	1.5	2.0	MHz
dF/dI_{OSC}*	100 ≤ I_{VFO} ≤ 500µA	2	3	4	GHz/A

**Guaranteed by design but not 100% tested.*

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PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section (cont'd)					
Trig in Threshold		1.0	1.4	1.8	V
Trig in Open Circuit Voltage		0.7	0.9	1.1	V
Trig in Delta (V_{TH}-V_{OC})		0.3	0.5	0.7	V
Trig in Input Resistance	dV $_{TRIG}$ = V_{OC} to V_{TH}	5	12	25	kΩ
Minimum Trig in Pulse Width*			3	10	ns
Osc. Disable Threshold		1.0	1.4	1.8	V
One Shot Timer					
On Time*		150	200	250	ns
Clamp Frequency*	I_{VFO} = 1.5mA	2.8	3.7	4.6	MHz
Dead Time*	I_{VFO} =1.5mA	35	70	100	ns
Output Stage					
Output Low Saturation	20mA		0.2	0.4	V
	200mA		0.5	2.2	V
Output High Saturation	-20mA		1.5	2.0	V
	-200mA		1.7	2.5	V
Rise/Fall Time*	C_{LOAD} = 1nF		15	30	ns
UVLO Low Saturation	20mA		0.8	1.5	V
Output Mode Low Input				0.4	V
Output Mode High Input		2.0			V
Under Voltage Lockout Section					
V_{CC} Comparator Threshold	On	16	17.3	18.5	V
	Off	9.5	10.5	12	V
UVLO Comparator Threshold	On	3.6	4.2	4.8	V
	Hysteresis	0.2	0.4	0.6	V
UVLO Input Resistance	UVLO = 4/V_{CC} = 8	10	23	50	kΩ
V_{REF} Comparator Threshold	V_{CC} = UVLO = V_{REF}		4.5	4.9	V
Supply Current					
I_{CC}	V_{CC} = 12V, V_{OSC} DSBL = 3V		30	40	mA
I_{START}	UVLO pin open V_{CC} = V_{CC} (on) -0.3V		0.3	0.5	mA
Fault Comparator					
Input Offset Voltage	–0.3 ≤ V_{CM} ≤ 3V		2	10	mV
Input Bias Current	V_{CM} = 0V		100	200	µA
Input Offset Current	V_{CM} = 0V		10	30	µA
Propagation Delay To Output*	±50mV input		100	150	ns
Uncommitted Comparator					
Input Offset Voltage	-0.3 ≤ V_{CM} ≤ 3V		2	10	mV
Input Bias Current	V_{CM} = 0V		100	200	µA
Input Offset Current	V_{CM} = 0V		10	30	µA
Output Low Voltage	I_O = 2mA		0.3	0.5	V
Propagation Delay To Sat*	±50mV input, 2.5k load to 5V		50	100	ns
Soft Start/Restart Control Section					
Saturation Voltage (2 pins)	I_{SINK} = 100µA		0.2	0.5	V
Charge Current (2 pins)		2	5	10	µA
Restart Delay Threshold		2.8	3.0	3.2	V

**Guaranteed by design but not 100% tested.*

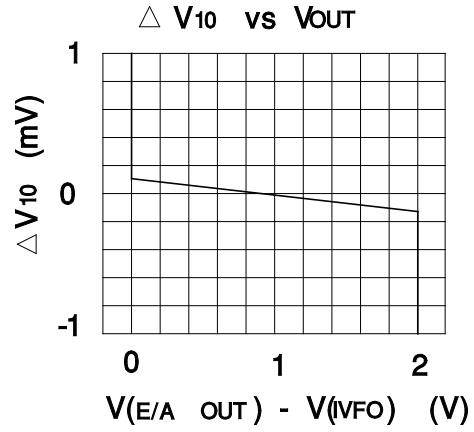
ERROR AMPLIFIER

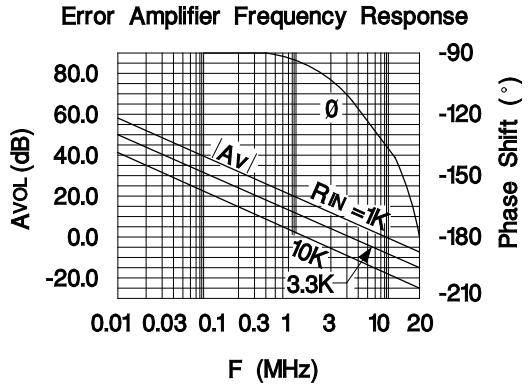
The error amplifier is a high gain, low offset, high bandwidth design with precise limits on its output swing. The bandwidth of the amplifier is externally determined by the resistance seen at the inverting input. Unity gain bandwidth is approximately:

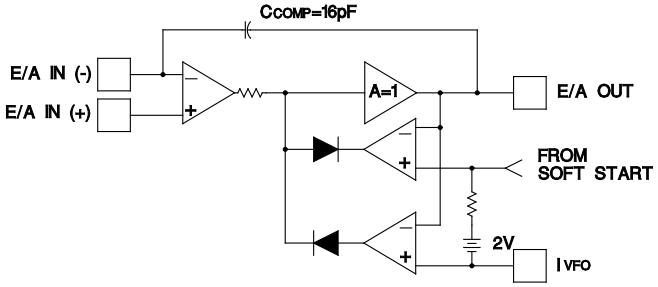
*Frequency (0dB) = 1/(2π * RIN (-) * CCOMP)*

The input common mode range of the amplifier is from 2.8 to 4.5V. As long as one pin is within this range, the other can go as low as zero.

The output swing with respect to the IVFO pin is limited from zero to 2V. Note that pulling Sft Strt (soft start) low will lower the reference of the upper clamp. The lower clamp, however, will dominate should the upper clamp reference drop below the lower reference.





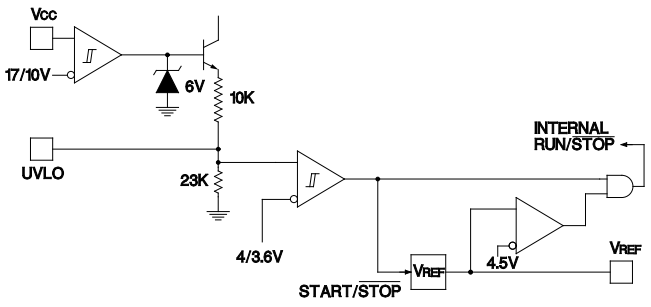


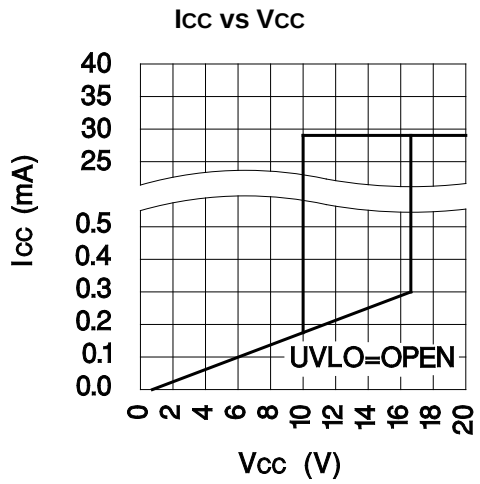
UNDER VOLTAGE LOCKOUT SECTION

The under voltage lockout consists of three comparators that monitor VCC, UVLO and VREF. The VREF comparator makes sure that the reference voltage is sufficiently high before operation begins. When the UVLO comparator is low, the outputs are driven low, the fault latch is reset, the soft start pin is discharged, and the toggle flip-flop is loaded for output A.

The VCC comparator is used for off-line applications by leaving the UVLO pin open. In this application the supply current is typically less than 0.3mA during start-up.

The UVLO comparator is used for DC to DC applications or to gate the chip on and off. To utilize its hysteretic threshold by an external resistive divider, the internal impedance of the pin must be accounted for. To run from a 5V external supply, UVLO, VCC, and VREF are tied together.





VARIABLE FREQUENCY OSCILLATOR

The VFO block is controlled through 4 pins: C_{VFO}, I_{VFO}, Osc Dsbl (oscillator disable), and Trig (trigger input). Oscillator frequency is approximately:

Frequency = $I_{VFO}/(C_{VFO} * 1V)$

With a fixed capacitor and low voltage applied to Trig and Osc Dsbl, frequency is linearly modulated by varying the current into the I_{VFO} pin.

The Trig and Osc Dsbl inputs are used to modify VFO operation. If Osc Dsbl is held high, the oscillator will complete the current cycle but wait until Osc Dsbl is returned low to initiate a new cycle. If a pulse is applied to Trig during a cycle, the oscillator will immediately initiate a new cycle. Osc Dsbl has priority over Trig, but if a trigger pulse is received while Osc Dsbl is high, the VFO will remember the trigger pulse and start a new cycle as soon as Osc Dsbl goes low.

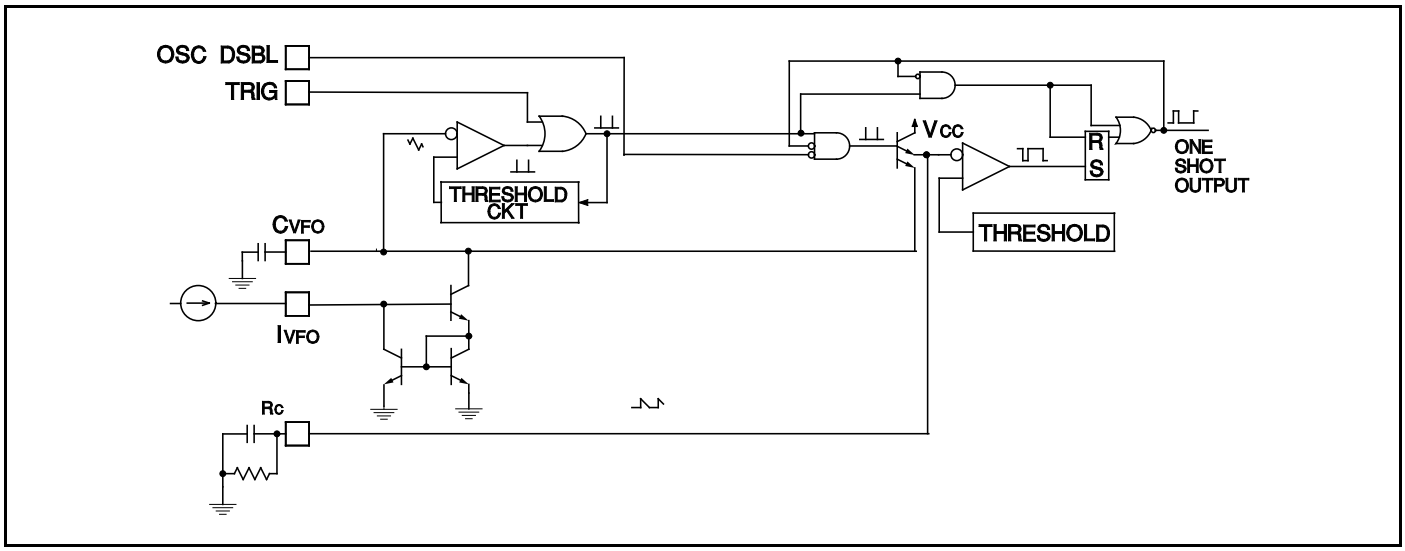
Normally low trigger pulses are used to synchronize the oscillator to a faster clock. Normally high trigger pulses can also be used to synchronize to a slower clock.

ONE SHOT TIMER

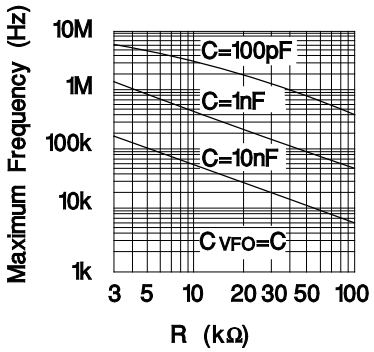
The one shot timer performs three functions and is programmed by the RC pin. The first function is to control output driver pulse width. Secondly, it clocks the toggle flip-flop. Thirdly, it establishes the maximum allowable frequency for the VFO. One shot operation is initiated at the beginning of each oscillator cycle. The RC pin, programmed by an external resistor and capacitor to ground, is charged to approximately 4.3V and then allowed to discharge. The lower threshold is approximately 80% of the peak. On time is approximately:

$t(on) = 0.2 * R * C.$

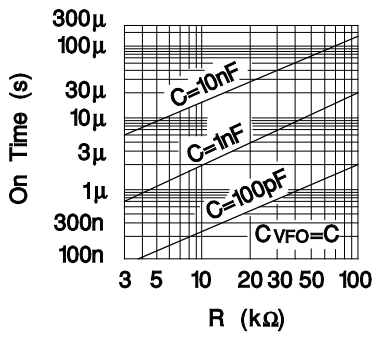
After crossing the lower threshold, the resistor continues to discharge the capacitor to approximately 3V, where it waits for the next oscillator cycle.



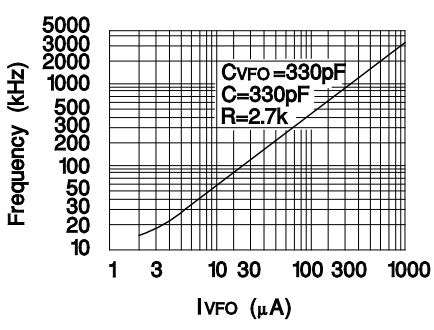
Maximum Frequency vs R

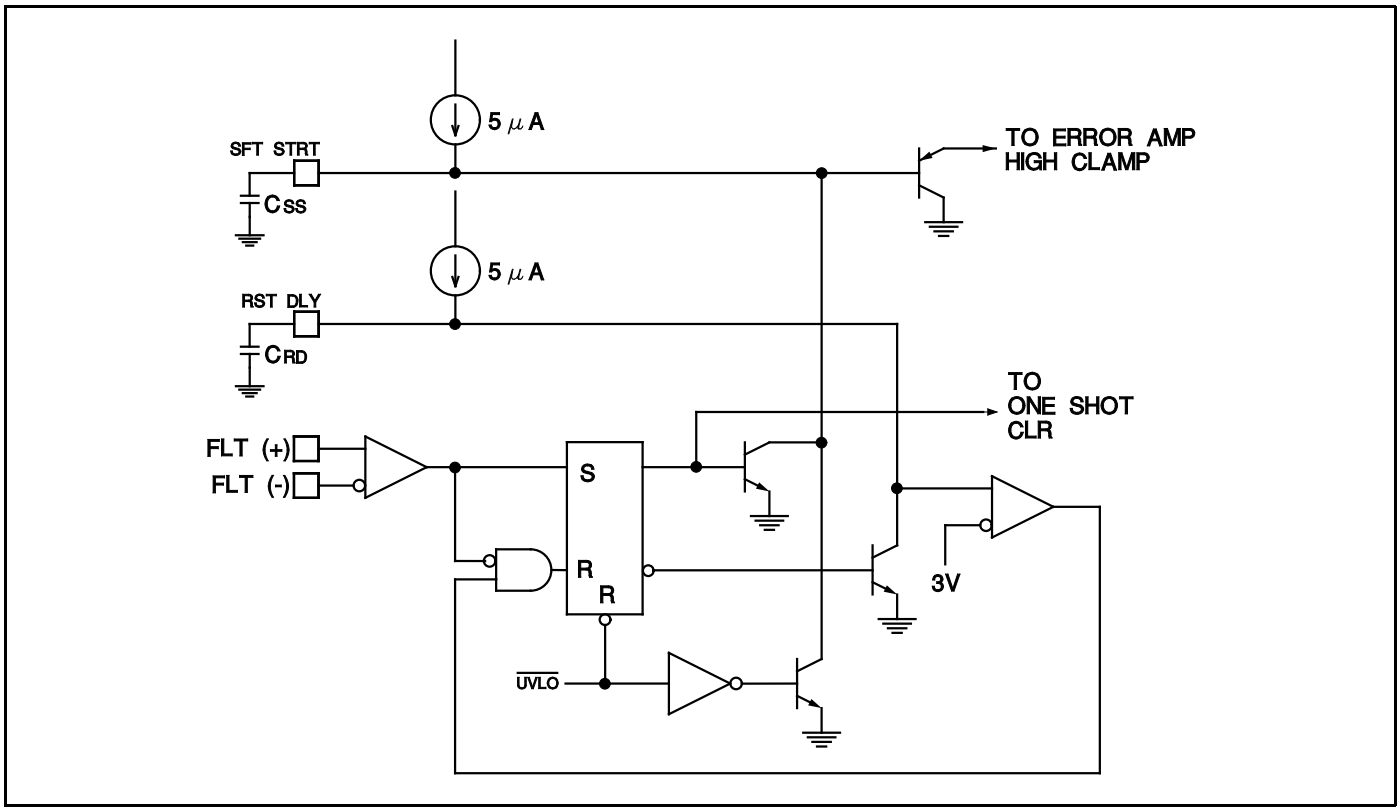


On Time vs R



VFO Frequency vs I_{VFO}





FAULT MANAGEMENT SECTION

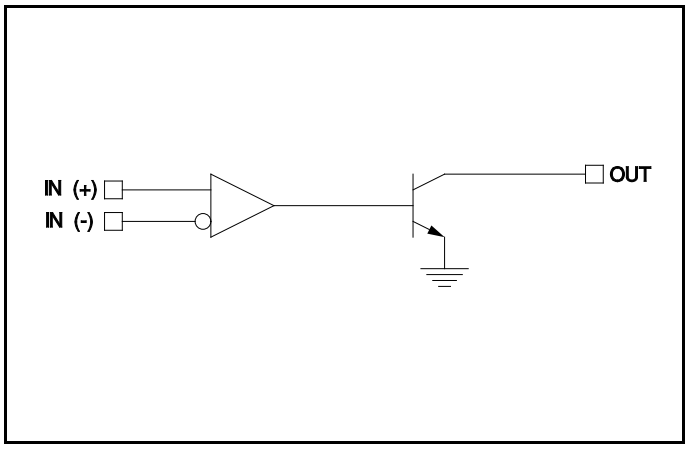
During UVLO, the fault management section is initialized. The latch is reset, and both Sft Strt (soft start) and Rst Dly (restart delay) are pulled low. When Sft Strt is low, it lowers the upper clamp of the error amplifier. As Sft Strt increases in voltage, the upper clamp increases from a value equal to the lower clamp until it is 2V more positive. A capacitor to ground from the Sft Strt pin will control the start rate.

UNCOMMITTED COMPARATOR

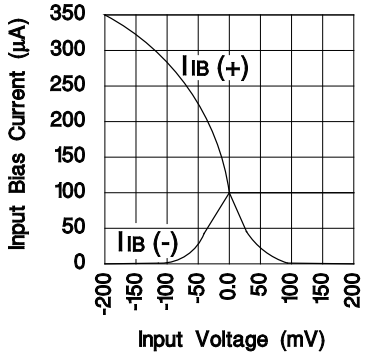
The uncommitted comparator, biased from the reference voltage, operates independently from the rest of the chip. The open collector output is capable of sinking 2mA. The inputs are valid in the common mode range of -0.3 to 3.0V. As long as one of the inputs is within this range, the other can be as high as 5V.

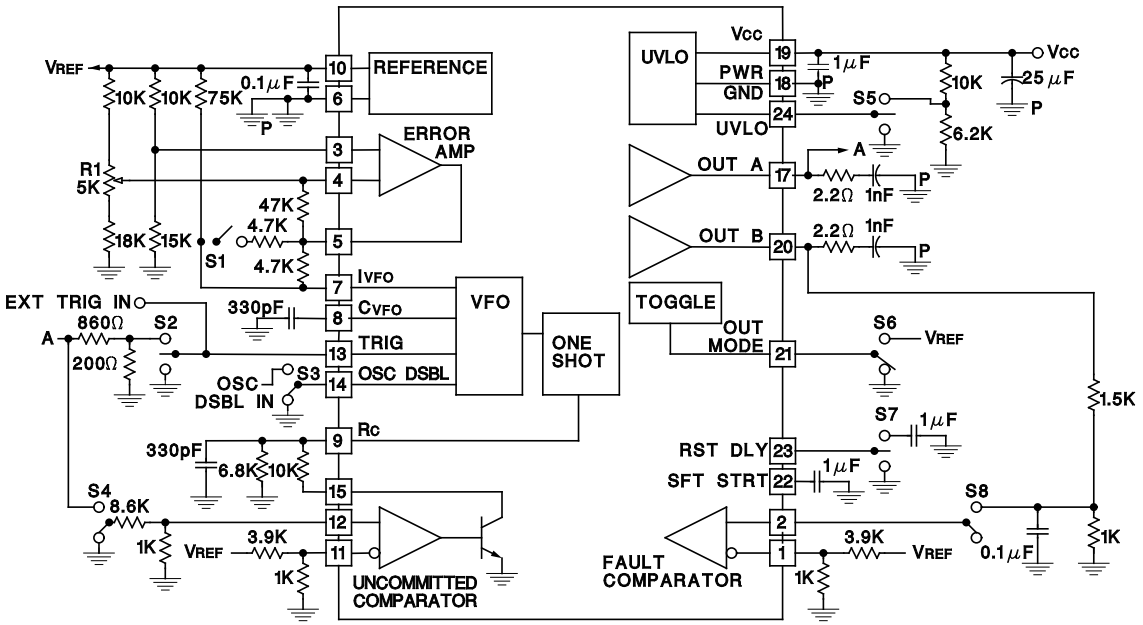
The high speed fault comparator will work over the input common mode range of -0.3 to 3.0V. When a fault is sensed, the one shot is immediately terminated, Sft Strt is pulled low, and Rst Dly is allowed to go high. Three modes of fault disposition can easily be implemented. If Rst Dly is externally held low, then a detected fault will shut the chip down permanently. If the Rst Dly pin is left open, a fault will simply cause an interruption of operation. If a capacitor is connected from Rst Dly to ground, then hic-up operation is implemented. The hic-up time is:

*t (off) = 600 kohm * C(Rst Dly).*



Input Bias Current Input Voltage





NOTE: PIN NUMBERS REFER TO THE DIP

OPEN LOOP LABORATORY TEST FIXTURE

The open loop laboratory test fixture is designed to allow familiarization with the operating characteristics of the UC3860. Note the pin numbers apply to the DIP.

To get started, preset all the options as follows:

Adjust the error amplifier variable resistor pot (R1) so the wiper is at a high potential.

Open the I_{VFO} resistor switch (S1).

Throw the Trig switch (S2) to ground.

Throw the Osc Dsbl switch (S3) to ground.

Throw the uncommitted comparator switch (S4) to ground.

Throw the UVLO switch (S5) to the resistive divider.

Throw the Out Mode switch (S6) to ground.

Open the restart delay switch (S7).

Throw the fault switch (S8)to ground.

In this configuration, the chip will operate for Vcc greater than 12V. Adjustment of the following controls allows examination of specific features.

R1 adjusts the output of the error amp. Notice the voltage at pin 5 is limited from 0 to 2V above the voltage at pin 7.

S1 changes the error amp output to VFO gain. With S1 open, the maximum frequency is determined by the error amp output. With S1 closed, the one shot will set the maximum frequency.

S2 demonstrates the trigger. An external trigger signal may be applied. When the switch is set to the resistive divider, the chip will operate in consecutive mode (ie: A,B, off,...)

S3 allows input of an external logic signal to disable the oscillator.

S4 demonstrates the uncommitted comparator. When set to output A, the comparator will accelerate the discharge of pin 9, shortening the output pulse.

S5 shorted to ground will disable the chip and the outputs will be low. If the switch is open, the V_{CC} start and stop thresholds are 17 and 10V. Switched to the resistive divider, the thresholds are approximately 12 and 10V.

S6 sets the mode of the toggle flip-flop. When grounded, the outputs operate alternately. Switched to 5V, the outputs switch in unison. (Note: If S6 and S2 are set for unison operation and triggered consecutive outputs, the chip will free run at the maximum frequency determined by the one shot.)

S7 open allows the chip to restart immediately after a fault sense has been removed. When grounded, it causes the chip to latch off indefinitely. This state can be reset by UVLO, V_{CC}, or opening the switch. Connected to 1μF programs a hic-up delay time of 600 ms.

S8 allows the simulation of a fault state. When flipped to the RC network, the comparator monitors scaled average voltage of output B. Adjusting frequency will cause the comparator to sense a 'fault' and the chip will enter fault sequence.

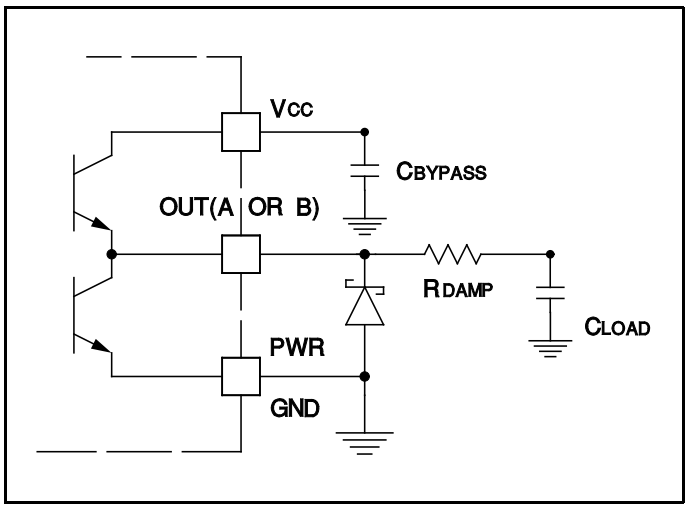
OUTPUT STAGE

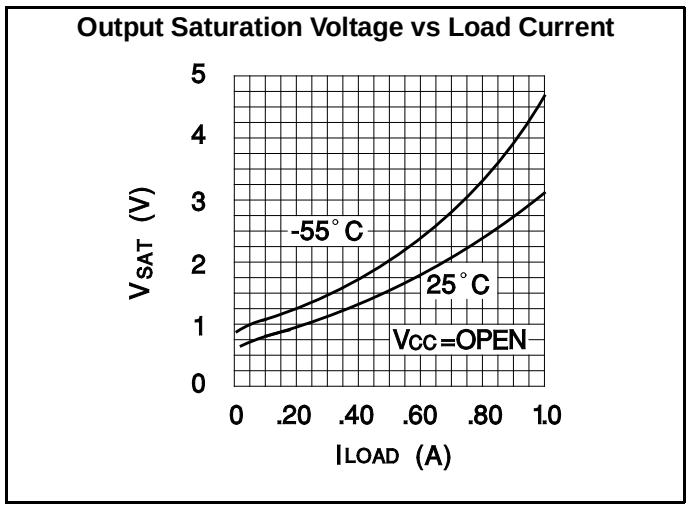
The two totem pole output stages can be programmed by Mode to operate alternately or in unison. When Mode is low the outputs alternate. During UVLO, the outputs are low.

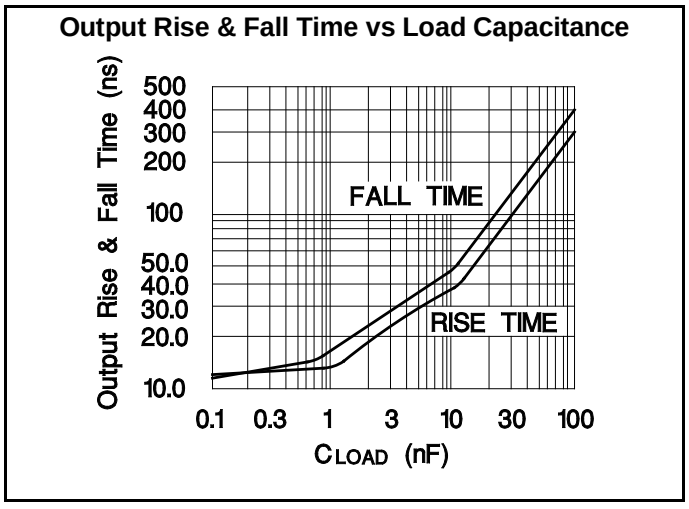
Extreme care needs to be exercised in the application of these outputs. Each output can source and sink transient currents of 2A or more and is designed for high values of dI/dt. This dictates the use of a ground plane, shielded interconnect cables, Schottky diode clamps from the output pins to Pwr Gnd (power ground), and some series resistance to provide damping. Pwr Gnd should not exceed ±0.2V from signal ground.

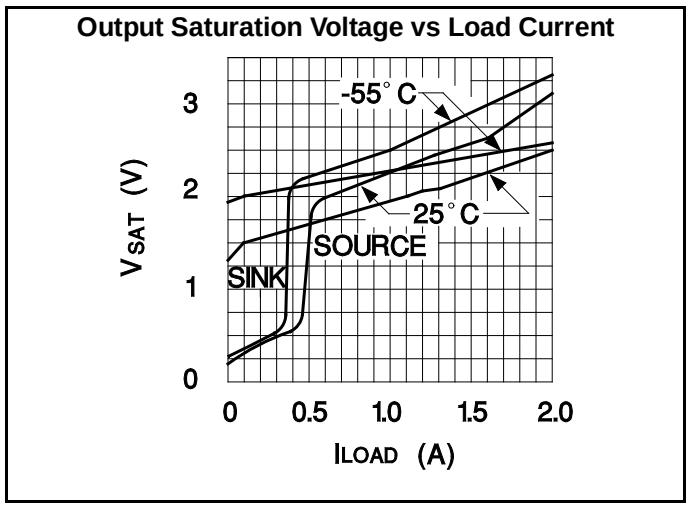
BYPASS NOTE

The reference should be bypassed with a 0.1µF ceramic capacitor from the V_{REF} pin directly to the ground plane near the Signal Ground pin. The timing capacitors on C_{VFO} and RC should be treated likewise. V_{CC}, however, should be bypassed with a ceramic capacitor from the V_{CC} pin to the section of ground plane that is connected to Power Ground. Any required bulk reservoir capacitor should parallel this one. The two ground plane sections can then be joined at a single point to optimize noise rejection and minimize DC drops.









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