TI0254—D3577, JUNE 1990

<ul> <li>Members of Texas Instruments Widebus™</li> <li>Family</li> </ul>	54AC16823, 54ACT16823 WD PACKAGE 74AC16823, 74ACT16823 DL PACKAGE		
<ul> <li>Packaged in Shrink Small-Outline 300-mil</li> </ul>	(TOP VIEW)		
Packages (SSOP) and 380-mil Fine-Pitch			
Ceramic Flat Packages Using 25-mil Center-	1CLR ☐1		
to-Center Pin Spacings	10E		
to-center Fin Spacings	1Q1□3 54□1D1		
<ul> <li>Inputs are TTL- or CMOS-Voltage</li> </ul>	GND 🛛 4 53 🗍 GND		
Compatible	1Q2 🗍 5 52 🗋 1D2		
3-State Outputs Drive Bus Lines Directly	1Q3		
-	V <sub>CC</sub>		
<ul> <li>Flow-Through Architecture Optimizes PCB</li> </ul>	1Q4 🛮 8 49 🗍 1D4		
Layout	1Q5 🗖 9     48 🗍 1D5		
<ul> <li>Distributed V<sub>CC</sub> and GND Pin Configuration</li> </ul>	1Q6 ☐10 47 ☐1D6		
Minimizes High-Speed Switching Noise	GND ☐11 46 ☐ GND		
- •	1Q7 12 45 1D7		
<ul> <li>EPIC™ (Enhanced-Performance implanted</li> </ul>	1Q8		
CMOS) 1-µm Process	1Q9 114 43 1D9		
● 500-mA Typical Latch-Up Immunity at 125°C	2Q1 ☐ 15 42 ☐ 2D1		
,, ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	2Q2 16 41 2D2		
description	2Q3 17 40 2D3		
The 'AC16922 and 'ACT16000	GND 18 39 GND		
The 'AC16823 and 'ACT16823 are nonin-	2Q4 🗍 19 38 🗍 2D4		
verting 18-bit D-type flip-flops composed of two 9-bit sections with separate control signals. For	2Q5   20 37   2D5		
either 9-bit flip-flop section, if the clock enable	206 21 36 206		
(1CLKEN or 2CLKEN) is low, the data present	V <sub>CC</sub>		
at the corresponding D inputs is stored in the	207 23 34 207		
flip-flops on the rising edge of 1CLK (or 2CLK).	2Q8 24 33 2D8		
When 1CLKEN (or 2CLKEN) is high, the flip-	GND		
flops retain their previously stored values.	209 726 31 209		
Taking 1CLR (or 2CLR) low asynchronously	20E   27 30   2CLKEN		
clears the corresponding flip-flops.	2CLR   28 29   2CLK		
sistais the corresponding hip-hops.	ZOLK ∐ZO Z9∐ ZULK		

When the output enable (10E or 20E) is low, the corresponding Q outputs are active (high or low logic levels). When  $1\overline{OE}$  (or  $2\overline{OE}$ ) is high, the corresponding outputs are in the high-impedance state.  $1\overline{OE}$  (or 2OE) does not affect the internal operation of the flip-flops: previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

## **FUNCTION TABLE, EACH SECTION**

	INPUTS				
CLR	CLKEN	CLK	ŌĒ	FLIP-FLOP DATA Q O	Q OUTPUTS
L	X	X	L	L	L
Н	Н	X	L	Previous D Data	Previous D Data
H	X	L	L	Previous D Data	Previous D Data
Н	L	<b>1</b>	L	Current D Data	Current D Data
Н	Н	X	Н	Previous D Data	Z
Н	X	L	Н	Previous D Data	Z
Н	Ĺ	1	Н	Current D Data	Z

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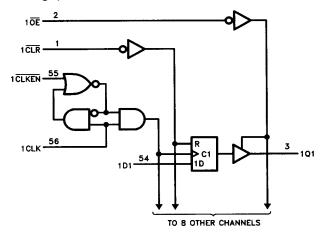


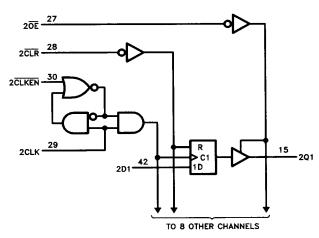
The 74AC16823 and 74ACT16823 are packaged in Ti's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16823 has CMOS-compatible input thresholds. The 'ACT16823 has TTL-compatible input thresholds.

The 54AC16823 and 54ACT16823 are characterized over the full military temperature range of  $-55^{\circ}$ C to 125°C. The 74AC16823 and 74ACT16823 are characterized for operation from  $-40^{\circ}$ C to 85°C.

## logic diagram (positive logic)







3-134

PRODUCT PREVIEW